

FAST<sup>®</sup>  
Advanced Schottky  
TTL Logic  
Databook





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National Semiconductor is an industry leader in the manufacture of high quality, high reliability integrated circuits. We have been the leading proponent of driving down IC defects and extending product lifetimes. From raw material through product design, manufacturing and shipping, our quality and reliability is second to none.

We are proud of our success . . . it sets a standard for others to achieve. Yet, our quest for perfection is ongoing so that you, our customer, can continue to rely on National Semiconductor Corporation to produce high quality products for your design systems.

Charles E. Sporck  
President, Chief Executive Officer  
National Semiconductor Corporation

Charles E. Sporck  
President, Chief Executive Officer  
National Semiconductor Corporation

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National Semiconductor Corporation ist führend bei der Herstellung von integrierten Schaltungen hoher Qualität und hoher Zuverlässigkeit. National Semiconductor war schon immer Vorreiter, wenn es galt, die Zahl von IC Ausfällen zu verringern und die Lebensdauern von Produkten zu verbessern. Vom Rohmaterial über Entwurf und Herstellung bis zur Auslieferung, die Qualität und die Zuverlässigkeit der Produkte von National Semiconductor sind unübertroffen.

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**Une Vocation Commune Chez National Semiconductor Corporation**

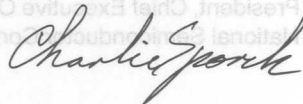
National Semiconductor Corporation est un des leaders industriels qui fabrique des circuits intégrés d'une très grande qualité et d'une fiabilité exceptionnelle. National a été le premier à vouloir faire chuter le nombre de circuits intégrés défectueux et à augmenter la durée de vie des produits. Depuis les matières premières, en passant par la conception du produit sa fabrication et son expédition, partout la qualité et la fiabilité chez National sont sans équivalents.

Nous sommes fiers de notre succès et le standard ainsi défini devrait devenir l'objectif à atteindre par les autres sociétés. Et nous continuons à vouloir faire progresser notre recherche de la perfection; il en résulte que vous, qui êtes notre client, pouvez toujours faire confiance à National Semiconductor Corporation, en produisant des systèmes d'une très grande qualité standard.

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Noi siamo orgogliosi del nostro successo che fissa per gli altri un traguardo da raggiungere. Il nostro desiderio di perfezione è d'altra parte illimitato e pertanto tu, nostro cliente, puoi continuare ad affidarti a National Semiconductor Corporation per la produzione dei tuoi sistemi con elevati livelli di qualità.



Charles E. Sporck  
President, Chief Executive Officer  
National Semiconductor Corporation



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## Table of Contents

Fairchild Advanced Schottky TTL, FAST®, is a family of TTL circuits that exhibits a combination of performance and efficiency unapproached by any other TTL family. Made with the proven Isoplanar process, 54F/74F circuits offer the switching speed and output drive capability of Schottky TTL, with superior noise margins and only one-fourth the power consumption.

### Product Index and Selection Guide

Lists 54F/74F circuits currently available, in design or planned. The Selection Guide groups the circuits by function.

### Section 1 Circuit Characteristics ..... 1-1

Discusses FAST technology, circuit configurations and characteristics.

### Section 2 Ratings, Specifications and Waveforms ..... 2-1

Contains common ratings and specifications for FAST devices, as well as AC test load and waveforms.

### Section 3 Design Considerations ..... 3-1

Provides the designer with useful guidelines for dealing with transmission and other high speed design concerns.

### Section 4 Data Sheets ..... 4-1

Contains data sheets for currently available and pending new products.

### Section 5 Ordering Information and Package Outlines, Field Sales Offices, Representatives and Distributor Locations ..... 5-1

Explains simplified purchasing code which identifies device type, package type and temperature range. Contains detailed physical dimension drawings for each package.



## Product Status Definitions

### Definition of Terms

Data Sheet Identification	Product Status	Definition
<b>Advance Information</b>	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
<b>Preliminary</b>	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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## FAST® Product Selection Guide

### Gates

Function	Device	Inputs/ Gate	No. of Gates	Leads
<b>NAND/NAND Buffer</b>				
Quad 2-Input NAND	54F/74F00	2	4	14
Triple 3-Input NAND	54F/74F10	3	3	14
Dual 4-Input NAND Schmitt Trigger	54F/74F13	4	2	14
Dual 4-Input NAND	54F/74F20	4	2	14
8-Input NAND	54F/74F30	8	1	14
Quad 2-Input Positive NAND Buffer	54F/74F37	2	4	14
Quad 2-Input NAND Buffer (OC)	54F/74F38	2	4	14
Dual 4-Input Positive NAND Buffer	54F/74F40	4	2	14
Quad 2-Input Positive NAND Schmitt Trigger	54F/74F132	2	4	14
<b>AND</b>				
Quad 2-Input AND	54F/74F08	2	4	14
Triple 3-Input AND	54F/74F11	3	3	14
<b>OR/NOR/Exclusive-OR</b>				
Quad 2-Input NOR	54F/74F02	2	4	14
Triple 3-Input NOR	54F/74F27	3	3	14
Quad 2-Input OR	54F/74F32	2	4	14
Quad 2-Input Exclusive-OR	54F/74F86	2	4	14
<b>Invert/AND-OR-Invert</b>				
Hex Inverter	54F/74F04	1	6	14
Hex Schmitt Trigger Inverter	54F/74F14	1	6	14
Dual AND-OR-Invert	54F/74F51	3/3/2/2		14
AND-OR-Invert	54F/74F64	4/2/3/2		14

### Dual Edge Triggered Flip Flops

Function	Device	Clock Inputs	Direct Set	Direct Clear	Leads
Dual D Positive	54F/74F74	✓	Yes	Yes	14
Dual JK Positive	54F/74F109	✓	Yes	Yes	16
Dual JK Negative	54F/74F112	✓	Yes	Yes	16
Dual JK	54F/74F113	✓	Yes		14
Dual JK Negative (Common Clocks & Clears)	54F/74F114	✓	Yes	Yes	14

		Inputs	Reset	Pinout	Outputs	
Hex D Flip-Flop	54F/74F174		Yes			16
Quad D Flip-Flop	54F/74F175		Yes			16
Octal D Flip-Flop	54F/74F273		Yes			20
Octal D Flip-Flop	54F/74F374				Yes	20
Octal D Flip-Flop w/Clock Enable	54F/74F377					20
Parallel D Register w/Enable	54F/74F378					16
Parallel D Register w/Enable	54F/74F379					16
Octal D Flip-Flop	54F/74F534				Yes	20
Octal D Flip-Flop	54F/74F564			Yes	Yes	20
Octal D Flip-Flop	54F/74F574			Yes	Yes	20
10-Bit D Flip-Flop	54F/74F821			Yes	Yes	24
9-Bit D Flip-Flop	54F/74F823		Yes	Yes	Yes	24
8-Bit D Flip-Flop	54F/74F825		Yes	Yes	Yes	24

## Registers

Function	Device	Clock Inputs	Leads
Parallel D Register w/Enable	54F/74F378		16
Quad Parallel D Register w/Enable	54F/74F379		16
Quad 2-Port Register	54F/74F398		20
Quad 2-Port Register	54F/74F399		16
Serial Data Polynomial Generator/Checker	54F/74F402		16
Data Access Register	54F/74F407		24
Register Stack—16 x 4 RAM TRI-STATE Output Register	54F/74F410		18
8-Bit Register with Readback	54F/74F794		20

## Latches

Function	Device	Enable Inputs	Broadside Pinout	Inverting	TRI-STATE Outputs	Leads
Octal Latch	54F/74F373	1(L) & 1(H)			Yes	20
Multimode Buffered 8-Bit Latch	54F/74F412				Yes	24
Multimode Buffered 8-Bit Latch	54F/74F432			Yes	Yes	24
Octal D Latch	54F/74F533	1(L) & 1(H)		Yes	Yes	20
Octal D Latch	54F/74F563	1(L) & 1(H)	Yes	Yes	Yes	20
Octal D Latch	54F/74F573	1(L) & 1(H)	Yes		Yes	20
10-Bit D Latch	54F/74F841	1(L) & 1(H)	Yes		Yes	24
9-Bit D Latch	54F/74F843	1(L) & 1(H)	Yes		Yes	24
8-Bit D Latch	54F/74F845	3(L) & 1(H)	Yes		Yes	24



## Counters

Function	Device	Parallel Entry	Reset	Up/Down	TRI-STATE Outputs	Leads
Presettable 4-Bit BCD Decade	54F/74F160A	S	A			16
Presettable 4-Bit Binary	54F/74F161A	S	A			16
Presettable 4-Bit BCD Decade	54F/74F162A	S	S			16
Presettable 4-Bit Binary	54F/74F163A	S	S			16
4-Bit BCD Decade	54F/74F168	S		Yes		16
4-Bit Binary	54F/74F169	S		Yes		16
4-Bit BCD Decade w/ Preset & Ripple Clock	54F/74F190	A		Yes		16
4-Bit Binary w/ Preset & Ripple Clock	54F/74F191	A				16
4-Bit BCD Decade w/ Separate Up/Down Clocks	54F/74F192	A	A	Yes		16
4-Bit Binary w/ Separate Up/Down Clocks	54F/74F193	A	A	Yes		16
8-Bit Binary	54F/74F269	S		Yes		24
16-Stage Programmable	54F/74F525		A			28
4-Bit BCD Decade	54F/74F568	S	S/A	Yes	Yes	20
4-Bit Binary	54F/74F569	S	S/A	Yes	Yes	20
8-Bit Binary	54F/74F579	S	S	Yes	Yes	20
8-Bit Binary	54F/74F779	S		Yes	Yes	16

S = Synchronous

A = Asynchronous

## Shift Registers

Function	Device	No. of Bits	Serial Inputs	Parallel Inputs	TRI-STATE Outputs	Leads
Shift Right, Serial-In, Parallel-Out	54F/74F164A	8	2			14
Bidirectional, Universal	54F/74F194	4	2	Yes		16
Universal Octal Shift/Storage w/ Common I/O Pins	54F/74F299	8	2	Yes	Yes	20
Octal Serial/Parallel w/ Sign Extend	54F/74F322	8	2	Yes	Yes	20
Universal Octal Shift/Storage w/ Synch. Reset	54F/74F323	8	2	Yes	Yes	20
Serial-In, Serial/Parallel-Out (Common I/O Pin)	54F/74F673A	16	1		Yes	24
Serial-In, Serial/Parallel-Out	54F/74F675A	16	1			24
Serial/Parallel-In, Serial-Out	54F/74F676	16	1	Yes		24

## Buffers/Line Drivers

Function	Device	No. of Bits	Inverting	Noninverting	Broadside Pinout	Leads
Quad Buffer (TRI-STATE)	54F/74F125	4		Yes		14
Octal Buffer/Line Driver (TRI-STATE)	54F/74F240	8	Yes			20
Octal Buffer/Line Driver (TRI-STATE)	54F/74F241	8		Yes		20
Octal Buffer/Line Driver (TRI-STATE)	54F/74F244	8		Yes		20
Hex Buffer/Driver (TRI-STATE)	54F/74F365	6		Yes		16
Hex Inverter/Buffer (TRI-STATE)	54F/74F366	6	Yes			16
Hex Inverter/Buffer (TRI-STATE)	54F/74F368	6	Yes			16
Octal Buffer/Line Driver (TRI-STATE)	54F/74F540	8	Yes		Yes	20
Octal Buffer/Line Driver (TRI-STATE)	54F/74F541	8		Yes	Yes	20
10-Bit Buffer/Line Driver	54F/74F827	10		Yes	Yes	24
10-Bit Buffer/Line Driver	54F/74F828	10	Yes		Yes	24
Octal Buffer/Line Driver with 25Ω Resistor in the Output Pull-Down	54F/74F2241	8		Yes		20
Octal Buffer/Line Driver with 25Ω Resistor in the Output Pull-Down	54F/74F2244	8		Yes		20

## Transceivers/Registered Transceivers

Function	Device	Registered	Enable Inputs	Features	Leads
Quad Bus Transceiver	54F/74F243		1(L) & 1(H)		14
Octal Bidirectional Transceiver	54F/74F245		1(L)	TRI-STATE Inputs	20
Octal Registered Transceiver	54F/74F543	Yes	6(L)		24
Octal Registered Transceiver	54F/74F544	Yes	6(L)	Inverting in Both Directions	24
Octal Bidirectional Transceiver	54F/74F545		1(L)	TRI-STATE Inputs	20
Octal Registered Transceiver	54F/74F550	Yes	4(L)	Status Flags	28
Octal Registered Transceiver	54F/74F551	Yes	4(L)	Status Flags, Inverting	28
Octal Registered Transceiver	54F/74F552	Yes	2(L)	Parity & Flag	28
Octal Bidirectional Transceiver	54F/74F588		1(L)	GPIO Compatible	20
Octal Bus Transceiver	54F/74F620		2(H)	Inverting	20
Octal Bus Transceiver	54F/74F623		2(H)		20
Octal Bus Transceiver	54F/74F640		1(L)	25Ω Resistor in Output Pull-Down, Inverting	20
Octal Bus Transceiver	54F/74F643		1(L)	25Ω Resistor in Output Pull-Down, Invert/Noninvert	20
Octal Bus Transceiver	54F/74F645		1(L)	25Ω Resistor in Output Pull-Down	20
Octal Bus Transceiver	54F/74F646	Yes	1(L) & 1(H)		24
Octal Bus Transceiver	54F/74F648	Yes	1(L) & 1(H)	Inverting	24
Octal Bus Transceiver	54F/74F651	Yes	1(L) & 1(H)	Inverting	24
Octal Bus Transceiver	54F/74F652	Yes	1(L) & 1(H)	Noninverting	24
Octal Bidirectional Transceiver	54F/74F657		1(L) & 1(H)	8-Bit Parity Gen./Checker	24
9-Bit Registered Transceiver	54F/74F899	Yes	2(L)	Parity Generate/Check	28
Quad Bus Transceiver	54F/74F2243		1(L) & 1(H)	25Ω Resistor in Output Pull-Down	20
Quad Bus Transceiver	54F/74F2620		1(L) & 1(H)	25Ω Resistor in Output Pull-Down, Inverting	20
Quad Bus Transceiver	54F/74F2623		1(L) & 1(H)	25Ω Resistor in Output Pull-Down	20
Quad Bus Transceiver	54F/74F2640		1(L)	25Ω Resistor in Output Pull-Down, Inverting	20
Quad Bus Transceiver	54F/74F2643		1(L)	25Ω Resistor in Output Pull-Down, Invert/Noninvert	20
Quad Bus Transceiver	54F/74F2645		1(L)	25Ω Resistor in Output Pull-Down	20
Octal Registered Transceiver	29F52	Yes	4(L)		24
Octal Registered Transceiver	29F53	Yes	4(L)	Inverting	24

## Multiplexers

Function	Device	Enable Inputs	True Output	Complement Output	Leads
8-Input	54F/74F151A	1(L)	Yes	Yes	16
Dual 4-Input	54F/74F153	2(L)	Yes		16
Quad 2-Input	54F/74F157A	1(L)	Yes		16
Quad 2-Input (Inverting)	54F/74F158A	1(L)		Yes	16
8-Input (TRI-STATE)	54F/74F251A	1(L)	Yes	Yes	16
Dual 4-Input (TRI-STATE)	54F/74F253	2(L)	Yes		16
Quad 2-Input (TRI-STATE)	54F/74F257A	1(L)	Yes		16
Quad 2-Input (TRI-STATE, Inverting)	54F/74F258A	1(L)		Yes	16
4-Input w/Shift (TRI-STATE)	54F/74F350	1(L)	Yes		16
Dual 4-Input	54F/74F352	2(L)		Yes	16
Dual 4-Input (TRI-STATE)	54F/74F353	2(L)		Yes	16
Quad 2-Port Register	54F/74F398		Yes	Yes	20
Quad 2-Port Register	54F/74F399		Yes		16

## Decoders/Demultiplexers

Function	Device	Address Inputs	Enable	Output Enable	Outputs	Leads
1-of-8 Decoder/Demultiplexer	54F/74F138	3	2(L) & 1(H)		8(L)	16
Dual 1-of-4 Decoder/Demultiplexer	54F/74F139	2 & 2	1(L) & 1 (L)		4(L) & 4(L)	16
1-of-10 Decoder (TRI-STATE)	54F/74F537	4	1(L) & 1(H)	1(L)	10(H)	20
1-of-8 Decoder (TRI-STATE)	54F/74F538	3	2(L) & 2(H)	2(L)	8(H)	20
Dual 1-of-4 Decoder (TRI-STATE)	54F/74F539	2 & 2	1(L) & 1(L)	1(L) & 1(L)	4(H) & 4(H)	20
Octal Decoder/Demultiplexer w/Latches	54F/74F547	3	1(L) & 2(H)		8(L)	20
Octal Decoder/Demultiplexer w/Acknowledge	54F/74F548	3	2(L) & 2(H)		8(L)	20

## Adders/Subtractors

Function	Device	Master Reset	Carry Lookahead	Leads
Binary Full Adder w/Fast Carry	54F/74F283		Yes	16
Quad Serial Adder/Subtractor	54F/74F385	Yes		20
4-Bit BCD Adder	54F/74F583		Yes	16

## Multipliers

Function	Device	Expandable	Adder/Subtractor	Leads
8-Bit Serial/Parallel Multiplier	54F/74F384	Yes		16
8-Bit Serial/Parallel Multiplier	54F/74F784	Yes	Yes	20

Function	Device	TRI-STATE Outputs	Leads
18 x 4 RAM	54F/74F188	Yes	16
18 x 4 RAM	54F/74F218	Yes	16
18 x 4 FIFO Buffer Memory	54F/74F403	Yes	24
64 x 4 FIFO Buffer Memory	54F/74F413		16
64 x 4 FIFO Buffer Memory	54F/74F433	Yes	24

## Comparators

Function	Device	Features	Leads
8-Bit Identity Comparator	54F/74F521	Expandable	20
8-Bit Comparator	54F/74F524	Expandable, Registered	20
Register/Counter/Comparator	54F/74F701	Expandable	24

## Divider

Function	Device	Features	Leads
16-Stage Programmable Counter/Divider	54F/74F525	Crystal Oscillator	28

## ALUs

Function	Device	No. of Bits	Arithmetic Functions	Logic Functions	Features	Leads
Arithmetic Logic Unit	54F/74F181	4	16	16	Carry Generate/ Propagate Outputs	24
Arithmetic Logic Unit	54F/74F381	4	3	3	Carry Generate/ Propagate Outputs	20
Arithmetic Logic Unit	54F/74F382	4	3	3	Ripple Carry Expansion	20
BCD Adder/Subtractor	54F/74F582	4	2		Lookahead & Ripple Carry Expansion	24

## ALU Support

Function	Device	No. of Bits	Features	Leads
Carry Lookahead Generator	54F/74F182	4	Carry Lookahead Generator for 4 ALUs	16
4-Bit Shifter (Specialized Multiplexer)	54F/74F350	4	Expandable Shifter	16
ALU/Function Generator	54F/74F881	4 & 4		24

## FIFOs

Function	Device	Input	Output	Leads
16 x 4 FIFO Buffer Memory	54F/74F403A	Serial/Parallel	Serial/Parallel	24
FIFO RAM Controller	54F/74F411			20
64 x 4 FIFO Buffer Memory	54F/74F413	Parallel	Serial/Parallel	16
64 x 4 FIFO Buffer Memory	54F/74F433	Serial/Parallel	Serial/Parallel	24

## Memories

Function	Device	TRI-STATE Outputs	Leads
16 x 4 RAM	54F/74F189	Yes	16
16 x 4 RAM	54F/74F219	Yes	16
16 x 4 FIFO Buffer Memory	54F/74F403	Yes	24
64 x 4 FIFO Buffer Memory	54F/74F413		16
64 x 4 FIFO Buffer Memory	54F/74F433	Yes	24



## Memory Support

Function	Device	Features	Leads
Data Access Register	54F/74F407	TRI-STATE Outputs	24
Register Stack—16 x 4 RAM	54F/74F410	TRI-STATE Output Register	18
FIFO RAM Controller	54F/74F411		40
Parallel Check Bit/Syndrome Bit Generator	54F/74F420	TRI-STATE Outputs	48
32-Bit Error Detection & Correction	54F/74F632	Latched, TRI-STATE Outputs	52
1 Megabit Dynamic RAM Controller	54F/74F968	TRI-STATE Outputs	52
Dynamic RAM Controller	29F68	TRI-STATE Outputs	48

## Cyclic Redundancy Checker-Generator

Function	Device	Polynomial Length	Expandable	Leads
Cyclic Redundancy Check Generator/Checker	54F/74F401	16		14
Serial Data Polynomial Generator/Checker	54F/74F402	64	Yes	16

## Parity Generator/Checker

Function	Device	Features	Leads
Parity Generator/Checker	54F/74F280	Odd/Even Outputs, 9-Bits In	14
Parallel Check Bit/Syndrome Bit Generator	54F/74F420		48
Octal Bidirectional Transceiver	54/74F657	Parity Generate/Check	24
9-Bit Registered Transceiver	54/74F899	Parity Generate/Check	28

## Error Detection and Correction

Function	Device	Leads
32-Bit Error Detection and Correction	54F/74F632	52

## Microprocessor Support

Function	Device	Leads
8-Line to 3-Line Priority Encoder	54F/74F148	16

## TTL to ECL Translators

Function	Device	Complementary	Latched	Features
Hex TTL-ECL Translator	F100124	Yes		Enable Input
Hex ECL-TTL Translator	F100125	Yes		Common Mode Rejection = + 1V
Octal ECL-TTL Transceiver	F100128		Yes	ECL Output Cut-Off State

For further information on TTL to ECL translators, refer to the F100K databook.





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Section 1  
Circuit Characteristics



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## Circuit Characteristics

### FAST® Technology

FAST (Fairchild Advanced Schottky TTL) circuits are made with the advanced Isoplanar II process, which produces transistors with very high, well-controlled switching speeds, extremely small parasitic capacitances and  $f_T$  in excess of 5 GHz. Isoplanar is an established National process, used for years in the manufacture of bipolar memories, CMOS, subnanosecond ECL and  $I^2L$  (Isoplanar Integrated Injection Logic) LSI devices.

In the isoplanar process, components are isolated by a selectively grown thick oxide rather than the  $p^+$  isolation region used in the planar process. Since this oxide needs no separation from the base-collector regions, component and chip sizes are substantially reduced. The base and emitter ends terminate in the oxide wall; masks can thus overlap the device area into the isolation oxide. This overlap feature eliminates the extremely close tolerances normally required for base and emitter masking, and the standard photolithographic processes can be used.

Figure 1-1 shows the relative size of phase splitter transistors (Q2 in Figure 1-3) used in Schottky, Low Power Schottky and FAST circuits. The LS-TTL transistor is smaller than that of S-TTL because of process refinements, shall-

lower diffusions and smaller operating currents. The relative size of the FAST and FAST LSI transistors illustrate the reduction afforded by the Isoplanar process. This in turn reduces junction capacitances, while the use of oxide isolation reduces sidewall capacitance. The end result of these reductions is an increase in frequency response by a factor of three or more. Figure 1-2 shows the frequency response of two sizes of transistors made with the Isoplanar II process. Because they have modest, well-defined loads and thus can use smaller, faster transistors, internal gates of MSI devices are faster than SSI gates such as the 'F00 or 'F02. SSI gates, on the other hand, are designed to have high output drive capability and thus use larger transistors.

As is the case with other modern LSI processes, the shallower diffusions and thinner oxides make FAST devices more susceptible to damage from electrostatic discharge than are devices of earlier TTL families. Users should take the usual precautions when handling FAST devices: avoid placing them on non-conductive plastic surfaces or in plastic bags, make sure test equipment and jigs are grounded, individuals should be grounded before handling the devices, etc.

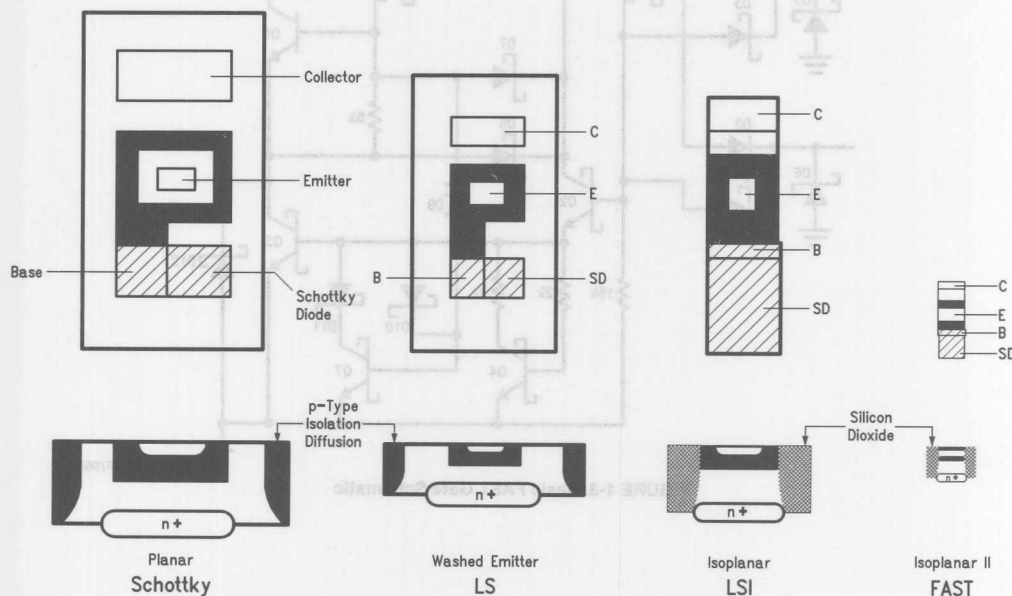
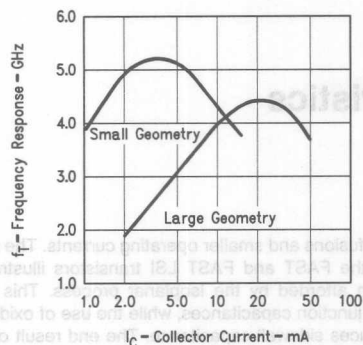


FIGURE 1-1. Relative Transistor Sizes in Various TTL Families

## FAST Technology (Continued)



TL/F/9592-2

FIGURE 1-2. Isoplanar Transistor Frequency Response

## FAST Circuitry

The 2-input NAND gate, shown in Figure 1-3, has three stages of gain (Q1, Q2, Q3) instead of two stages as in other TTL families. This raises the input threshold voltage and increases the output drive. The higher threshold makes it possible to use pn diodes for the input AND function (D1 and D2) and still achieve an input threshold of 1.5V.

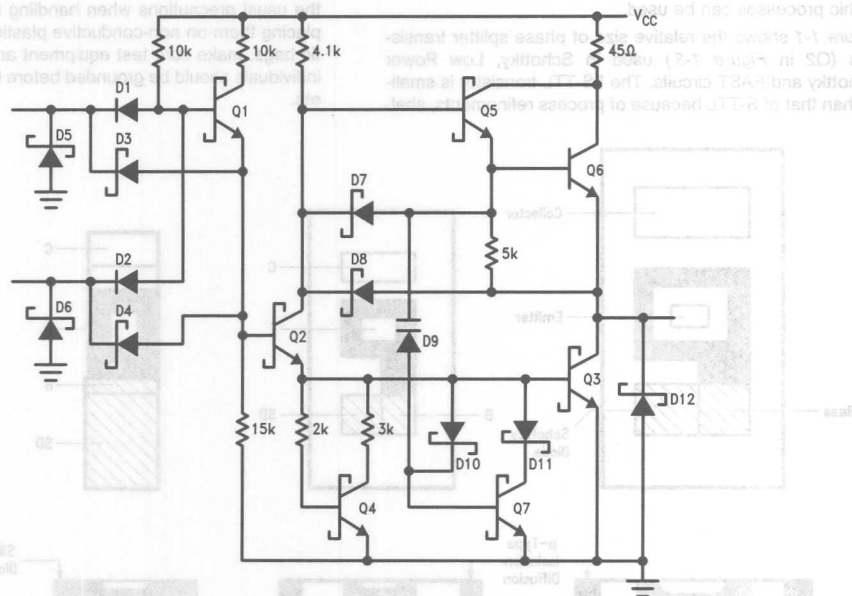


FIGURE 1-3. Basic FAST Gate Schematic

TL/F/9592-3

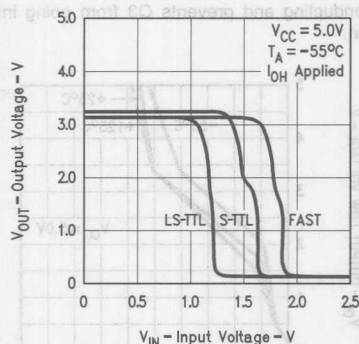
The capacitance of these diodes is comparatively low, which results in improved AC noise immunity. The effect of the threshold adjustment can be seen in the voltage transfer characteristics of Figures 1-4, 1-5 and 1-6. At 25°C (Figure 1-5) the FAST circuit threshold is nearly centered between the 0.8V and 2.0V limits specified for TTL circuits. This gives a better balance between the HIGH- and LOW-state noise margins. The +125°C characteristics (Figure 1-6) show that the FAST circuits threshold is comfortably above the 0.8V specification, more so than in S-TTL or LS-TTL circuits. At -55°C, the FAST circuit threshold is still well below the 2.0V specification, as shown in Figure 1-4.

FAST circuits contain several speed-up diodes to help discharge internal capacitances. Referring again to Figure 1-3, when a HIGH-to-LOW transition occurs at the D1 input, for example, Schottky diode D3 acts as a low-resistance path to discharge the several parasitic capacitances connected to the base of Q2. This effect only comes into play, however, as the input signal falls below about 1.2V; D3 does not act as an entry path for negative spikes superimposed on a HIGH input level. When Q2 turns ON and its collector voltage falls, D7 provides a discharge path for capacitance at the base of Q6. Whereas D3, D4 and D7 enhance switching speed by helping to discharge internal nodes, D8 contributes to the ability of a FAST circuit to rapidly discharge load capacitance. Part of the charge stored in load capacitance passes through D8 and Q2 to increase the base current of Q3 and increase Q3's current sinking capability during the HIGH-to-LOW output voltage transition.



**FAST Circuitry** (Continued)

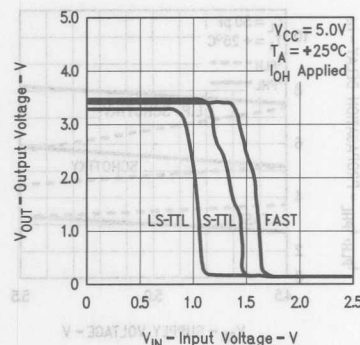
In addition to the 2K-Q4-3K squaring network, which is standard for Schottky-clamped TTL circuits, FAST circuits contain a network D9-D10-D11-Q7 whose purpose is to provide a momentary low impedance at the base of Q3 during an output LOW-to-HIGH transition. The rising voltage at the emitter of Q5 causes displacement current to flow through varactor diode D9 and momentarily turn ON Q7, which in turn pulls down the base of Q3 and absorbs the displacement current that flows through the collector-base capacitance (not shown) of Q3 when the output voltage rises. Without the D9-Q7 network, the displacement current through the collector-base capacitance acts as base current, tending to prolong the turn-off of Q3 and allow current to flow from Q6 to ground through Q3.

**FIGURE 1-4. Transfer Functions at Low Temperature**

The collector-base capacitance of Q3, although small, is effectively multiplied by the voltage gain of Q3. This phenomenon, first identified many years ago with vacuum tube triodes, is called the Miller effect. Thus the D9-Q7 network is familiarly called the 'Miller Killer' circuit and its use improves the output rise time and minimizes power consumption during repetitive switching at high frequencies. Diode D10 completes the discharge path for D9 through D7 when Q2 turns on. D11 limits how low Q7 pulls down the base of Q3 to a level adequate for the intended purpose, without sacrificing turn-on speed when a circuit is cycled rapidly.

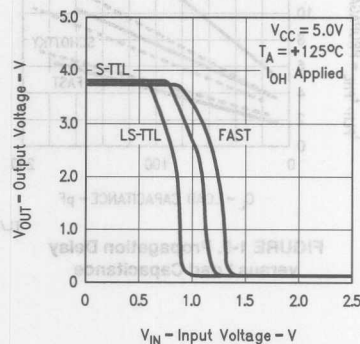
Also shown in Figure 1-3 is a clamp diode, D12, at the output. This diode limits negative voltage excursions due to parasitic coupling in signal lines or transmission line effects.

The Schottky clamping diodes built into the transistors prevent saturation, thereby eliminating storage time as a factor in switching speed. Similarly, the speed-up diodes tend to minimize the impact of other variables on switching speed. The overall effect is to minimize variation in switching speed of FAST circuits with variations in supply voltage and ambient temperature (Figures 1-7 and 1-8). Propagation delay is specified not only under nominal supply voltage and temperature conditions, but also over the recommended operating range of  $V_{CC}$  and  $T_A$  for both military and commercial grade devices.

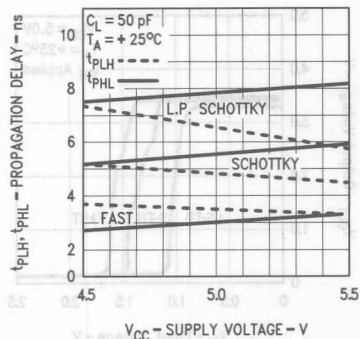
**FIGURE 1-5. Transfer Functions at Room Temperature**

The internal switching speed of a logic circuit is only one aspect of the circuit's suitability for high-speed operations at the system or subsystem level; the other aspect is the ability of the circuit to drive load capacitance. FAST circuit outputs are structured to sink at least 20 mA in the LOW state, the same as S-TTL. This capability plus the effect of the aforementioned feedback through D8 assures that the circuit can rapidly discharge capacitance. During a LOW-to-HIGH transition, the pull-up current is limited by the 45Ω resistor, versus 55Ω for S-TTL. Therefore, FAST circuits are inherently more capable than S-TTL of charging load capacitance.

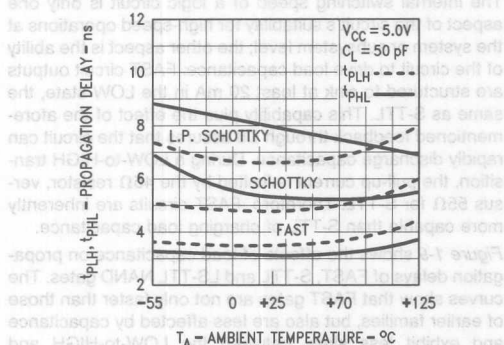
Figure 1-9 shows the effects of load capacitance on propagation delays of FAST, S-TTL and LS-TTL NAND gates. The curves show that FAST gates are not only faster than those of earlier families, but also are less affected by capacitance and exhibit less skew between the LOW-to-HIGH and HIGH-to-LOW delays. These improved characteristics offered by FAST circuits make it easier to predict system performance early in the design phase, before loading details are precisely known. The curves show that the skew between HIGH-to-LOW and LOW-to-HIGH delays for the FAST gate is only about 0.5 ns over a broad range of load capacitance, whereas the skew for the S-TTL gate is 1 ns or greater, depending on loading.

**FIGURE 1-6. Transfer Functions at High Temperature**

## FAST Circuitry (Continued)

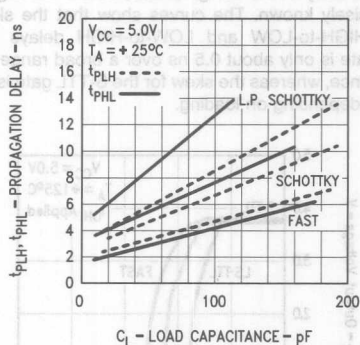


TL/F/9592-7

FIGURE 1-7. Propagation Delay versus  $V_{CC}$ 

TL/F/9592-8

FIGURE 1-8. Propagation Delay versus Temperature

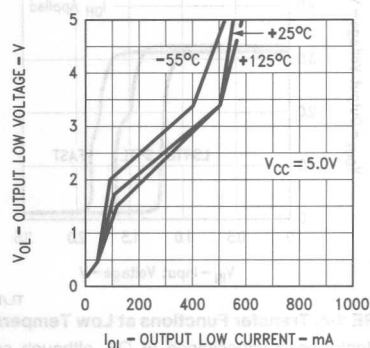


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FIGURE 1-9. Propagation Delay versus Load Capacitance

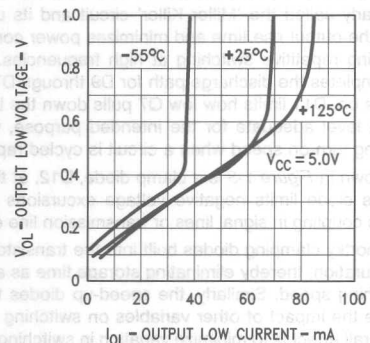
## Output Characteristics

Figure 1-10 shows the current-voltage characteristics of a FAST gate with the pull-down transistor Q3 turned ON. These curves illustrate instantaneous conditions in discharging load capacitance during an output HIGH-to-LOW transmission. When the output voltage is at about 3.5V, for example, the circuit can absorb charge from the load capacitance at a 500 mA rate at +25°C. From this level the rate decreases steadily down to about 100 mA at 1.5V. In this region from 3.5V to 1.5V, part of the charge from the load capacitance is fed back through D8 (Figure 1-3) and Q2 to provide extra base current for Q3, boosting its current sinking capability and thus reducing the fall time. Below the 1.5V level, Q3 continues to discharge the load capacitance, but without extra base current from D8. At about 0.5V, the integral Schottky clamp diode from base to collector of Q3 starts conducting and prevents Q3 from going into deep saturation.



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FIGURE 1-10. Output LOW Characteristics—'F00'



TL/F/9592-11

FIGURE 1-11. Output LOW Characteristics—'F00'

## Output Characteristics (Continued)

On a greatly expanded scale, the output LOW characteristics of a gate are shown in Figure 1-11. With no load, the output voltage is about 0.1V, increasing with current on a slope of about 7.5 $\Omega$ . When the load current increases beyond the current-sinking capability of Q3, the output voltage rises steeply. It can be seen that the worst-case specification of 0.5V max at 20 mA load is easily met. Similar characteristics for a buffer shown in Figure 1-12, over a broader current range. The curves are well below the output LOW voltage specification of 0.55V max at 48 mA over the military temperature range or 64 mA over the commercial temperature range.

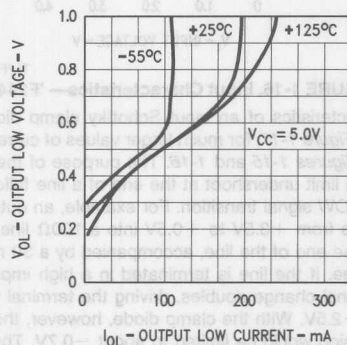


FIGURE 1-12. Output LOW Characteristics—'F244

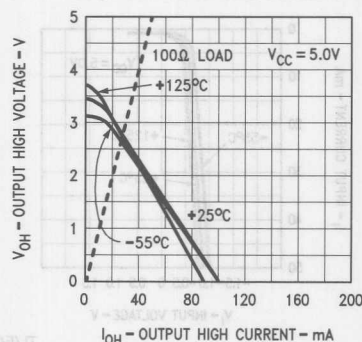


FIGURE 1-13. Output HIGH Characteristics—'F00

The output HIGH characteristics of a FAST gate are shown in Figure 1-13. At low values of output current the voltage is approximately 3.5V. This value is just the supply voltage minus the combined base-emitter voltages of the Darlington pull-up transistors Q5 and Q6 (Figure 1-3). For load currents above 16 mA or 18 mA, the voltage drop across the 45 $\Omega$  Darlington collector resistor becomes appreciable and the Darlington saturates. For greater load currents the output voltage decreases with a slope of about 50 $\Omega$ , which is largely due to the 45 $\Omega$  resistor. The value of current where a characteristic intersects the horizontal axis is the short-

circuit output current  $I_{OS}$ . This is guaranteed to be at least 60 mA for a FAST gate, compared to 40 mA for S-TTL. This parameter is an important indicator of the ability of an output to charge load capacitance. Thus the FAST specifications insure that an output can charge load capacitance faster, or force a higher LOW-to-HIGH voltage step into the dynamic impedance of a long interconnection.

The output HIGH characteristics of a buffer are shown in Figure 1-14. These are similar in shape to Figure 1-13 but at higher levels of current. The output HIGH voltage of a buffer is guaranteed at two different levels of load current. With a 3 mA load,  $V_{OH}$  is guaranteed to be at least 2.4V for both military and commercial devices.  $V_{OH}$  is also guaranteed to be at least 2.0V with a 12 mA load for military or 15 mA load for commercial devices. In addition, the short-circuit output current of a buffer is guaranteed to be at least 100 mA.

When an output is driving a long interconnection, the initial LOW-to-HIGH transition is somewhat less than the final, quiescent HIGH level because of the loading effect of the line impedance. The full HIGH voltage level is only reached after the reflection from the far end of the line returns to the driver. The initial LOW-to-HIGH voltage step that an output can force into a line is determined by drawing a load line on the graph containing the output HIGH characteristic and noting the voltage value where the load line intersects the characteristic. For example, if a FAST gate is driving a 100 $\Omega$  line, a straight line from the lower left origin up to the point 5V, 50 mA intersects the -55°C characteristic curve at about 2.8V. This indicates that the gate output voltage will rise to 2.8V initially, and the 2.8V signal, accompanied by 28 mA of current, will travel to the end of the line. If not terminated, the 28 mA is forced to return to the driver, whereupon it unloads the driver and the output voltage rises to the maximum value. Similarly, a 50 $\Omega$  load line drawn on the buffer characteristic shows an intercept voltage of 2.5V. In both cases, the initial voltage step is great enough to pass through the switching region of any inputs that might be located near the driver end of the line, and thus would not exhibit any exaggerated propagation delay due to the loading effect of the line impedance on the driver output. Thus the FAST output characteristics insure better system performance under adverse loading conditions.

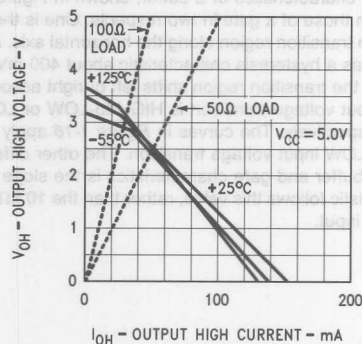


FIGURE 1-14. Output HIGH Characteristics—'F244

## Input Characteristics

The input of a FAST circuit represents a small capacitance, typically 4 pF to 5 pF, in parallel with an I-V characteristic that exhibits different slopes over different ranges of input voltage. Figure 1-15 shows the input characteristic of a FAST gate at three temperatures. In the upper right, the flat horizontal portion is the  $V_{IH}$ - $I_{IH}$  characteristic. In this region, all of the current from the 10 k $\Omega$  input resistor (Figure 1-3) is flowing into the base of Q1 and the only current flowing in the input diode is the leakage current  $I_{IH}$ . When the input voltage decreases to about 1.7V (+25°C), current starts to flow out of the input diode and the curve shows a knee. At this point some of the current from the 10 k $\Omega$  resistor is diverted from the base of Q1. When the input voltage declines to about 1.4V the curve shows another knee; at this point, substantially all of the current from the 10 k $\Omega$  resistor flows out of the input diode. The portion of the curve between 1.4V and 1.7V input voltage is the active region, essentially corresponding to the FAST transfer function in Figure 1-5.

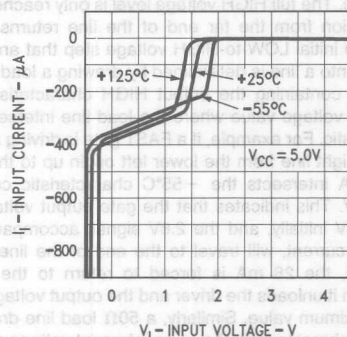


FIGURE 1-15. Input Characteristics—'F00

Below 1.4V input, the characteristic has the slope of the 10 k $\Omega$  input resistor. When the input voltage declines to about -0.3V, the Schottky clamping diode starts conducting and the current increases rapidly as the input voltage decreases further.

The input characteristics of a buffer, shown in Figure 1-16, differ from those of a gate in two respects. One is the location of the transition region along the horizontal axis. A buffer input has a hysteresis characteristic about 400 mV wide, such that the transition region shifts left or right accordingly as the input voltage transition is HIGH-to-LOW or LOW-to-HIGH, respectively. The curves in Figure 1-16 apply to the HIGH-to-LOW input voltage transition. The other difference between buffer and gate characteristics is the slope of the characteristic follows this value, rather than the 10 k $\Omega$  slope of a gate input.

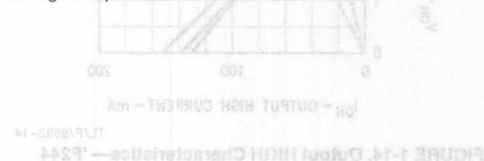


FIGURE 1-14. Output HIGH Characteristics—'F244

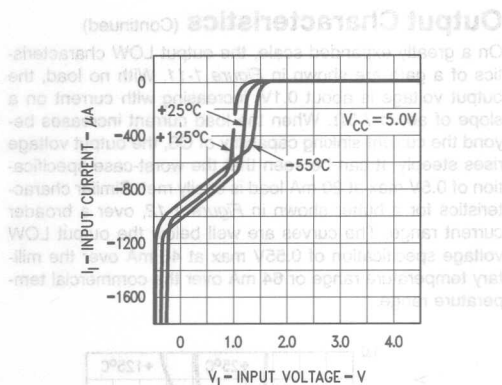


FIGURE 1-16. Input Characteristics—'F244

The characteristics of an input Schottky clamp diode are shown in Figure 1-17, for much larger values of current than those of Figures 1-15 and 1-16. The purpose of the clamp diode is to limit undershoot at the end of a line following a HIGH-to-LOW signal transition. For example, an output signal change from +3.5V to +0.5V into a 100 $\Omega$  line propagates to the end of the line, accompanied by a 30 mA current change. If the line is terminated in a high impedance the 3V signal change doubles, driving the terminal voltage down to -2.5V. With the clamp diode, however, the negative excursion would be limited to about -0.7V. The same HIGH-to-LOW signal change on a 50 $\Omega$  line would be clamped at about -1.0V. Figure 1-18 shows the typical breakdown characteristics for a FAST input.

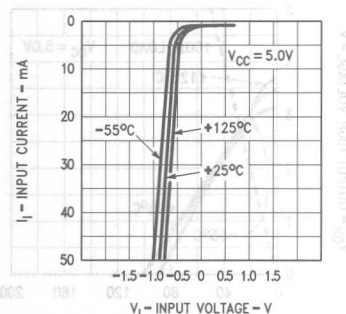


FIGURE 1-17. Input Characteristics—'F00 or 'F244

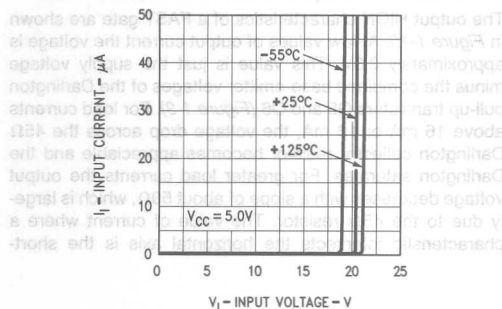


FIGURE 1-18. Input Characteristics—'F00 or 'F244

## TRI-STATE® Outputs

A partial schematic of a circuit having a TRI-STATE output is shown in Figure 1-19. When the internal Output Enable (OE) signal is HIGH, the circuit operates in the normal fashion to provide HIGH or LOW output drive characteristics. When OE is LOW, however, the bases of Q1, Q2 and Q5 are pulled down. In this condition the output is a high imped-

ance. In this High Z condition, the output leakage is guaranteed not to exceed 50  $\mu\text{A}$ . In the case of a transceiver, each data pin is an input as well as an output and the leakage specification is increased to 70  $\mu\text{A}$ . In the High Z state, output capacitance averages about 5 pF for a 20 mA output and about 12 pF for a 64 mA output.

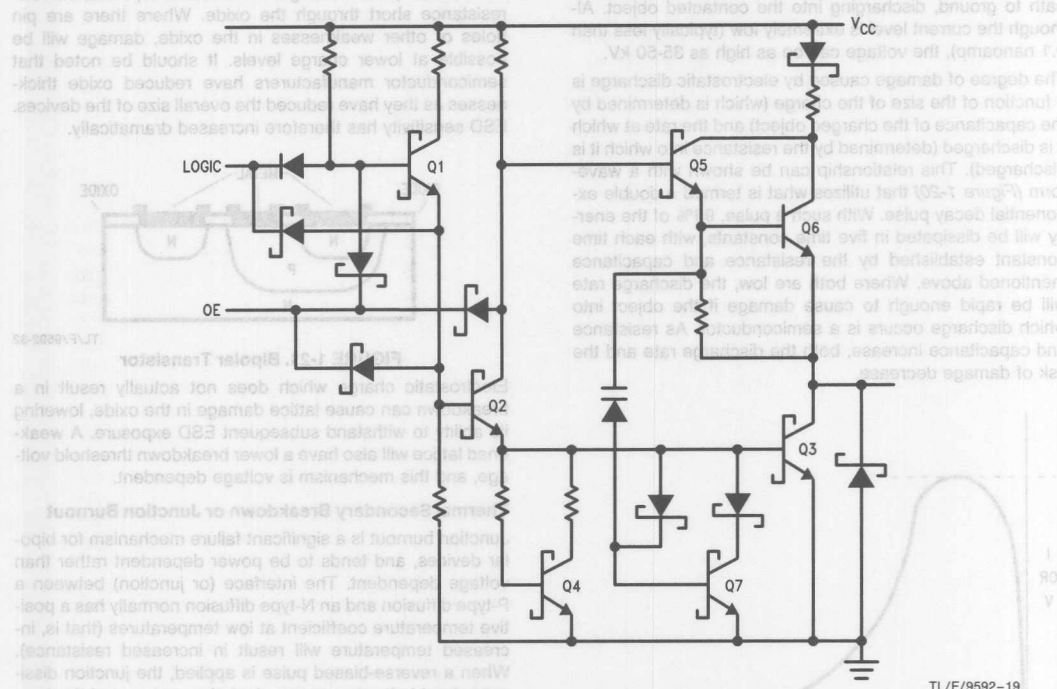


FIGURE 1-19. Typical TRI-STATE Input Control

## FAST ESD Protection

### INTRODUCTION

The study of ESD failures began in earnest back when system designers, faced with very expensive assembly and post-assembly rework, began investigating system failures in great detail. In the course of their study, they checked all the records to determine which devices had passed earlier testing, but had failed once in the system. The data clearly indicated that something in the handling process resulted in higher attrition rates among the devices. Reliability physicists examined the failed devices in minute detail, in some cases subjecting them to examination under high powered scanning electron microscopes.

The problem was found to be one of electrical overstress, and further investigation determined that the cause of the overstress was a phenomenon called electrostatic discharge (or ESD).

### EXPLANATION OF HOW ESD OCCURS

The concept of electrostatic discharge is easily understood. Electrostatic energy is static electricity, a stationary charge which can build up in either a nonconductive material or in an ungrounded conductive material. This charge can occur

in one of two ways, either through polarization, which occurs when a conductive material is exposed to a magnetic field, or triboelectric effects, which occur when two surfaces contact and then separate, leaving one positively charged and one negatively charged. Friction between two materials increases triboelectric charge by increasing the surface area that comes in contact. A good example of this phenomenon would be the charge one accumulates walking across a nylon carpet. The discharge occurs when one reaches for a doorknob or other conductive surface. The types of ESD with which we will be concerned fall into the category of triboelectric effects. Within this category, various materials have differing potentials for charge. Asbestos, nylon, human and animal hair and wool have a high positive triboelectric potential. Silicon has one of the highest negative triboelectric potentials, followed by such materials as polyurethane, polyester and rayon. Cotton, wood, steel and paper all tend to be relatively neutral, which makes cotton clothing and steel table tops excellent ESD protective materials in environments where ESD problems can be anticipated.



10%RH. When an object storing a static charge comes in contact with another object, the charge will attempt to find a path to ground, discharging into the contacted object. Although the current level is extremely low (typically less than 0.1 nanoamp), the voltage can be as high as 35-50 kV.

The degree of damage caused by electrostatic discharge is a function of the size of the charge (which is determined by the capacitance of the charged object) and the rate at which it is discharged (determined by the resistance into which it is discharged). This relationship can be shown with a waveform (Figure 1-20) that utilizes what is termed a double exponential decay pulse. With such a pulse, 99% of the energy will be dissipated in five time constants, with each time constant established by the resistance and capacitance mentioned above. Where both are low, the discharge rate will be rapid enough to cause damage if the object into which discharge occurs is a semiconductor. As resistance and capacitance increase, both the discharge rate and the risk of damage decrease.

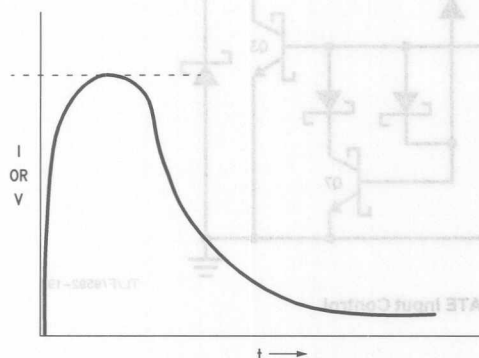


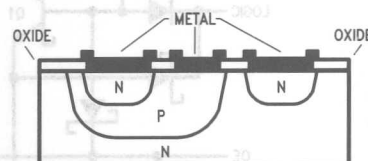
FIGURE 1-20. Ideal RC Waveform

It is estimated that the value of devices lost to ESD could run as high as \$1 billion per year. Most electrostatic damage is caused by the handling of devices by personnel who have not taken adequate precautions. One would expect this in light of the fact that the capacitance of the human body ranges from 50 to 200 pF. The ESD characteristics of work surfaces and of materials passing through the area should not be ignored, however, in an attempt to concentrate on the human effect.

#### TYPES OF ESD DAMAGE

The damage caused by ESD results from the charge's tendency to seek the shortest path to ground, overstressing any electrical interfaces in that path. There are several different types of damage that result, and each of these tends to be typical of specific component technologies and elements.

most important factor in this breakdown is the oxide thickness (Figure 1-21). Thinner oxide is more susceptible to electrostatic punch-through, which leaves a permanent low-resistance short through the oxide. Where there are pin holes or other weaknesses in the oxide, damage will be possible at lower charge levels. It should be noted that semiconductor manufacturers have reduced oxide thicknesses as they have reduced the overall size of the devices. ESD sensitivity has therefore increased dramatically.



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FIGURE 1-21. Bipolar Transistor

Electrostatic charge which does not actually result in a breakdown can cause lattice damage in the oxide, lowering its ability to withstand subsequent ESD exposure. A weakened lattice will also have a lower breakdown threshold voltage, and this mechanism is voltage dependent.

#### Thermal Secondary Breakdown or Junction Burnout

Junction burnout is a significant failure mechanism for bipolar devices, and tends to be power dependent rather than voltage dependent. The interface (or junction) between a P-type diffusion and an N-type diffusion normally has a positive temperature coefficient at low temperatures (that is, increased temperature will result in increased resistance). When a reverse-biased pulse is applied, the junction dissipates heat in its very narrow depletion region, and the temperature increases rapidly. If enough energy is applied, the temperature of the junction will reach a point at which the temperature coefficient of the silicon will turn negative (that is, at which increased temperature will result in **decreased** resistance). Since the area of the junction is not uniform, hot spots occur. When the melting temperature of silicon (1415°C) is reached as a result of the ensuing thermal runaway condition, junction melting occurs in the localized area. If there is an additional energy available after the initiation of melt, the hot spot can grow into a filament short. The longer the pulse, the wider the resultant filament short.

After the occurrence of the transient, the silicon will resolidify. In a relatively short pulse, a hot spot may form, but not grow completely across the junction. As a result, the damage may not manifest itself immediately as a junction short but will appear at a later time as a result of electromigration. Shrinking geometries will decrease junction areas, and this should increase the susceptibility of these devices to ESD related junction problems.



ility. As feature sizes continue to be reduced, metallization cross-section will be reduced as well. Reducing metallization line width by half and metallization thickness by half reduces the current carrying capability of that metallization stripe by 75%. Metallization melt, which is a power-dependent failure mechanism, is more likely to occur during short duration, high current pulses, since the only available heat sink (the bonding pad) is nearby and the heat dissipated in the metallization does not have time to flow into the surrounding areas. It can also occur as a side effect during junction melt.

#### Latent Failures

Immediate failure resulting from ESD exposure is easily determined: the device no longer works. A failed device may be removed from the lot or from the subassembly in which it is installed, and it represents no further reliability risk to the system. There are, however, devices which have been exposed to ESD but which have not immediately failed. Unfortunately, there has never been sufficient data dealing with the long-term reliability of devices which have survived ESD exposure, although some experts feel that two to five devices are degraded for every one that fails. It should be obvious from an examination of the failure mechanisms described above that there can be significant degradation without immediate failure. Damage can manifest itself in either a shortening of the device's lifetime (a possible cause for many of the infant mortality failures seen during burn-in) or in electrical performance shifts, many of which cause the device to fail electrical test limits.

#### ESD PROTECTIVE MEASURES

It should be obvious then that there are three principal considerations when dealing with ESD. The first is that the device should be designed in a manner that minimizes ESD sensitivity and incorporates some ESD protective features.

understand the generation of and sources of ESD charges well enough to establish proper precautions throughout their plants.

#### Fast Dual-Rail ESD Protection

The continuing development of faster and more complex IC's makes it unlikely that we will see a return to thicker oxide layers and larger junctions. Early IC's used fairly simple clamping diodes on the inputs to protect them against voltage transients in the system. Similar, but more comprehensive protective networks can be employed to provide ESD protection. Figure 1-22 shows National's FAST proprietary dual-rail ESD protection circuitry. These structures are included on most of the high volume FAST products and are now standard on all new FAST designs and redesigns. (See individual product specifications for identification of parts with enhanced ESD protection.) By its design, this form of ESD control limits product vulnerability to both positive and negative ESD/EOS voltages by protecting inputs and output to  $V_{CC}$  as well as ground.

Protection to ground is provided through transistor Q2 on the input and diode D2 on the output. On the input, the unique design and layout of the Schottky device insures a minimum turn-on voltage as well as maximum current carrying capability. For the output the standard Schottky clamp diode provides the protection. Q1 and Q3, through use of a BVCEO breakdown mechanism, protects the path to  $V_{CC}$ . Diode D1 and D3 insure isolation of the input or output from  $V_{CC}$  leakages. Again, these devices have been designed and laid-out to insure dependable turn-on characteristics as well as robustness.

Dual-rail ESD protection has provided FAST parts with protection levels exceeding 4000V. In fact, as measured through use of the MIL-STD-883 techniques described below, FAST ESD protection has averaged in excess of 8000V. Best of all, this protection has been achieved with no appreciable effect on speed or significant increase in input capacitance.

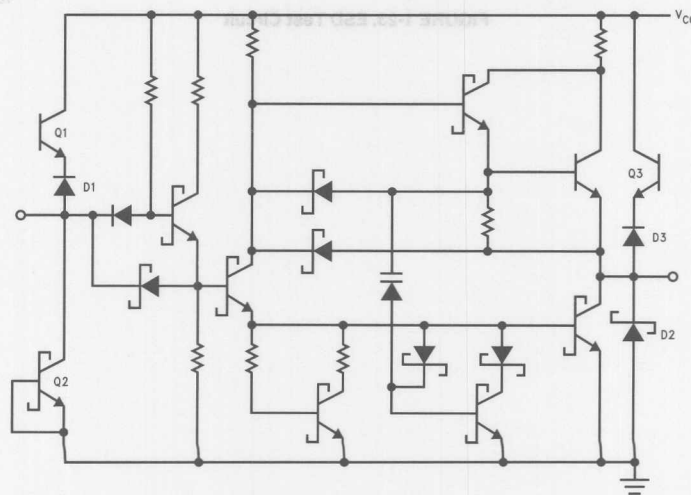


FIGURE 1-22. FAST ESD Circuitry

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## FAST ESD Protection (Continued)

### Assessing ESD Tolerance Levels

As awareness of the importance of addressing ESD concerns spread, many experts felt that ESD testing had to be uniform if results were to be shared. Method 3015 of MIL-STD-883 was created for the purpose of allowing manufacturers to assess the ESD tolerance levels of the devices they offered and to allow users to determine the ESD sensitivity of the parts with which they were assembling systems. Method 3015 has established a test circuit (see Figure 1-23) which approximates the resistance and capacitance found in the human body (which continues to provide the major source of destructive ESD). The testing is performed by charging the capacitor in the test circuit and then discharging that capacitor into the unit under test. After testing, a device will be classified as either Class 1, those devices which exhibit ESD-induced failure or degradation at levels between zero volts and 1,999V; or Class 2, those which may exhibit ESD sensitivity at levels between 2,000V and 3,999V; or Class 3, those devices which may exhibit ESD sensitivity at levels above 4,000V but have passed all testing up to that level. This testing is performed on a sample basis at initial device qualification and need not be repeated unless the device is redesigned. The testing is considered destructive, even for those devices which do not fail.

A device may be characterized as Class 1 in lieu of testing at a manufacturer's discretion. Some manufacturers, concerned with the possibility of latent damage due to inadequate protection of devices which test as Class 2, and concerned that static charges resulting from handling can run as high as 50 kV, have elected to treat all of their devices as Class 1, thus ensuring that consistent implementation of common handling procedures will provide maximum protection for all devices.

Data generated by an RADC study of electrostatic discharge susceptibility (VZAP-1, Spring 1983) would seem to support that kind of a conservative approach. The data (see Figure 1-24) shows the point at which failure first occurred for a given device. It indicates that there are a number of devices which can be expected to fail between 2 kV and 5 kV, but few that will survive beyond 10 kV.

Those devices which are classified as Class 1 must be marked with one equilateral triangle, and those classified as Class 2 must be marked with two equilateral triangles to identify them as static sensitive. (Class 3 devices will have no top mark designator.)

TABLE I. Device ESD Failure Threshold Classification

MIL Class	ESD Tolerance	Top Mark Designation
Class 1	0V to 1,999V	One triangle (i.e., ▲)
Class 2	2,000V to 3,995V	Two triangles (i.e., ▲▲)
Class 3	4,000V and above	No mark

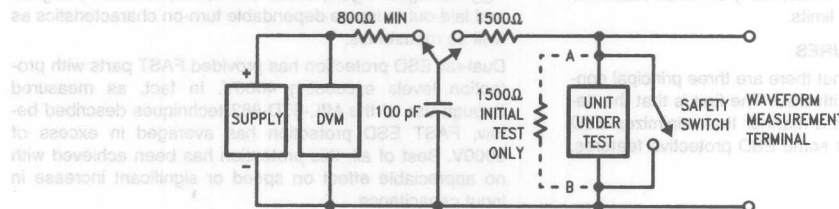


FIGURE 1-23. ESD Test Circuit

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## FAST ESD Protection (Continued)

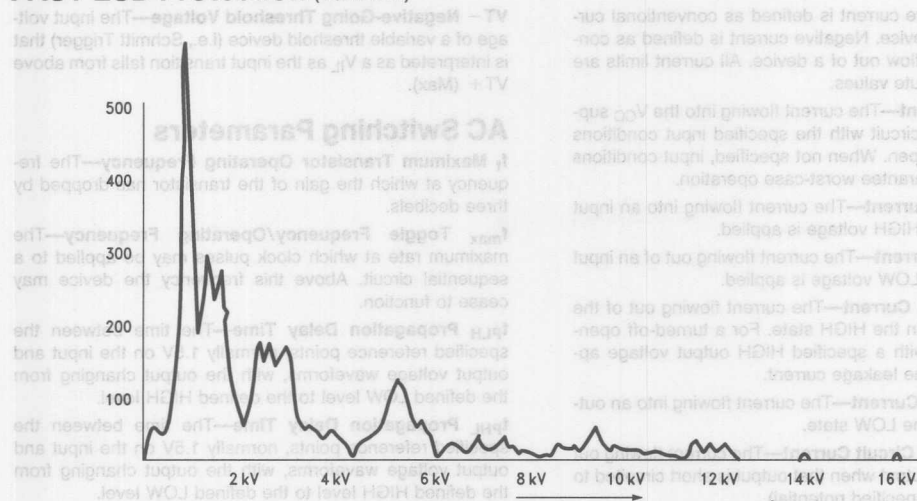


FIGURE 1-24. Failure Rate at Ascending ESD Voltages

## ESD Precautionary Measures

ESD protective measures fall into two categories: those which shield the device from ESD and those which control the occurrence of ESD. ESD shielding can be accomplished by either grounding all of the device leads together, thus providing a more direct path to ground, or by surrounding the device with insulating material that would keep ESD from reaching the device. The first method is most practical during device assembly and environmental test, the second during shipment and storage. However, neither can be utilized during electrical testing.

Most of the handling of ICs, however, occurs during electrical testing. Testing cannot be performed if the device's leads are shorted together, nor can it take place if the device is within an insulated container. Control of ESD during testing is therefore extremely important. This is accomplished through the grounding of all potential sources of ESD. Stainless steel work surfaces connected to ground through an appropriate resistive element provide a harmless bleed-off of any charge that occurs. Requiring that all personnel who handle devices wear ground straps can effectively eliminate the human body and its clothing as sources of ESD. It is also important to minimize the handling of devices. This can be partially accomplished through the use of automated test handlers, which allow the devices to be loaded into the testers from ESD-protective rails and returned to those rails from the tester. Equally important is the

elimination of any unnecessary testing or test insertions. Semiconductor manufacturers have decreased the number of test insertions for many devices by combining parametric, functional and switching tests onto a single insertion test program. Users have minimized handling by relying more heavily on the testing performed by their vendors and by eliminating incoming testing. Pick-and-place systems and other automated board assembly hardware have also helped to minimize device handling. Most systems manufacturers have also implemented procedures that minimize the handling of boards and subassemblies in order to ensure that devices receive no potentially damaging exposure to ESD after board assembly.

Effective control of ESD, however, cannot be accomplished unless the entire work area is designed around ESD concerns. This level of attention to detail is essential to the minimization of ESD problems.

## SUMMARY

Electrostatic discharge will continue to be a major concern for those who use semiconductor devices. As device geometries continue to shrink, the ESD sensitivity of devices will increase. Only through proper handling and packaging, and through proper attention to ESD concerns will we be able to ensure that long term reliability of key systems is not negatively affected by ESD problems.

## Glossary

**Currents**—Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

**$I_{CC}$  Supply Current**—The current flowing into the  $V_{CC}$  supply terminal of a circuit with the specified input conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst-case operation.

**$I_{IH}$  Input HIGH Current**—The current flowing into an input when a specified HIGH voltage is applied.

**$I_{IL}$  Input LOW Current**—The current flowing out of an input when a specified LOW voltage is applied.

**$I_{OH}$  Output HIGH Current**—The current flowing out of the output when it is in the HIGH state. For a turned-off open-collector output with a specified HIGH output voltage applied, the  $I_{OH}$  is the leakage current.

**$I_{OL}$  Output LOW Current**—The current flowing into an output when it is in the LOW state.

**$I_{OS}$  Output Short Circuit Current**—The current flowing out of a HIGH-state output when that output is short circuited to ground (or other specified potential).

**$I_{OZH}$  Output OFF Current HIGH**—The current flowing into a disabled TRI-STATE output with a specified HIGH output voltage applied.

**$I_{OZL}$  Output OFF Current LOW**—The current flowing out of a disabled TRI-STATE output with a specified LOW output voltage applied.

**Voltages**—All voltages are referenced to the ground pin. Negative voltage limits are specified as absolute values (i.e.,  $-10.0V$  is greater than  $-1.0V$ ).

**$V_{CC}$  Supply Voltage**—The range of power supply voltage over which the device is guaranteed to operate within the specified limits.

**$V_{CD}(\text{Max})$  Input Clamp Diode Voltage**—The most negative voltage at an input when a specified current is forced out of that input terminal. This parameter guarantees the integrity of the input diode, intended to clamp negative ringing at the input terminal.

**$V_{IH}$  Input HIGH Voltage**—The range of input voltages that represents a logic HIGH in the system.

**$V_{IH}(\text{Min})$  Minimum Input HIGH Voltage**—The minimum allowed input HIGH in a logic system. This value represents the guaranteed input HIGH threshold for the device.

**$V_{IL}$  Input LOW Voltage**—The range of input voltages that represent a logic LOW in the system.

**$V_{IL}(\text{Max})$  Maximum Input LOW Voltage**—The maximum allowed input LOW in a system. This value represents the guaranteed input LOW threshold for the device.

**$V_{OH}(\text{Min})$  Output HIGH Voltage**—The minimum voltage at an output terminal for the specified output current  $I_{OH}$  and at the minimum value of  $V_{CC}$ .

**$V_{OL}(\text{Max})$  Output LOW Voltage**—The maximum voltage at an output terminal sinking the maximum specified load current  $I_{OL}$ .

**$V_T+$  Positive-Going Threshold Voltage**—The input voltage of a variable threshold device (i.e., Schmitt Trigger) that is interpreted as a  $V_{IH}$  as the input transition rises from below  $V_T-$  (Min).

**$V_T-$  Negative-Going Threshold Voltage**—The input voltage of a variable threshold device (i.e., Schmitt Trigger) that is interpreted as a  $V_{IL}$  as the input transition falls from above  $V_T+$  (Max).

## AC Switching Parameters

**$f_t$  Maximum Transistor Operating Frequency**—The frequency at which the gain of the transistor has dropped by three decibels.

**$f_{max}$  Toggle Frequency/Operating Frequency**—The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

**$t_{PLH}$  Propagation Delay Time**—The time between the specified reference points, normally 1.5V on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

**$t_{PHL}$  Propagation Delay Time**—The time between the specified reference points, normally 1.5V on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.

**$t_w$  Pulse Width**—The time between 1.5V amplitude points on the leading and trailing edges of a pulse.

**$t_h$  Hold Time**—The interval immediately following the active transition of the timing pulse (usually the clock pulse) of following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

**$t_s$  Setup Time**—The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

**$t_{PHZ}$  Output Disable Time (of a TRI-STATE Output) from HIGH Level**—The time between the 1.5V level on the input and a voltage 0.3V below the steady state output HIGH level with the TRI-STATE output changing from the defined HIGH level to a high impedance (OFF) state.

**$t_{PLZ}$  Output Disable Time (of a TRI-STATE Output) from LOW Level**—The time between the 1.5V level on the input and a voltage 0.3V above the steady state output LOW level with the TRI-STATE output changing from the defined LOW level to a high impedance (OFF) state.

**$t_{PZH}$  Output Enable Time (of a TRI-STATE Output) to a HIGH Level**—The time between the 1.5V levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a HIGH level.

**$t_{PZL}$  Output Enable Time (of a TRI-STATE Output) to a LOW Level**—The time between the 1.5V levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a LOW level.

**$t_{rec}$  Recovery Time**—The time between the 1.5V level on the trailing edge of an asynchronous input control pulse and the same level on a synchronous input (clock) pulse such that the device will respond to the synchronous input.

## Logic Symbols and Terminology

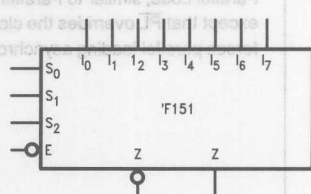
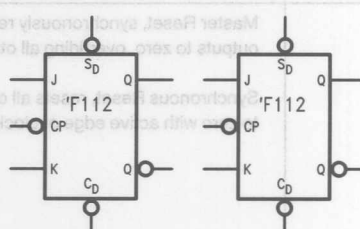
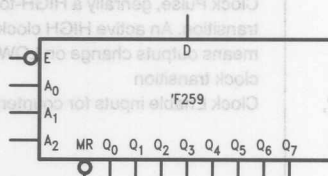
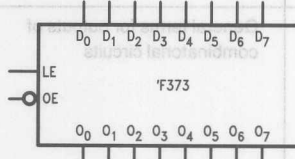
The definitions of LOW and HIGH logic levels are: LOW- a voltage defined by  $V_{IL}$ ; HIGH- a voltage defined by  $V_{IH}$ . A LOW condition represents logic '0'; a HIGH condition, logic '1'.

The logic symbols used to represent the FAST devices follow MIL-STD-806B for logic symbols. Elements are represented by rectangular blocks with appropriate external AND/OR gates when necessary. A small circle at an external input means that the specific input is active-LOW; (it produces the desired function, in conjunction with other inputs, if its voltage is the lower of the two logic levels in the system). A circle at the output indicates that when the func-

tion designated is true, the output is LOW. Generally, inputs are at the top and left and outputs appear at the bottom and right of the logic symbol. An exception is the asynchronous Master Reset in some sequential circuits which is always at the left hand bottom corner.

Inputs and outputs are labeled with mnemonic letters as illustrated in Table 1-1. Note that an active LOW function labeled outside of the logic symbol is given a bar over the label, while the same function inside the symbol is labeled without the bar. When several inputs or outputs use the same letter, subscript numbers starting with zero are used in an order natural for device operation.

TABLE 1-1

Label	Meaning	Example
I <sub>x</sub>	General term for inputs to combinatorial circuits.	 TL/F/9592-20
J, K S, R D	Inputs to JK, SR and D flip-flops and latches.	 TL/F/9592-21
A <sub>x</sub> , S <sub>x</sub>	Address or Select inputs, used to select an input, output, data route, junction, or memory location.	 TL/F/9592-22
LE	Enable, active LOW on all TTL/MSI. A latch can receive new data when its Enable input is in the active state.	 TL/F/9592-23

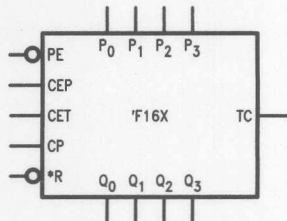
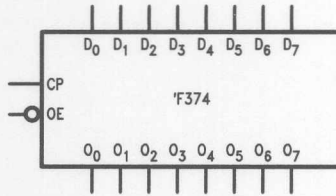


Label	Meaning	Example	
PE	Parallel Enable, a control input used to synchronously load information in parallel into an otherwise autonomous circuit.		TL/F/9592-24
PL	Parallel Load; similar to Parallel Enable except that PL overrides the clock and forces parallel loading asynchronously.		TL/F/9592-25
MR	Master Reset, synchronously resets all outputs to zero, overriding all other inputs.		TL/F/9592-26
SR	Synchronous Reset, resets all outputs to zero with active edge of clock.		TL/F/9592-27
CP	Clock Pulse, generally a HIGH-to-LOW-to-HIGH transition. An active HIGH clock (no circle) means outputs change on LOW-to-HIGH clock transition		TL/F/9592-28
CE, CEP, CET	Clock Enable inputs for counters.		
Zx, Ox, Fx	General terms for outputs of combinatorial circuits		



## Logic Symbols and Terminology (Continued)

TABLE 1-1 (Continued)

Label	Meaning	Example
Q <sub>x</sub>	General term for latch and flip-flop outputs. If they pass through an enable gate before exiting the package, Q or $\bar{Q}$ changes to O or $\bar{O}$ .	 <p>Diagram of a 4-bit counter (F16X) showing inputs PE, CEP, CET, CP, *R and outputs P<sub>0</sub>, P<sub>1</sub>, P<sub>2</sub>, P<sub>3</sub>, Q<sub>0</sub>, Q<sub>1</sub>, Q<sub>2</sub>, Q<sub>3</sub>, and TC.</p>
TC	Terminal Count output (1111 for up binary counters, 1001 for up decimal counters, or 0000 for down counters).	TL/F/9592-29
$\bar{O}E$	Output Enable, used to force TRI-STATE outputs into the high impedance state.	 <p>Diagram of an 8-bit counter (F374) showing inputs CP, OE and outputs D<sub>0</sub>, D<sub>1</sub>, D<sub>2</sub>, D<sub>3</sub>, D<sub>4</sub>, D<sub>5</sub>, D<sub>6</sub>, D<sub>7</sub>, Q<sub>0</sub>, Q<sub>1</sub>, Q<sub>2</sub>, Q<sub>3</sub>, Q<sub>4</sub>, Q<sub>5</sub>, Q<sub>6</sub>, Q<sub>7</sub>.</p>
		TL/F/9592-30

This nomenclature is used throughout this book and may differ from nomenclature used on other data books, where outputs use alphabetic subscripts or use number sequences starting with one.

### Handling Precautions for Semiconductor Components

The following standard handling precautions should be observed for oxide isolation, shallow junction processed parts, such as FAST or 100k ECL:

1. All National devices are shipped in conducting foam or antistatic tubes. When they are removed for inspection or assembly, proper precautions should be used.

2. National devices, after removal from their shipping material, should be placed leads down on a grounded surface. Under no circumstances should they be placed in polystyrene foam or non-conducting plastic trays used for shipment and handling of conventional ICs.
3. Individuals and tools should be grounded before coming in contact with these devices.
4. Do not insert or remove devices in sockets with power applied. Ensure that power supply transients, such as occur during power turn-on or off, do not exceed maximum ratings.
5. After assembly on PC boards, ensure that static discharge cannot occur during handling, storage or maintenance. Boards may be stored with their connectors surrounded with conductive foam.





Section 2 Contents

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2-4	AC Loading and Waveforms
2-8	Absolute Maximum Ratings
2-8	Recommended Operating Conditions
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## Section 2

### Ratings, Specifications, and Waveforms



## Section 2 Contents

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Section 2  
Ratings, Specifications,  
and Waveforms

## Ratings, Specifications and Waveforms

For convenience in system design, the input loading and fan-out characteristics of each circuit are specified in terms of unit loads.

One unit load in the HIGH state is defined as 20  $\mu$ A; thus both the input HIGH leakage current,  $I_{IH}$ , and the output HIGH current-sourcing capability,  $I_{OH}$ , are normalized to 20  $\mu$ A. The specified  $I_{IH}$  for a typical FAST® single load input is 20  $\mu$ A or 1.0 U.L. The  $I_{OH}$  rating for a FAST output depends upon whether the device has a standard or TRI-STATE® output or if the device is a buffer/line driver. The  $I_{OH}$  rating for a standard FAST device is 1.0 mA or 50 U.L., while TRI-STATE is 3.0 mA or 150 U.L. and line driver/buffers specify  $I_{OH}$  of 12.0 mA or 600 U.L.

Similarly, one unit load in the LOW state is defined as 0.6 mA and both the input LOW current,  $I_{IL}$ , and the output LOW current-sinking capability,  $I_{OL}$ , are normalized to 0.6 mA. The specified maximum  $I_{IL}$  for a typical FAST single load input is 0.6 mA or 1.0 U.L. However, the  $I_{OL}$  rating differs among standard, TRI-STATE and buffer/line driver outputs. The  $I_{OL}$  rating for a standard output is 20 mA or 33.3 U.L. FAST devices with TRI-STATE outputs specify  $I_{OL}$  at 24 mA or 40 U.L. for commercial temperature range and 20 mA or 33.3 U.L. for military temperature range. The  $I_{OH}$  rating for a FAST buffer/line driver output is 64 mA or 106.6 U.L. for the commercial temperature range and 48 mA or 80 U.L. over the military temperature range.

On the data sheets the input and output load factors are listed in the Input Loading/Fan-Out table. The tables from

the 54F/74F373 Transparent Latch and the 29F52 Registered Transceiver are reproduced below.

In the second column from the right, the 54F/74F373 input HIGH/LOW load factors are 1.0/1.0 with the first number representing  $I_{IH}$  and the second representing  $I_{IL}$ . The 29F52 has input HIGH/LOW load factors of 1.0/1.0 for the typical FAST single load inputs and 3.5/1.083 for the register inputs. For testing procurement purposes, these unit load specifications can easily be translated into actual test limits by multiplying the HIGH/LOW load factors by 20  $\mu$ A and 0.6 mA respectively. The current limits are listed as well.

Also in this column are the output HIGH/LOW output load factors, with the first number representing  $I_{OH}$  and the second representing  $I_{OL}$ . These load factors can be translated to actual test limits by multiplying them by 20  $\mu$ A and 0.6 mA respectively. These are shown in the far right column. The 54F/74F373 output HIGH/LOW drive factors are 150/40 (33.3) which translate into an  $I_{OH}$  of 3.0 mA and  $I_{OL}$  of 24 mA for commercial grade and 20 mA for military grade. The 29F52 A-Register outputs are TRI-STATE outputs with HIGH/LOW drive factors of 150/40 (33.3) indicating an  $I_{OH}$  of 3 mA and  $I_{OL}$  of 24 mA for commercial and 20 mA for military. The B-Register outputs specify unit load factors of 600/106.6 (80) translating into an  $I_{OH}$  of 12 mA and  $I_{OL}$  of 64 mA for commercial and 48 mA for military.

### Unit Loading/Fan Out 29F52: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
A <sub>0</sub> -A <sub>7</sub>	A-Register Inputs	3.5/1.083	70 $\mu$ A/0.65 mA
	A-Register Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)
B <sub>0</sub> -B <sub>7</sub>	B-Register Inputs	3.5/1.083	70 $\mu$ A/0.65 mA
	B-Register Outputs	600/106.6 (80)	-12 mA/64 mA (48 mA)
OE <sub>A</sub>	Output Enable A-Register	1.0/1.0	20 $\mu$ A/-0.6 mA
CP <sub>A</sub>	A-Register Clock	1.0/1.0	20 $\mu$ A/-0.6 mA
CE <sub>A</sub>	A-Register Clock Enable	1.0/1.0	20 $\mu$ A/-0.6 mA
OE <sub>B</sub>	Output Enable B-Register	1.0/1.0	20 $\mu$ A/-0.6 mA
CP <sub>B</sub>	B-Register Clock	1.0/1.0	20 $\mu$ A/-0.6 mA
CE <sub>B</sub>	B-Register Clock Enable	1.0/1.0	20 $\mu$ A/-0.6 mA

**Unit Loading/Fan Out 54F/74F373:** See Section 2 for U.L. definitions

Pin Names	Description	29F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$D_0-D_7$	Data Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
LE	Latch Enable Input (Active HIGH)	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$O_0-O_7$	TRI-STATE Latch Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

**AC Loading and Waveforms**

Figure 2-1 shows the AC loading circuit used in characterizing and specifying propagation delays of all FAST devices, unless otherwise specified in the data sheet of a specific device. The use of this load, which differs somewhat from previous practice, provides more meaningful information and minimizes problems of instrumentation and customer correlation. In the past, +25°C propagation delays for TTL devices were specified with a load of 15 pF to ground; this required great care in building test jigs to minimize stray capacitance, and implied the use of high impedance, high frequency scope probes. FAST circuits changed to 50 pF of capacitance allowing more leeway in stray capacitance and also loading the device during rising or falling output transitions. This more closely resembles the loading to be expected in average applications and thus gives the designer more useful delay figures. The net effect of the change in AC load is to increase the observed propagation delay by an average of about 1 ns.

The 500 $\Omega$  resistor to ground, in Figure 2-1, acts as a ballast, to slightly load the totem-pole pull-up and limit the quiescent HIGH-state voltage to about +3.5V. Otherwise, an output would rise quickly to about +3.5V but then continue to rise very slowly to about +4.4V. On the subsequent HIGH-to-LOW transition the observed  $t_{PHL}$  would vary slightly with duty cycle, depending on how long the output voltage was allowed to rise before switching to the LOW state. Perhaps more importantly, the 500 $\Omega$  resistor to ground can be a high frequency passive probe for a sampling scope, which costs much less than the equivalent high impedance probe. Alternatively, the 500 $\Omega$  load to ground can simply be a 450 $\Omega$  resistor feeding into a 50 $\Omega$  coaxial cable leading to a sampling scope input connector, with the internal 50 $\Omega$  termination of the scope completing the path to ground. Note that with this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a 50 $\Omega$  termination for the pulse generator that supplies the input signal.

Also shown in Figure 2-1 is a second 500 $\Omega$  resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring a device with open-collector outputs and for measuring one set of the Enable/Disable parameters (LOW-to-OFF and OFF-to-LOW) of a TRI-STATE output. With the switch closed, the pair of 500 $\Omega$  resistors and the +7.0V supply establish a quiescent HIGH level of +3.5V, which correlates with the HIGH level discussed in the preceding paragraph.

Figure 2-5 shows that the Disable times are measured at the point where the output voltage has risen or fallen by 0.3V from the quiescent level (i.e., LOW for  $t_{PLZ}$  or HIGH for  $t_{PHZ}$ ), compared to a  $\Delta V$  of 0.5V used in previous practice. This change enhances the repeatability of measurements and gives the system designer more realistic delay times to

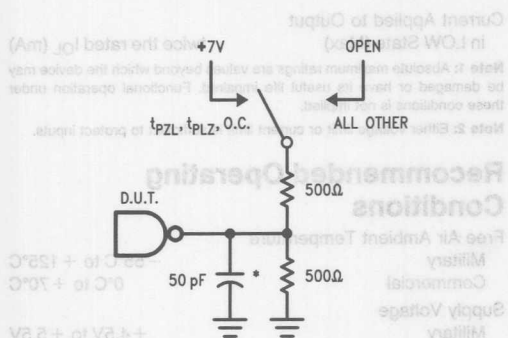
use in calculating minimum cycle times. Since the rising or falling waveform is RC-controlled, the first 0.3V of change is more linear than the first 0.5V and is less susceptible to external influences. More importantly, perhaps, from the system designer's point of view, a  $\Delta V$  of 0.3V is adequate to ensure that a device output has turned OFF; measuring to a  $\Delta V$  of 0.5V merely exaggerates the apparent Disable time and thus penalizes system performance, since the designer must use the Enable and Disable times to devise worst-case timing signals to ensure that the output of one device is disabled before that of another device is enabled.

Figure 2-2 describes the input signal voltages recommended for use when testing FAST circuits. The AC input signal levels follow industry convention of  $V_{IN}$  switching 0 to 3 volts. DC low input levels are typically 0 to  $V_{IL}$ , and high input levels are typically  $V_{IH}$  to  $V_{CC}$ . Input thresholds are guaranteed during  $V_{OL}$  and  $V_{OH}$  tests. High level noise immunity is the difference between  $V_{OH}$  and  $V_{IH}$ . Low level noise immunity is the difference between  $V_{IL}$  and  $V_{OL}$ . Noise-free  $V_{IH}$  or  $V_{IL}$  levels should not induce a switch on the appropriate output of the FAST device. When testing in an automatic test environment, extreme caution should be taken to ensure that input levels plus noise do not go into the transition region.

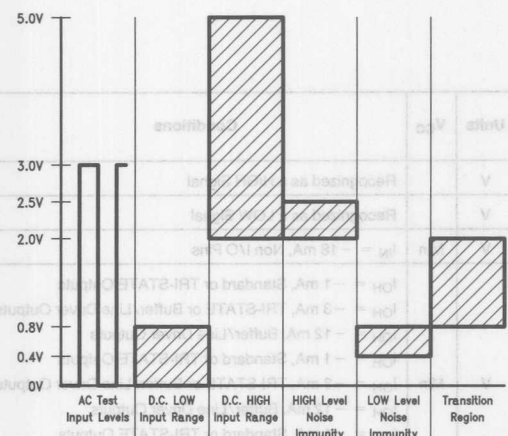
Good high frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A  $V_{CC}$  bypass capacitor should be provided at the test socket, also with minimum lead lengths. Input signals should have rise and fall times of 2.5 ns and signal swing of 0V to +3.0V. Rise and fall times  $\leq 1$  ns should be used for testing  $f_{max}$  or pulse width. A 1.0 MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing  $f_{max}$ . A 50% duty cycle should always be used when testing  $f_{max}$ . Two pulse generators are usually required for testing such parameters as setup time, hold time, recovery time, etc.

Precautions should be taken to prevent damage to devices by electrostatic charge. Static charge tends to accumulate on insulated surfaces, such as synthetic fabrics or carpeting, plastic sheets, trays, foam, tubes or bags, and on ungrounded electrical tools or appliances. The problem is much worse in a dry atmosphere. In general, it is recommended that individuals take the precaution of touching a known ground before handling devices. To effectively avoid electrostatic damage to FAST devices it may be necessary for individuals to wear a grounded wrist strap when handling devices.

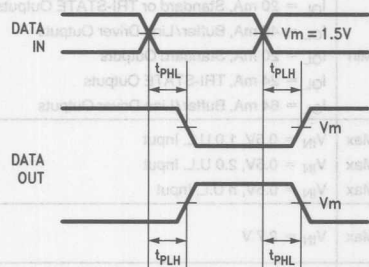




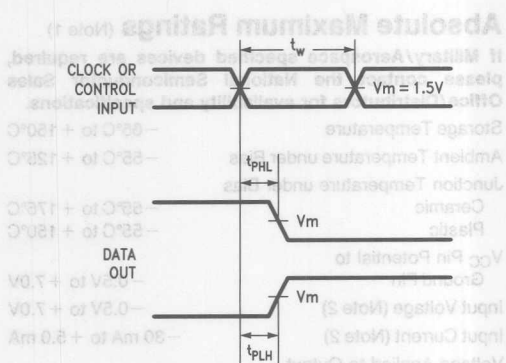
**FIGURE 2-1. Test Load**



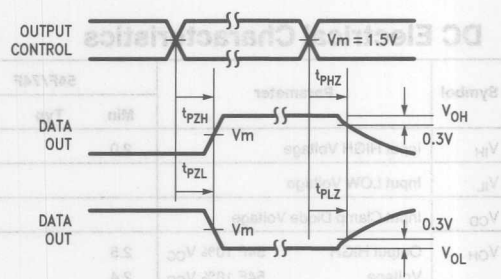
**FIGURE 2-2. Test Input Signal Levels**



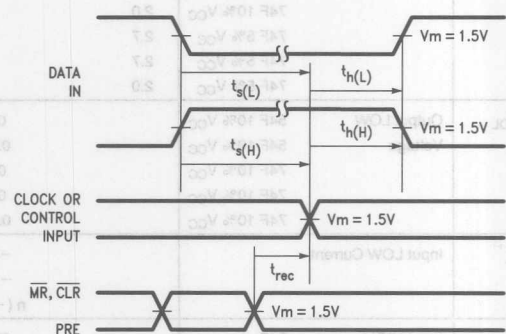
**FIGURE 2-3. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**



**FIGURE 2-4. Propagation Delay, Pulse Width Waveforms**



**FIGURE 2-5. TRI-STATE Output HIGH and LOW Enable and Disable Times**



**FIGURE 2-6. Setup Time, Hold Time and Recovery Time Waveforms**

**Office/Distributors for availability and specifications.**

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	
Ceramic	–55°C to +175°C
Plastic	–55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	–0.5V to V <sub>CC</sub>
Standard Output TRI-STATE Output	–0.5V to +5.5V

these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	–55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				–1.2	V	Min	I <sub>IN</sub> = –18 mA, Non I/O Pins
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5			V	Min	I <sub>OH</sub> = –1 mA, Standard or TRI-STATE Outputs
		54F 10% V <sub>CC</sub>	2.4					I <sub>OH</sub> = –3 mA, TRI-STATE or Buffer/Line Driver Outputs
		54F 10% V <sub>CC</sub>	2.0					I <sub>OH</sub> = –12 mA, Buffer/Line Driver Outputs
		74F 10% V <sub>CC</sub>	2.5					I <sub>OH</sub> = –1 mA, Standard or TRI-STATE Outputs
		74F 10% V <sub>CC</sub>	2.4					I <sub>OH</sub> = –3 mA, TRI-STATE or Buffer/Line Driver Outputs
		74F 10% V <sub>CC</sub>	2.0					I <sub>OH</sub> = –12 mA, Buffer/Line Driver Outputs
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = –1 mA, Standard or TRI-STATE Outputs
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = –3 mA, TRI-STATE or Buffer/Line Driver Outputs
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>			0.5	V	Min	I <sub>OL</sub> = 20 mA, Standard or TRI-STATE Outputs
		54F 10% V <sub>CC</sub>			0.55			I <sub>OL</sub> = 48 mA, Buffer/Line Driver Outputs
		74F 10% V <sub>CC</sub>			0.5			I <sub>OL</sub> = 20 mA, Standard Outputs
		74F 10% V <sub>CC</sub>			0.5			I <sub>OL</sub> = 24 mA, TRI-STATE Outputs
		74F 10% V <sub>CC</sub>			0.55			I <sub>OL</sub> = 64 mA, Buffer/Line Driver Outputs
I <sub>IL</sub>	Input LOW Current				–0.6	mA	Max	V <sub>IN</sub> = 0.5V, 1.0 U.L. Input
					–1.2	mA	Max	V <sub>IN</sub> = 0.5V, 2.0 U.L. Input
					n (–0.6)	mA	Max	V <sub>IN</sub> = 0.5V, n U.L. Input
I <sub>IH</sub>	Input HIGH Current	54F			20.0	μA	Max	V <sub>IN</sub> = 2.7 V
		74F			5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F			100	μA	Max	V <sub>IN</sub> = 7.0 V
		74F			7.0			
I <sub>BVIT</sub>	Input HIGH Current Breakdown (i/o)	54F			1.0	mA	Max	V <sub>IN</sub> = 5.5 V
		74F			0.5			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F			50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded

# DC Electrical Characteristics (Continued)

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
I <sub>OZH</sub>	Output Leakage Current		50		μA	Max	V <sub>OUT</sub> = 2.7V, TRI-STATE Outputs, Non I/O
I <sub>OZL</sub>	Output Leakage Current		−50		μA	Max	V <sub>OUT</sub> = 0.5V, TRI-STATE Outputs, Non I/O
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current		70		μA	Max	V <sub>I/O</sub> = 2.7V, I/O Pins
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current		−650		μA	Max	V <sub>I/O</sub> = 0.5V, I/O Pins
I <sub>OS</sub>	Output Short-Circuit Current	−60	−150		mA	Max	V <sub>OUT</sub> = 0V, Standard or TRI-STATE Outputs
		−100	−225		mA	Max	V <sub>OUT</sub> = 0V, Buffer/Line Driver Outputs
I <sub>ZZ</sub>	Bus Drainage Test		500		μA	0.0V	V <sub>OUT</sub> = 5.25V TRI-STATE Outputs
I <sub>OHC</sub>	Open Collector, Output OFF Leakage Test		250		μA	Min	V <sub>OUT</sub> = V <sub>CC</sub> , O.C. Outputs
I <sub>CCH</sub>	Power Supply Current				mA	Max	V <sub>OUT</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current				mA	Max	V <sub>OUT</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current				mA	Max	V <sub>OUT</sub> = HIGH Z





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## Section 3 Design Considerations

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Section 3  
Design Considerations

# FAST® Design Considerations

National Semiconductor  
Application Note 661



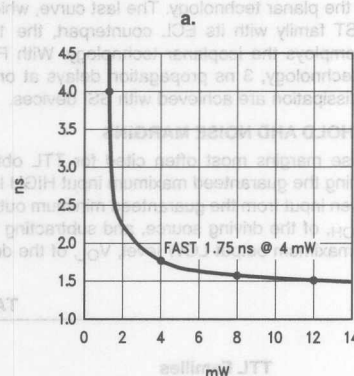
FAST® is a high-speed logic family that achieves speeds typically 30% faster than the Schottky family with a corresponding power reduction of approximately 75%. It is fabricated with an advanced oxide isolation technique, Isoplanar II, which produces transistors with very high, well-controlled switching speeds, extremely small parasitic capacitances and  $f_T$  in excess of 5 GHz.

Since the family is designed to be pin-compatible with other TTL families such as Schottky, Low Power Schottky and standard TTL, existing designs can be easily upgraded. FAST logic offers significant improvement over the Schottky family in addition to improved speed and power specifications. Other key advantages are higher input threshold levels (improving noise margins), reduced input loading, and increased output drive. The FAST family contains a full complement of circuits for more efficient design capabilities: small scale integration, medium scale integration and large scale integration.

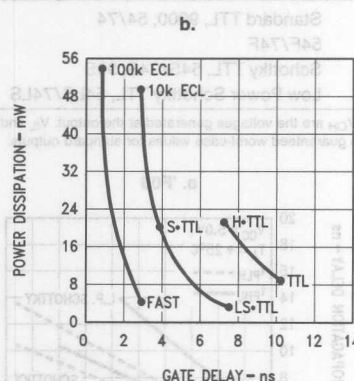
Fairchild engineers had some specific design objectives in mind when they developed the FAST logic family. The primary objective was the improvement of the circuit speed-power performance versus earlier TTL families. Another important objective was increasing threshold levels to improve DC noise immunity. Other goals were maintaining or improving the output drive of Schottky for improved line driving capability, and reducing input loading for increasing the overall fanout of the family. Output and input voltage levels, functions and pinouts were standardized to previous TTL families to maintain compatibility.

The primary design consideration was to improve speed while reducing power. The speed of any device is limited by the charge storage of the transistors. The time required to remove this charge is proportional to the capacitance and current available. Thus, to improve the speed, either the internal resistor values must be lowered to increase the available current and therefore remove the charge faster, such as in the Schottky family, or the capacitance must be reduced.

The speed-power curve shown in Figure 3-1a was used empirically to determine the optimum operating power level for the FAST family. Several internal gates programmed at a variety of power levels were produced on a wafer and the propagation delay of an internal gate for each power level was measured.



TL/F/9607-1



TL/F/9607-2

FIGURE 3-1. Speed-Power Product

As can be seen from the curves, power levels significantly below 4 mW per gate exhibit a dramatic degradation in performance. Power levels significantly above 4 mW, however, appear to have passed the point of diminishing returns with only minor improvements in propagation delay resulting from increased power. It was therefore concluded that the FAST family could be biased at 4 mW achieving a 1.75 ns propagation delay.



Figure 3-1b compares the FAST logic family with previous TTL and ECL logic families. Each curve groups families with similar technologies. The first line, known as "gold doped," groups together the 7400 and the 74H families into one technology grouping. These saturating logic families can be seen to have a relatively poor speed-power curve.

The second curve notes the Schottky, Low Power Schottky and 10k ECL families. They use non-gold doped, soft saturated (Baker clamped) or current steering logic in order to achieve their speed-power performance; however, they still employ the planar technology. The last curve, which shows the FAST family with its ECL counterpart, the 100k ECL family, employs the Isoplanar technology. With FAST Isoplanar technology, 3 ns propagation delays at only 4 mW power dissipation are achieved with SSI devices.

#### THRESHOLD AND NOISE MARGINS

The noise margins most often cited for TTL obtained by subtracting the guaranteed maximum input HIGH level,  $V_{IH}$ , of a driven input from the guaranteed minimum output HIGH level,  $V_{OH}$ , of the driving source, and subtracting the guaranteed maximum output LOW level,  $V_{OL}$ , of the driver from

the guaranteed minimum input LOW level,  $V_{IL}$ , of a driven circuit. The guaranteed worst-case values of these parameters vary slightly among the various circuit families and are summarized in Table III-I. Note that although the 9000 Series  $V_{IH}$  and  $V_{IL}$  specifications have different limits at different temperatures, they are grouped with the 54/74 family in the table as a matter of convenience. Note also that the  $V_{OL}$  limit listed for 74LS is 0.5V, whereas these circuits are also specified at 0.4V at a lower level of  $I_{OL}$ . Noise margins calculated in this manner are quite conservative, since it is assumed that both the driver output characteristics are worst-case and that  $V_{CC}$  is on the low side for the driver and on the high side for the receiver.

Figure 3-2 shows how load capacitance affects the propagation delay of Low Power Schottky, Schottky and FAST gates, flip-flops, registers and decoders, etc. As would be expected, Low Power Schottky TTL shows greater sensitivity since LS output drive capability is not as great as either Schottky or FAST. Significantly, FAST is less affected than Schottky by load capacity. Figure 3-2 shows propagation delay versus load capacitance for buffers and line drivers since they are designed for greater output drive.

TABLE III-I. Parameter Limits

TTL Families		Military (-55°C to +125°C)				Commercial (0°C to +70°C)				Units
		$V_{IL}$	$V_{IH}$	$V_{OL}$	$V_{OH}$	$V_{IL}$	$V_{IH}$	$V_{OL}$	$V_{OH}$	
TTL	Standard TTL, 9000, 54/74	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
FAST	54F/74F	0.8	2.0	0.5	2.4	0.8	2.0	0.5	2.5	V
S-TTL	Schottky TTL, 54S/74S, 93S	0.8	2.0	0.5	2.5	0.8	2.0	0.5	2.7	V
LS-TTL	Low Power Schottky TTL, 54LS/74LS	0.7	2.0	0.4	2.5	0.8	2.0	0.5	2.7	V

$V_{OL}$  and  $V_{OH}$  are the voltages generated at the output.  $V_{IL}$  and  $V_{IH}$  are the voltages required at the input to generate the appropriate levels. The numbers given above are guaranteed worst-case values for standard outputs.

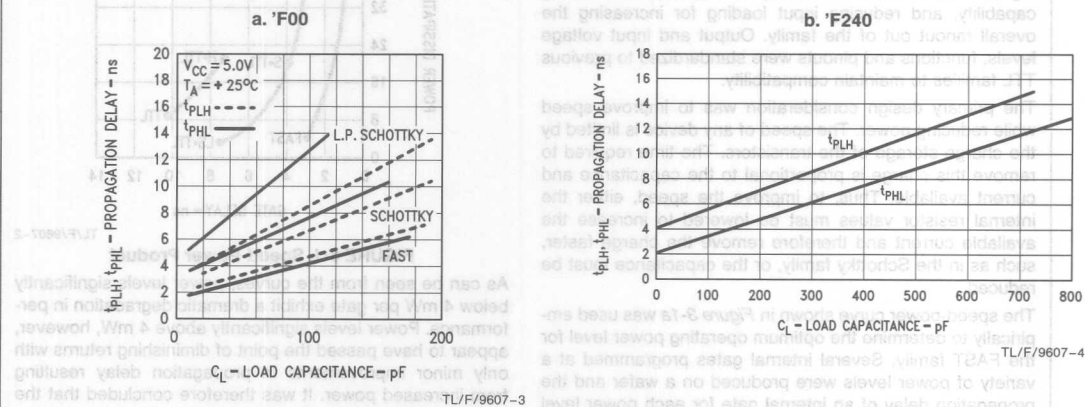


FIGURE 3-2. Propagation Delay vs Load Capacitance

Notice also that for Schottky, the HIGH-to-LOW output transition is more affected than its LOW-to-HIGH transition, while for FAST both transitions are equally affected. This indicates a better balance in the design of the FAST output, and minimizes pulse stretching and compressing.

Designers are cautioned that curves of this type do not apply when the load capacitance is distributed along an interconnection.

#### TEST AND SPECIFICATION IMPROVEMENTS

Because the circuitry and technological improvements (feedback and speedup diodes and the Miller Killer circuitry) yield well-controlled AC parameters, the FAST family can be specified over extremes of external influences. FAST is the first TTL logic family which does not require derating estimates for worst-case design. This has been accomplished by specifying minimum and maximum propagation delays over the operating temperature and supply voltage ranges with 50 pF loading.

In order to achieve easier correlation with our customers' needs, a change in the actual AC test load was needed. Previously, most TTL families were measured with three serial diodes in parallel with the load capacitor. For the FAST logic family, a 50 pF capacitance in parallel with a 500Ω resistor is employed. This facilitates fabrication of low capacitance test jigs. It also provides better correlation with customers' measurements of propagation delay. Passive 500Ω scope probes, which are less expensive and easier to use than the high impedance FET input scope probes, can be employed. This facilitates measurement of the AC performance on automatic test equipment and yields more conservative AC figures than are achieved with the previous AC load technique.

#### DESIGN CONSIDERATIONS

There are areas of concern which need to be addressed when designing with any high performance logic family. These topics include: transmission line concepts, printed circuit board layout, interfacing between technologies, open collector outputs, fanout, and unused inputs.

For additional information, please refer to National's FAST Applications Handbook.

#### TRANSMISSION LINES

Practical transmission lines, cables and strip lines used for TTL interconnections have a characteristic impedance between 30Ω and 150Ω. FAST is capable of driving a 50Ω line under worst-case conditions.

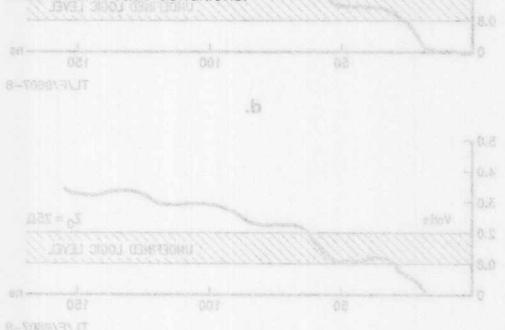


FIGURE 3-4. TTL Driving Transmission Line

Note that the worst-case values, assuming a 30% tolerance on the current limiting resistor and a 10% tolerance on  $V_{CC}$  is 80% higher than the values for nominal conditions.

These considerations, applicable only when the round trip delay of the line is longer than the rise or fall time of the driving signal ( $2t_d > t_r$ ), do not affect most TTL interconnections. Short interconnections do not behave like a resistive transmission line, but more like a capacitive load. Since the rise time of different TTL outputs is known, the longest interconnection that can be tolerated without causing transmission line effects can easily be calculated and is listed in Table III-II.

TABLE III-II. PC Board Interconnections

TTL Family	Rise Time	Fall Time	Max Interconnection Length
54/74, 54/74LS	6–9 ns	4–6 ns	18 in. (45 cm)
54S/74S	4–6 ns	2–3 ns	9 in. (22.5 cm)
FAST	1.8–2.8 ns	1.6–2.6 ns	7.5 in. (19 cm)

Assuming 1.7 ns/foot propagation speed, typical for epoxy fiberglass PC boards with  $\epsilon_r = 4.7$ .

Slightly longer interconnections show minimal transmission line effects; the longer the interconnections, the greater the chance that system performance may be degraded due to reflections and ringing.

#### TRANSMISSION LINE EFFECTS

The fast rise and fall times of TTL outputs (2.0 ns to 6.0 ns) produce transmission line effects even with relatively short (<2 ft) interconnections. Consider one TTL device driving another and switching from the LOW to the HIGH state. If the propagation delay of the interconnection is long compared to the rise time of the signal, the arrangement behaves like a transmission line driven by a generator with a non-linear output impedance. Simple transmission line theory shows that the initial voltage step at the output just after the driver has switched is

$$V_{OUT} = V_E \frac{Z_0}{Z_0 + R_O}$$

where  $Z_0$  is the characteristic impedance of the line,  $R_O$  is the output impedance of the driver, and  $V_E$  is the equivalent output voltage source in the driver, (i.e.,  $V_{CC}$  minus the forward drop of the pull-up transistors).

Figure 3-3 shows how the initial voltage step can be determined graphically by superimposing lines of constant impedance of the static input and output characteristics of TTL elements. The constant impedance lines are drawn from the intersection of the  $V_{IN}$  and  $V_{OL}$  characteristics which is the quiescent condition preceding a LOW-to-HIGH transition. After this transition the  $V_{OH}$  characteristic applies, and the intersection of a particular impedance line with the  $V_{OH}$  characteristic determines the initial voltage step. The  $V_{OH}$  characteristic shown in Figure 3-3 has an  $R_O$  of about 80Ω and  $V_E$  of approximately 4.0V, for calculation purposes.

These considerations, applicable only when the round trip delay of the line is longer than the rise or fall time of the driving signal ( $t_{\text{rise}}$ ), do not affect most TTL interconnections. Short interconnections do not behave like a resistive transmission line but more like a capacitive load. Since the rise time of the TTL outputs is known, the longest interconnection that can be tolerated without causing transmission line effects can easily be calculated and is listed in Table III-II.

TABLE III-II: PCB Interconnections

Max Interconnection Length	Max Interconnection Length
4-8 ns (18 in. (45 cm))	4-8 ns (18 in. (45 cm))
2-3 ns (9 in. (22.5 cm))	2-3 ns (9 in. (22.5 cm))
1.8-2.5 ns (7.5 in. (19 cm))	1.8-2.5 ns (7.5 in. (19 cm))

Interconnections show minimal transmission line effects when the round trip delay is less than the rise or fall time of the driving signal. The longer the interconnections, the greater the transmission line effects. System performance may be degraded due to transmission line effects.

TRANS. LINE EFFECTS  
The fast rise and fall times of TTL outputs (2.0 ns to 8.0 ns) produce transmission line effects even with relatively short interconnections. Consider one TTL device driving a load. The output voltage will rise from LOW to the HIGH state. If the round trip delay of the system is longer than the rise time of the driving signal, the initial output voltage  $V_{\text{OUT}}$  might not exceed  $V_{\text{IH}}$ . This input is then undetermined until after the round trip of the system. Figure 3-4 shows the F00 driver output waveform for four different line impedances.

This initial voltage step propagates down the line and reflects at the end, assuming the typical case where the line is open-ended or terminated in an impedance greater than its characteristic impedance  $Z_0$ . Arriving back at the source, this reflected wave increases  $V_{\text{OUT}}$ . If the total round-trip delay is larger than the rise time of the driving signal, there is a staircase response at the driver output and anywhere along the line. If one of the loads (gate inputs) is connected to the line close to the driver, the initial output voltage  $V_{\text{OUT}}$  might not exceed  $V_{\text{IH}}$ . This input is then undetermined until after the round trip of the system. Figure 3-4 shows the F00 driver output waveform for four different line impedances.

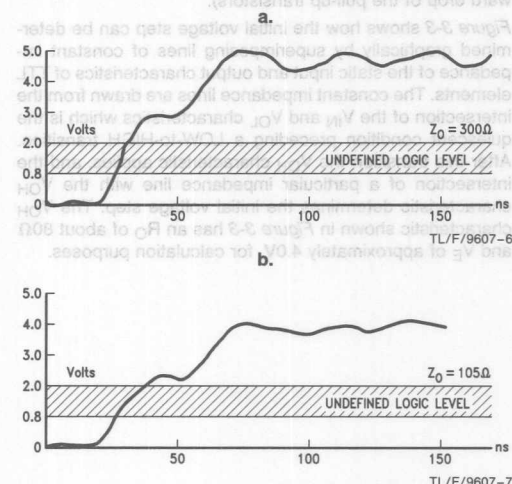


FIGURE 3-4. TTL Driving Transmission Line

Note that the worst-case value, assuming a +30% tolerance on the current limiting resistor and a -10% tolerance on  $V_{\text{CC}}$ , is 80% higher than the value for nominal conditions.

Notice also that for Schottky, the HIGH-TO-LOW output transition is more affected than the LOW-TO-HIGH transition, while for FAST both transitions are equally affected. This indicates a better balance in the design of the FAST output, and minimizes pulse distortion and compression.

Designers are cautioned that curves of this type do not apply when the load capacitance is distributed along an interconnection.

TEST AND SPECIFICATION IMPROVEMENTS  
Because the circuitry and mechanical improvements (feedback and speedup diodes) in the FAST family can be specified over a wide range of external impedances, FAST is the first TTL logic family which does not require detailed estimates for worst-case design. This has been achieved by specifying minimum and maximum propagation delays over the operating temperature and supply voltage ranges with 80 pf loading.

In order to achieve easier correlation with our customers' needs, a change in the actual AC test load was needed. Previous most TTL families were measured with three standard diodes in parallel with the load capacitor. For the FAST logic family a 50 pf capacitance in parallel with a 500Ω resistor is employed. This facilitates fabrication of low cost test pads. It also provides better correlation with customers' measurements of propagation delay. Previous 500Ω capacitors, which were used for testing, are no longer recommended.

For  $Z_0$  of 25Ω and 50Ω, the initial voltage step is in the threshold region of a TTL input and the output voltage only rises above the guaranteed 2.0V  $V_{\text{IH}}$  level after a reflection returns from the end of the line. If  $V_{\text{OUT}}$  is increased to > 2.0V, by either increasing  $Z_0$  or decreasing  $R_0$ , additional delay does not occur.  $R_0$  is characteristic of the driver output configuration, varying between the different TTL speed categories.  $Z_0$  can be changed by varying the width of the conductor and its distance from ground. Table III-III lists the lowest transmission line impedance that can be driven by different TTL devices to insure an initial voltage step of 2.0V.

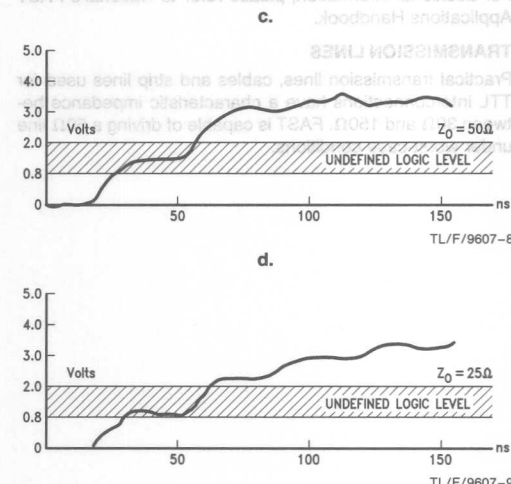


TABLE III-III. Transmission Line Driving Capability

TTL Family or Device	Collector Resistor $R_{\Omega}$	Lowest Transmission Line Impedance $\Omega$				
		Worst Case ( $R + 30\%$ )	Nominal	Best Case ( $R - 30\%$ )		
54/74	130	241.4	204.8	136.8	84.6	75.8
54S/74S	55	110.0	92.2	61.1	37.5	33.4
5440/7440	100	185.7	157.5	105.2	65.1	58.3
54S/74S40	25	50.0	41.9	27.7	17.0	15.2
54F/74F00	45	66.2	57.7	40.9	27.6	25.0
54F/74F258	25	36.76	32.0	22.7	15.3	13.9
54F/74F240	15	22.0	19.2	13.6	9.2	8.3
Supply Voltage ( $V_{CC}$ )		4.50	4.75	5.00	5.25	5.50

A graphical method provides excellent insight into the effects of high-speed digital circuits driving interconnections acting as transmission lines. A load line is drawn for each input and output situation. Each load line starts at the previous quiescent point, determined where the previous load line intersects the appropriate characteristic. The magnitude of the slope of the load lines is identical and equal to the characteristics impedance of the line, but alternate load lines have opposite signs representing the change in direction of current flow. The points where the load lines intersect the input and output characteristics represent the voltage and current value at the input or output, respectively, for that reflection. The results, Figure 3-5, are shown with and without the input diode and illustrate how the input diode on TTL elements assists in eliminating spurious switching due to reflection.

#### TRANSMISSION LINE CONCEPTS

The interactions between wiring and circuitry in high-speed systems are more easily determined by treating the interconnections as transmission lines. A brief review of basic concepts is presented and simplified methods of analysis

are used to examine situations commonly encountered in digital systems. Since the principles and methods apply to any type of logic circuit, normalized pulse amplitudes are used in sample waveforms and calculations.

#### SIMPLIFYING ASSUMPTIONS

For the great majority of interconnections in digital systems, the resistance of the conductors is much less than the input and output resistance of the circuits. Similarly, the insulating materials have very good dielectric properties. These circumstances allow such factors as attenuation, phase distortion and bandwidth limitations to be ignored. With these simplifications, interconnections can be dealt with in terms of characteristic impedance and propagation delay.

#### CHARACTERISTIC IMPEDANCE

The two conductors that interconnect a pair of circuits have distributed series inductance and distributed capacitance between them, and thus constitute a transmission line. For any length in which these distributed parameters are constant, the pair of conductors have a characteristic imped-

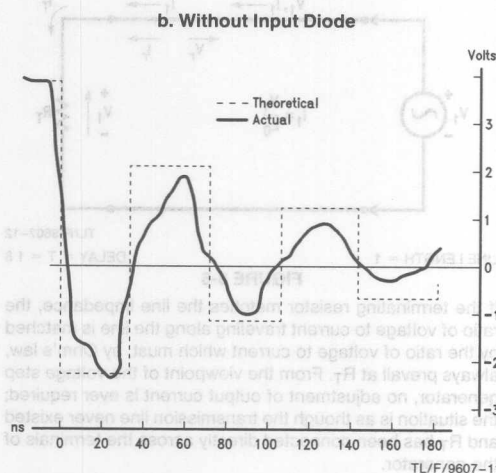
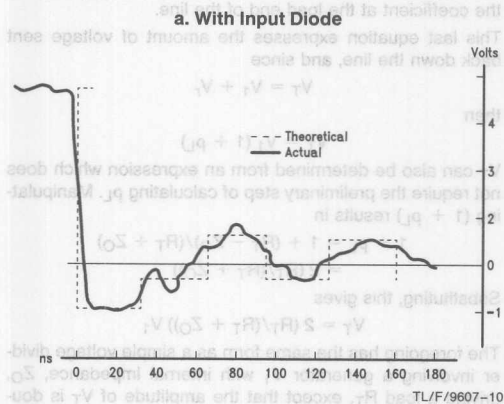


FIGURE 3-5. Ringing Caused by Reflections

ance  $Z_0$ . Where quiescent conditions on the line are determined by the circuits and terminations,  $Z_0$  is the ratio of transient voltage to transient current passing by a point on the line when a signal change or other electrical disturbance occurs. The relationship between transient voltage, transient current, characteristic impedance, and the distributed parameters is expressed as follows:

$$V/I = Z_0 = \sqrt{L_0/C_0}$$

where  $L_0$  = inductance per unit length, and  $C_0$  = capacitance per unit length.  $Z_0$  is in ohms,  $L_0$  in henries, and  $C_0$  in farads.

### PROPAGATION VELOCITY

Propagation velocity ( $v$ ) and its reciprocal, delay per unit length  $\delta$ , can also be expressed in terms of  $L_0$  and  $C_0$ . A consistent set of units is nanoseconds, microhenries and picofarads, with a common unit of length.

$$v = 1/\sqrt{L_0 C_0} \quad \delta = \sqrt{L_0 C_0}$$

These equations provide a convenient means of determining the  $L_0$  and  $C_0$  of a line when delay, length and impedance are known. For a length  $l$  and delay  $T$ ,  $\delta$  is the ratio  $T/l$ . To determine  $L_0$  and  $C_0$ , combine these equations.

$$L_0 = \delta Z_0$$

$$C_0 = \delta/Z_0$$

More formal treatments of transmission line effects are available from many sources.

### TERMINATION AND REFLECTION

A transmission line with a terminating resistor is shown in Figure 3-6. As indicated, a positive step function voltage travels from left to right. To keep track of reflection polarities, it is convenient to consider the lower conductor as the voltage reference and to think in terms of current flow in the top conductor only. The generator is assumed to have zero internal impedance. The initial current  $I_1$  is determined by  $V_1$  and  $Z_0$ .

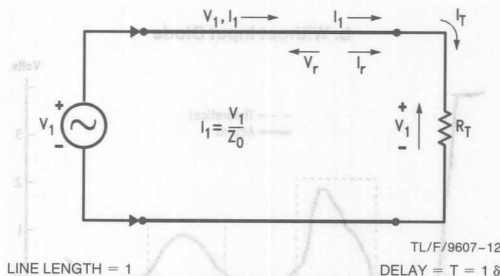


FIGURE 3-6

If the terminating resistor matches the line impedance, the ratio of voltage to current traveling along the line is matched by the ratio of voltage to current which must, by Ohm's law, always prevail at  $R_T$ . From the viewpoint of the voltage step generator, no adjustment of output current is ever required; the situation is as though the transmission line never existed and  $R_T$  has been connected directly across the terminals of the generator.

From the  $R_T$  viewpoint, the only thing the line did was delay the arrival of the voltage step by the amount of time  $T$ .

When  $R_T$  is not equal to  $Z_0$ , the initial current starting down the line is still determined by  $V_1$  and  $Z_0$  but the final steady

state current, after all reflections have died out, is determined by  $V_1$  and  $R_T$  (ohmic resistance of the line is assumed to be negligible). The ratio of voltage to current in the initial wave is not equal to the ratio of voltage to current demanded by  $R_T$ . Therefore, at the instant the initial wave arrives at  $R_T$ , another voltage and current wave must be generated so that Ohm's law is satisfied at the line-load interface. This reflected wave, indicated by  $V_r$  and  $I_r$  in Figure 3-6, starts to return toward the generator. Applying Kirchhoff's laws to the end of the line at the instant the initial wave arrives results in the following:

$$I_1 + I_r = I_T = \text{current into } R_T$$

Since only one voltage can exist at the end of the line at this instant of time, the following is true:

$$V_1 + V_r = V_T$$

thus,

$$I_T = V_T/R_T = (V_1 + V_r)/R_T$$

also,

$$I_1 = V_1/Z_0 \text{ and } I_r = -V_r/Z_0$$

with the minus sign indicating that  $V_r$  is moving toward the generator.

Combining the foregoing relationships algebraically and solving for  $V_r$  yields a simplified expression in terms of  $V_1$ ,  $Z_0$  and  $R_T$ :

$$\begin{aligned} \frac{V_1}{Z_0} - \frac{V_r}{Z_0} &= \frac{V_1 + V_r}{R_T} = \frac{V_1}{R_T} + \frac{V_r}{R_T} \\ V_1 \left( \frac{1}{Z_0} - \frac{1}{R_T} \right) &= V_r \left( \frac{1}{R_T} + \frac{1}{Z_0} \right) \\ V_r &= V_1 \left( \frac{R_T - Z_0}{R_T + Z_0} \right) = \rho_L V_1 \end{aligned}$$

The term in parentheses is called the coefficient of reflection ( $\rho_L$ ). With  $R_T$  ranging between zero (shorted line) and infinity (open line), the coefficient ranges between  $-1$  and  $+1$  respectively. The subscript  $L$  indicates that  $\rho_L$  refers to the coefficient at the load end of the line.

This last equation expresses the amount of voltage sent back down the line, and since

$$V_T = V_1 + V_r$$

then

$$V_T = V_1 (1 + \rho_L)$$

$V_T$  can also be determined from an expression which does not require the preliminary step of calculating  $\rho_L$ . Manipulating  $(1 + \rho_L)$  results in

$$\begin{aligned} 1 + \rho_L &= 1 + (R_T - Z_0)/(R_T + Z_0) \\ &= 2(R_T/(R_T + Z_0)) \end{aligned}$$

Substituting, this gives

$$V_T = 2(R_T/(R_T + Z_0)) V_1$$

The foregoing has the same form as a simple voltage divider involving a generator  $V_1$  with internal impedance,  $Z_0$ , driving a load  $R_T$ , except that the amplitude of  $V_T$  is doubled.

The arrow indicating the direction of  $V_r$  in Figure 3-6 correctly indicates the  $V_r$  direction of travel, but the direction of  $I_r$  flow depends on the  $V_r$  polarity. If  $V_r$  is positive,  $I_r$  flows toward the generator, opposing  $I_1$ . This relationship between the polarity of  $V_r$  and the direction of  $I_r$  can be deduced by noting that if  $V_r$  is positive it is because  $R_T$  is greater than  $Z_0$ . In turn, this means that the initial current  $I_1$



is larger than the final quiescent current, dictated by  $V_1$  and  $R_T$ . Hence  $I_r$  must oppose  $I_1$  to reduce the line current to the final quiescent value. Similar reasoning shows that if  $V_r$  is negative,  $I_r$  flows in the same direction as  $I_1$ .

It is somewhat easier to determine the effect of  $V_r$  on line conditions by thinking of it as an independent voltage generator in series with  $R_T$ . With this concept, the direction of  $I_r$  is immediately apparent; its magnitude, however, is the ratio of  $V_r$  to  $Z_0$ , i.e.,  $R_T$  is already accounted for in the magnitude of  $V_r$ . The relationships between incident and reflected signals are represented in Figure 3-7 for both cases of mismatch between  $R_T$  and  $Z_0$ .

The incident wave is shown in Figure 3-7a, before it has reached the end of the line. In Figure 3-7b, a positive  $V_r$  is returning to the generator. To the left of  $V_r$  the current is still  $I_1$ , flowing to the right, while to the right of  $V_r$  the net current in the line is the difference between  $I_1$  and  $I_r$ . In Figure 3-7c, the reflection coefficient is negative, producing a negative  $V_r$ . This, in turn, causes an increase in the amount of current flowing to the right behind the  $V_r$  wave.

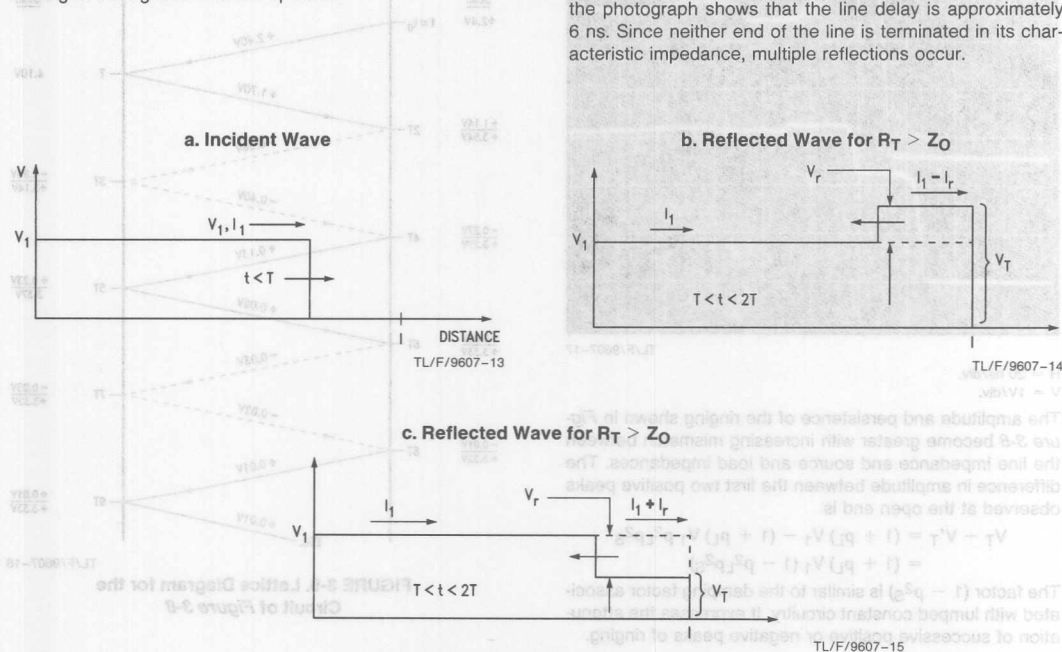


FIGURE 3-7. Reflections for  $R_T = Z_0$

### SOURCE IMPEDANCE, MULTIPLE REFLECTIONS

When a reflected voltage arrives back at the source (generator), the reflection coefficient at the source determines the response to  $V_r$ . The coefficient of reflection at the source is governed by  $Z_0$  and the source resistance  $R_S$ .

$$\rho_S = (R_S - Z_0)/(R_S + Z_0)$$

If the source impedance matches the line impedance, a reflected voltage arriving at the source is not reflected back toward the load end. Voltage and current on the line are stable with the following values.

$$V_T = V_i + V_r$$

If neither source impedance nor terminating impedance matches  $Z_0$ , multiple reflections occur; the voltage at each end of the line comes closer to the final steady state value with each succeeding reflection. An example of a line mismatched on both ends is shown in Figure 3-8. The source is a step function of  $V_{CC} = 5.0V$  amplitude occurring at time  $t_0$ . The initial value of  $V_1$  starting down the line is  $2.4V$  due to the voltage divider action of  $Z_0$  and  $R_S$ . The time scale in the photograph shows that the line delay is approximately 6 ns. Since neither end of the line is terminated in its characteristic impedance, multiple reflections occur.



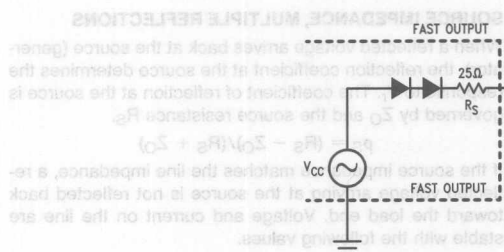


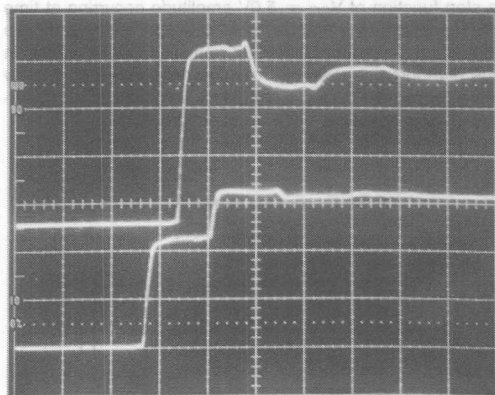
FIGURE 3-8. Multiple Reflections Due to Mismatch at Load and Source

$$PS = \frac{(25 - 50)\Omega}{(25 + 50)\Omega} = -0.33$$

$$V_0 = V_{CC} - 2 \cdot V_{BE} = 3.6V$$

$$\text{Initially, } V_1 = \frac{Z_0}{Z_0 + R_S} \cdot V_0 = \frac{50\Omega}{(50 + 25)\Omega} (3.6V) = 2.4V$$

$$PL = \frac{(300 - 50)\Omega}{(300 + 50)\Omega} = 0.71$$



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H = 20 ns/div.  
V = 1V/div.

The amplitude and persistence of the ringing shown in Figure 3-8 become greater with increasing mismatch between the line impedance and source and load impedances. The difference in amplitude between the first two positive peaks observed at the open end is

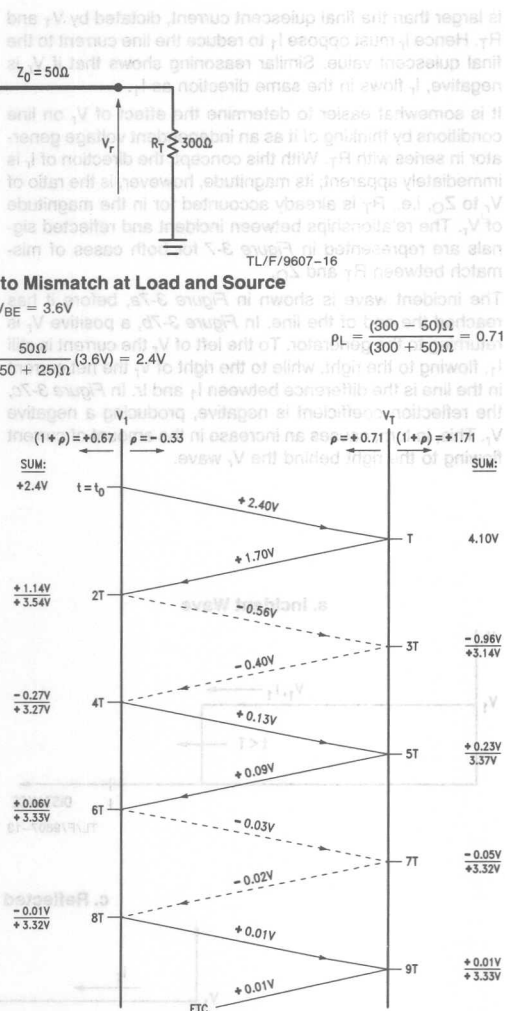
$$V_T - V'_T = (1 + \rho_L) V_1 - (1 + \rho_L) V_1 \rho_L \rho_S^2$$

$$= (1 + \rho_L) V_1 (1 - \rho_L \rho_S^2)$$

The factor  $(1 - \rho_S^2)$  is similar to the damping factor associated with lumped constant circuitry. It expresses the attenuation of successive positive or negative peaks of ringing.

#### LATTICE DIAGRAM

In the presence of multiple reflections, keeping track of the incremental waves on the line and the net voltage at the ends becomes a bookkeeping chore. A convenient and systematic method of indicating the conditions which combine magnitude, polarity and time utilizes a graphic construction called a lattice diagram. A lattice diagram for the line conditions of Figure 3-8 is shown in Figure 3-9.



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FIGURE 3-9. Lattice Diagram for the Circuit of Figure 3-8

The vertical lines symbolize discontinuity points, in this case the ends of the line. A time scale is marked off on each line in increments of  $2T$ , starting at  $t_0$  for  $V_1$  and  $T$  voltages traveling between the ends of the line; solid lines are used for positive voltages and dashed lines for transmission multipliers  $\rho$  and  $(1 + \rho)$  at each vertical line, and to tabulate the incremental and net voltages in columns alongside the vertical lines. Both the lattice diagram and the waveform photograph show that  $V_1$  and  $V_T$  asymptotically approach 3.4V, as they must with a 3.4V source driving a lightly loaded line.

### SHORTED LINE

The open-ended line in Figure 3-8 has a reflection coefficient of 0.71 and the successive reflections tend toward the steady state conditions of zero line current and a line voltage equal to the source voltage. In contrast, a shorted line has a reflection coefficient of  $-1$  and successive reflections must cause the line conditions to approach the steady state conditions of zero voltage and a line current determined by the source voltage and resistance.

Shorted line conditions are shown in Figure 3-10a with the reflection coefficient at the source end of the line also negative. A negative coefficient at both ends of the line means that any voltage approaching either end of the line is reflected in the opposite polarity. Figure 3-10b shows the response to an input step-function with a duration much longer than the line delay. The initial voltage starting down the line is about 2.4V, which is inverted at the shorted end and returned toward the source as  $-2.4V$ . Arriving back at the source end of the line, this voltage is multiplied by  $(1 + \rho_S)$ , causing a  $-1.61V$  net change in  $V_1$ . Concurrently, a reflected voltage of  $+0.80V$  ( $-2.4V$  times  $\rho_S$  of  $-0.33$ ) starts back toward the shorted end of the line. The voltage at  $V_1$  is reduced by 50% with each successive round trip of reflections, thus leading to the final condition of zero volts on the line.

When the duration of the input pulse is less than the delay of the line, the reflections observed at the source end of the line constitute a train of negative pulses, as shown in Figure 3-10c. The amplitude decreases by 50% with each successive occurrence as it did in Figure 3-10b.

### SERIES TERMINATION

Driving an open-ended line through a source resistance equal to the line impedance is called series termination. It is particularly useful when transmitting signals which originate on a PC board and travel through the back-plane to another board, with the attendant discontinuities, since reflections coming back to the source are absorbed and ringing thereby controlled. The amplitude of the initial signal sent down the line is only half of the generator voltage, while the voltage at the open end of the line is doubled to full amplitude ( $1 + \rho_L = 2$ ). The reflected voltage arriving back at the source raises  $V_1$  to the full amplitude of the generator signal. Since the reflection coefficient at the source is zero, no further changes occur and the line voltage is equal to the generator voltage. Because the initial signal on the line is only half the normal signal swing, the loads must be connected at or near the end of the line to avoid receiving a 2-step input signal.

A TTL output driving a series-terminated line is severely limited in its fanout capabilities due to the IR drop associated with the collective  $I_L$  drops of the inputs being driven. For most TTL families other than FAST it should not be considered since either the input currents are so high (TTL, S, H) or the input threshold is very low (LS). In either case the noise margins are severely degraded to the point where the circuit becomes unusable. In FAST, however, the  $I_L$  of 0.6 mA, if sunk through a resistor of  $25\Omega$  used a series terminating resistor, will reduce the low level noise margin 15 mV for each standard FAST input driven.

FIGURE 3-10 Reflections of Long and Short Pulses on a Shorted Line

All the above information on impedance and propagation delays are for the circuit interconnect only. The actual impedances and propagation delays will differ from this by the loading effects of gate input and output capacitances, and by any connectors that may be in line. The effective impedance and propagation delay can be determined from the following formula:

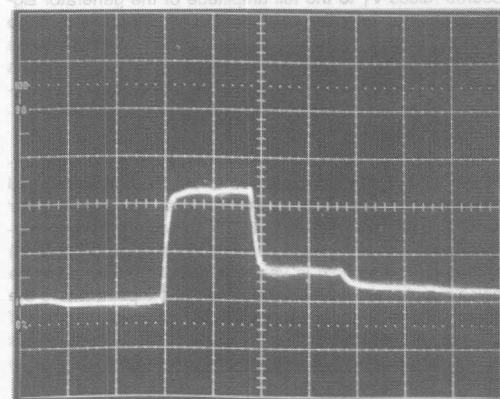
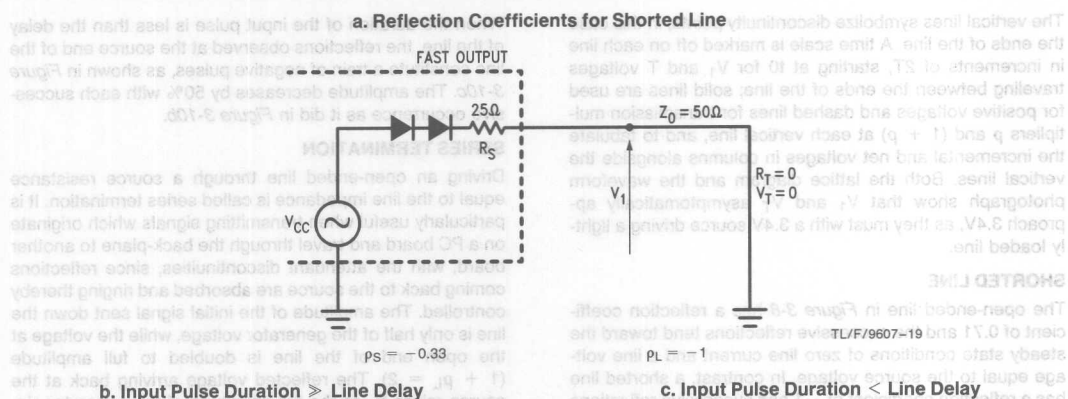
$$Z_{in} = \sqrt{\frac{L}{C}} \sqrt{1 + \left(\frac{C_L}{C}\right)^2}$$

$$t_{pd} = \sqrt{LC} \sqrt{1 + \left(\frac{C_L}{C}\right)^2}$$

where  $C_L$  is the total of all additional loading. The results of these formulas will frequently give effective impedances of less than half  $Z_0$  and interconnect propagation delays greater than the driving device propagation delay, thus becoming the predominant delay.

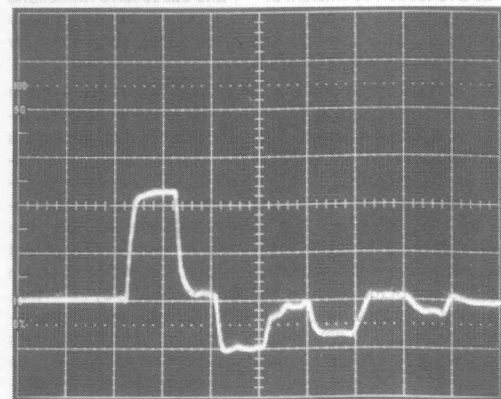
TABLE III-IV. Relative Dielectric Constants at Various Materials

Material	$\epsilon_r$
Polyethylene	2.2
Mylar	3.0
Epoxy Glass	4.7
Dairin	3.7
Epoxy Resin	3.6
Polyvinylchloride (PVC)	3.5
Silicon Rubber	3.4
Nylon	3.3
Polyurethane	3.2
Polyethylene	2.3
Teflon	2.1
Cellular Polyethylene	1.8
Polyethylene Foam	1.8
Air	1.0



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V = 1V/div.  
H = 20 ns/div.



TL/F/9607-20

FIGURE 3-10. Reflections of Long and Short Pulses on a Shorted Line

TABLE III-IV. Relative Dielectric Constants of Various Materials

Material	$\epsilon_r$
Air	1.0
Polyethylene Foam	1.6
Cellular Polyethylene	1.8
Teflon	2.1
Polyethylene	2.3
Polystyrene	2.5
Nylon	3.0
Silicon Rubber	3.1
Polyvinylchloride (PVC)	3.5
Epoxy Resin	3.6
Delrin	3.7
Epoxy Glass	4.7
Mylar	5.0
Polyurethane	7.0

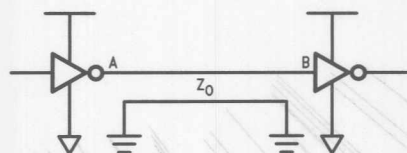
All the above information on impedance and propagation delays are for the circuit interconnect only. The actual impedance and propagation delays will differ from this by the loading effects of gate input and output capacitances, and by any connectors that may be in line. The effective impedance and propagation delay can be determined from the following formula:

$$Z_O' = \sqrt{1 + \left(\frac{C_L}{C_O}\right)} \Omega$$

$$t_{PD} = \sqrt{L_O C_O} \therefore t_{PD}' = t_{PD} \sqrt{1 + \left(\frac{C_L}{C_O}\right)}$$

where  $C_L$  is the total of all additional loading.

The results of these formulas will frequently give effective impedances of less than half  $Z_O$ , and interconnect propagation delays greater than the driving device propagation delays, thus becoming the predominant delay.



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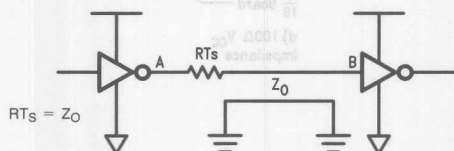
FIGURE 3-11. Unterminated

The maximum length for an unterminated line can be determined by

$$l_{\max} = T_r / 2t_{pd}$$

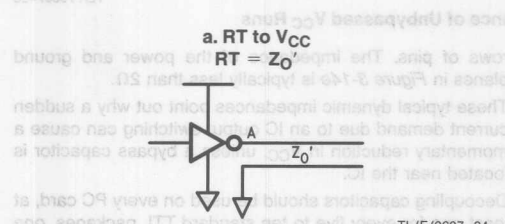
and for FAST,  $t_r = 3$  ns, so  $l_{\max} = 10$  inches for trace on G10 epoxy glass PC.

The voltage wave propagated down the transmission line ( $V$  step) is the full output drive of the device into  $Z_0$ . Reflections will not be a problem if  $l \leq l_{\max}$ . Lines longer than  $l_{\max}$  will be subject to ringing and reflections and will drive the inputs and outputs below ground.

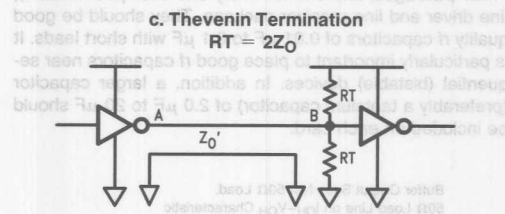


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FIGURE 3-12. Series-Terminated



TL/F/9607-24

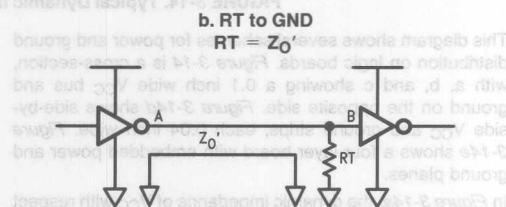


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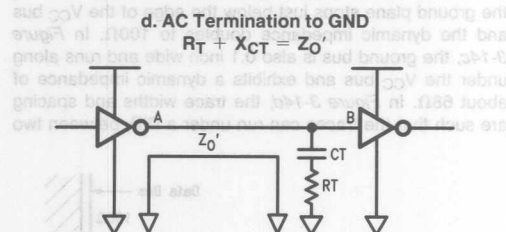
Series termination has limited use in TTL interconnect schemes due to the voltage drop across RTs in the LOW state, reducing noise margins at the receiver. Series termination is the ideal termination for highly capacitive memory arrays whose DC loadings are minimal. RTs values of 10Ω to 50Ω are normally found in these applications.

Four possibilities for parallel termination exist:

- $Z_0'$  to  $V_{CC}$ . This will consume current from  $V_{CC}$  when output is LOW;
- $Z_0'$  to GND. This will consume current from  $V_{CC}$  when output is HIGH;
- Thevenin equivalent termination. This will consume half the current of A and B from the output stage, but will have reduced noise margins, and consume current from  $V_{CC}$  with outputs HIGH or LOW. If used on a TRI-STATE® bus, this will set the quiescent line voltage to half.
- AC Termination. An RC termination to GND,  $C = 3tr/Z_0$ . This consumes no DC current with outputs in either state. If this is used on a TRI-STATE bus, then the quiescent voltage on the line can be established at  $V_{CC}$  or GND by a high value pull up (down) resistor to the appropriate supply rail.



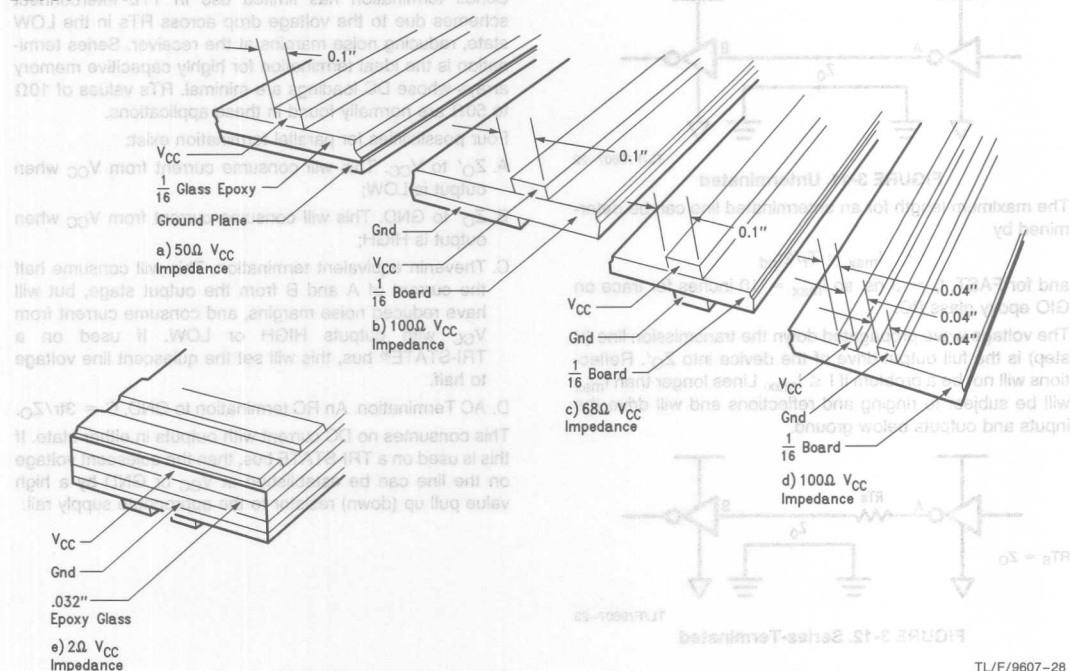
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TL/F/9607-27

FIGURE 3-13. Parallel Terminated

## DECOUPLING

FIGURE 3-14. Typical Dynamic Impedance of Unbypassed  $V_{CC}$  Runs

TL/F/9607-28

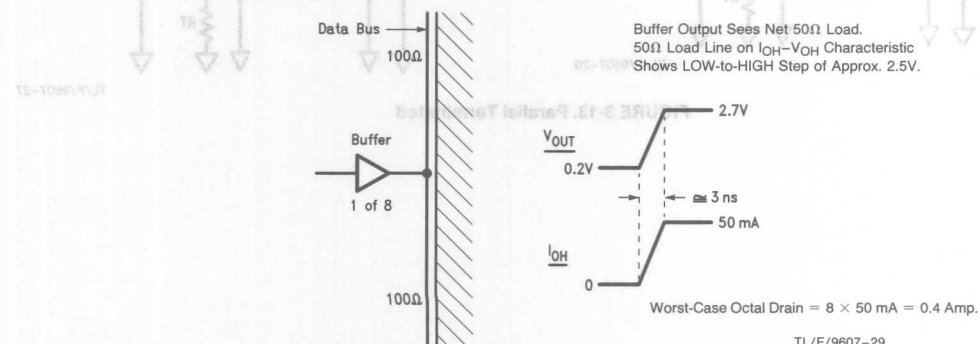
This diagram shows several schemes for power and ground distribution on logic boards. Figure 3-14 is a cross-section, with a, b, and c showing a 0.1 inch wide  $V_{CC}$  bus and ground on the opposite side. Figure 3-14d shows side-by-side  $V_{CC}$  and ground strips, each 0.04 inch wide. Figure 3-14e shows a four layer board with embedded power and ground planes.

In Figure 3-14a, the dynamic impedance of  $V_{CC}$  with respect to ground is  $50\Omega$ , even though the  $V_{CC}$  trace width is generous and there is a complete ground plane. In Figure 3-14b, the ground plane stops just below the edge of the  $V_{CC}$  bus and the dynamic impedance doubles to  $100\Omega$ . In Figure 3-14c, the ground bus is also 0.1 inch wide and runs along under the  $V_{CC}$  bus and exhibits a dynamic impedance of about  $68\Omega$ . In Figure 3-14d, the trace widths and spacing are such that the traces can run under a DIP, between two

rows of pins. The impedance of the power and ground planes in Figure 3-14e is typically less than  $2\Omega$ .

These typical dynamic impedances point out why a sudden current demand due to an IC output switching can cause a momentary reduction in  $V_{CC}$ , unless a bypass capacitor is located near the IC.

Decoupling capacitors should be used on every PC card, at least one for every five to ten standard TTL packages, one for every five 'LS and 'S packages, one for every three FAST packages, and one for every one-shot (monostable), line driver and line receiver package. They should be good quality rf capacitors of  $0.01\mu F$  to  $0.1\mu F$  with short leads. It is particularly important to place good rf capacitors near sequential (bistable) devices. In addition, a larger capacitor (preferably a tantalum capacitor) of  $2.0\mu F$  to  $20\mu F$  should be included on each card.



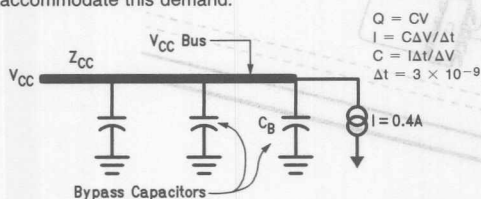
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FIGURE 3-15.  $I_{CC}$  Drain Due to Line Driving



This diagram illustrates the sudden demand for current from  $V_{CC}$  when a buffer output forces a LOW-to-HIGH transition into the midpoint of a data bus. The sketch shows a wire-over-ground transmission line, but it could also be a twisted pair, flat cable or PC interconnect.

The buffer output effectively sees two  $100\Omega$  lines in parallel and thus a  $50\Omega$  load. For this value of load impedance, the buffer output will force an initial LOW-to-HIGH transition from  $0.2V$  to  $2.7V$  in about  $3\text{ ns}$ . This net charge of  $2.5V$  into a  $50\Omega$  load causes an output-HIGH current change of  $50\text{ mA}$ . If all eight outputs of an octal buffer switch simultaneously, in this application the current demand on  $V_{CC}$  would be  $0.4A$ . Clearly, a nearby  $V_{CC}$  bypass capacitor is needed to accommodate this demand.



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**FIGURE 3-16.  $V_{CC}$  Bypass Capacitor for Octal Driver**

Specify  $V_{CC}$  Droop =  $0.1V$  max.

$$C = \frac{0.4 \times 3 \times 10^{-9}}{0.1} = 12 \times 10^{-9} = 0.012 \mu F$$

Select  $C_B \geq 0.02 \mu F$

A  $V_{CC}$  bus with bypass capacitors connected periodically along its length is shown above. Also shown is a current source representing the current demand of the buffer in the preceding application.

The equations illustrate an approximation method of estimating the size of a bypass capacitor based on the current demand, the drop in  $V_{CC}$  that can be tolerated and the length of time that the capacitor must supply the charge. While the demand is known, the other two parameters must be chosen. A  $V_{CC}$  droop of  $0.1V$  will not cause any appreciable change in performance, while a time duration of  $3\text{ ns}$  is long enough for other nearby bypass capacitors to help supply charge. If the current demand continues over a long period of time, charge must be supplied by a very large capacitor on the board. This is the reason for the recommendation that a large capacitor be located where  $V_{CC}$  comes onto a board. If the buffers are also located near the connector end of the board, the large capacitor helps supply charge sooner.

## DESIGN GUIDELINES

### Ground

A good ground system is essential for a PC card containing a large number of packages. The ground can either be a good ground bus, or better, a ground plane which, incorporated with the  $V_{CC}$  supply, forms a transmission line power system. Power transmission systems, which can be attached to a PC card to give an excellent power system without the cost of a multilayer PC card, are commercially available. Ground loops on or off PC cards are to be avoided unless they approximate a ground plane.

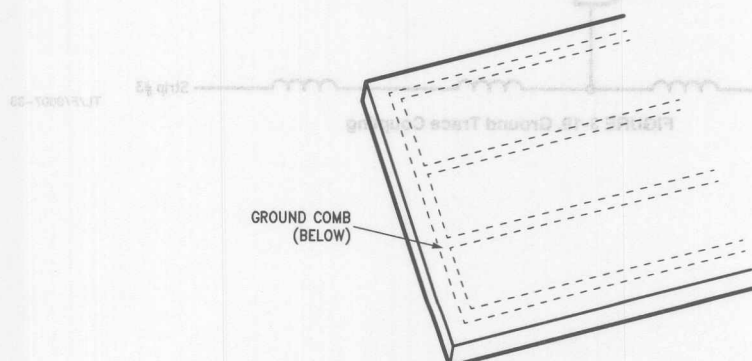
With the advent of FAST, with considerably faster edge rates and switching times, proper grounding practice has become of primary concern in printed circuit layout. Poor circuit grounding layout techniques may result in crosstalk and slowed switching rates. This reduces overall circuit performance and may necessitate costly redesign. Also when FAST chips are substituted for standard TTL-designed printed circuit boards, faster edge rates can cause noise problems. The source of these problems can be sorted into three categories:

1.  $V_{CC}$  droop due to faster load capacitance charging;
2. Coupling via ground paths adjacent to both signal sources and loads; and
3. Crosstalk caused by parallel signal paths.

$V_{CC}$  droop can be remedied with better or more bypassing to ground. The rule here is to place  $0.01 \mu F$  capacitors from  $V_{CC}$  to ground for every three FAST circuits used, as near the IC as possible. The other two problems are not as easily corrected, because PC boards, may already be manufactured and utilized. In this case, simply replacing TTL circuits with FAST compatible circuits is not always as easy as it may seem, especially on two-sided boards. In this situation IC placement is critical at high speeds. Also when designing high density circuit layout, a ground-plane layer is imperative to provide both a sufficiently low inductance current return path and to provide electromagnetic and electrostatic shielding thus preventing noise problem 2 and reducing, by a large degree, noise problem 3.

### Two-Sided PC Board Layout

When considering the two-sided PC board, more than one ground trace is often found in a parallel or non-parallel configuration. For this illustration parallel traces tied together at one end are shown. This arrangement is referred to as a ground comb. The ground comb is placed on one side of the PC board while the signal traces are on the other side, thus the two-sided circuit board.



**FIGURE 3-17**

TL/F/9607-31



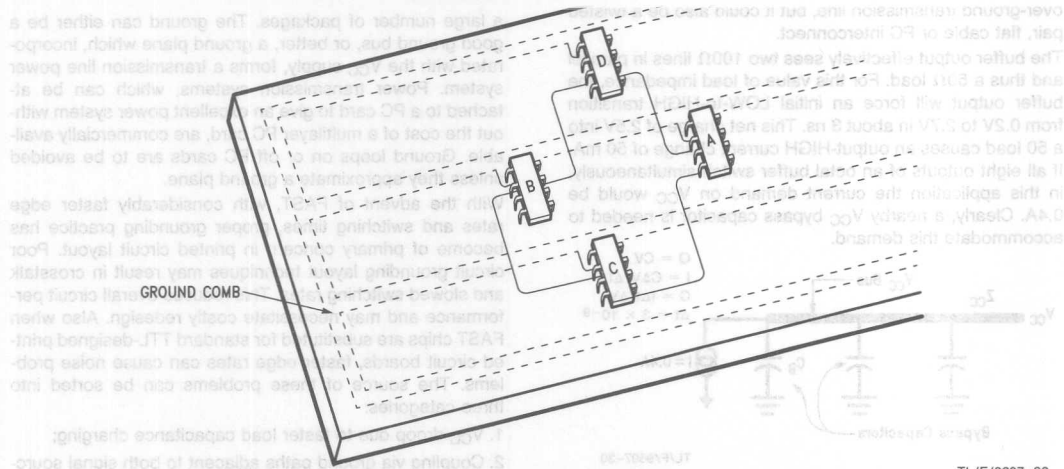


FIGURE 3-18

Figure 3-18 illustrates how noise is generated even though there is no apparent means of crosstalk between the circuits. If package A has an output which drives package D input and package B output drives package C input, there is no apparent path for crosstalk since mutual signal traces

are remotely located. What is significant, and must be emphasized here, is that circuit packages A and B accept their ground link from the same trace. Hence, circuit A may well couple noise to circuit B via the common or shared portion of the trace. This is especially true at high switching speeds.

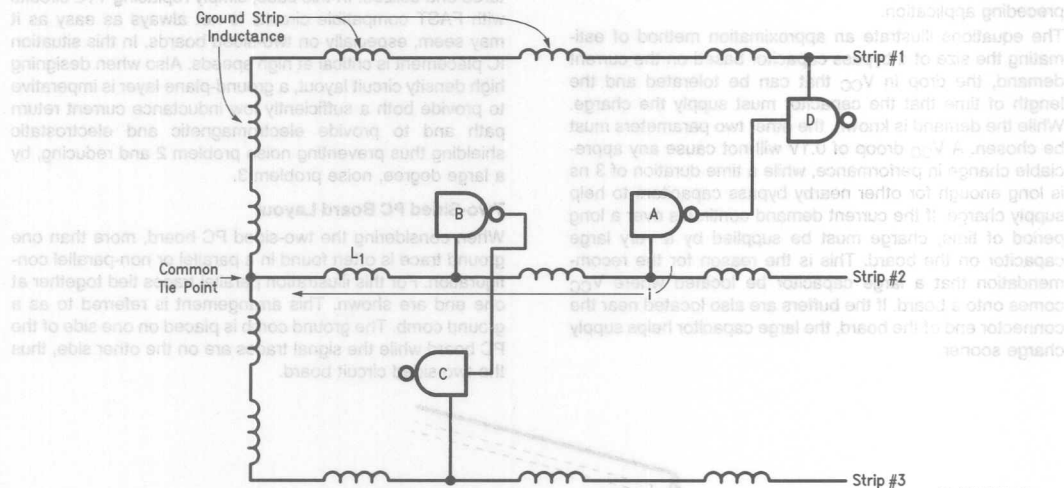


FIGURE 3-19. Ground Trace Coupling



can see that if we switch gate A from HIGH to LOW, the current for the transition is drawn from ground strip number two. Current flows in the direction indicated by the arrow to the common tie point. It can be seen that gate B shares ground strip number two with gate A from the point where gate B is grounded back to the common tie point. This length is represented by L1. When A switches states there is a current transient which occurs on the ground strip in the positive direction. This current spike is caused by the ground strip inductance and it is "felt" by gate B. If gate B is in a LOW state ( $V_{OL}$ ) the spike will appear on the output since gate B's  $V_{OL}$  level is with reference to ground. Thus if gate B's ground reference rises momentarily  $V_{OL}$  will also rise. Consequently, if gate B is output to another gate (C in the illustration) problems may arise.

#### Supply Voltage and Temperature

The normal supply voltage  $V_{CC}$  for all TTL circuits is +5.0V. Commercial grade parts are guaranteed to perform with a  $\pm 10\%$  supply tolerance ( $\pm 500$  mV) over an ambient temperature range of 0°C. Military grade parts are guaranteed to perform with  $\pm 10\%$  supply tolerance ( $\pm 500$  mV) over an ambient temperature range of -55°C to +125°C.

The actual junction temperature can be calculated by multiplying the power dissipation of the device with the thermal resistance of the package and adding it to the measured ambient temperature  $T_A$  or package (case) temperature  $T_C$ . For example, a device in ceramic DIP ( $\theta_{JA}$  100°C/W) dissipates typically 145 mW. At +55°C ambient temperature, the junction temperature is

$$T_J = (0.145 \times 100) + 55^\circ\text{C}$$

Designers should note that localized temperatures can rise well above the general ambient in a system enclosure. On a large PC board mounted in a horizontal plane, for example, the local temperature surrounding an IC in the middle of the board can be quite high due to the heating effect of the

All TTL circuits are compatible, and any TTL output can drive a certain number of TTL inputs. There are only subtle differences in the worst-case noise immunity when low power, standard and Schottky TTL circuits are intermixed. Open-collector outputs, however, require a pull-up resistor to drive TTL inputs reliably.

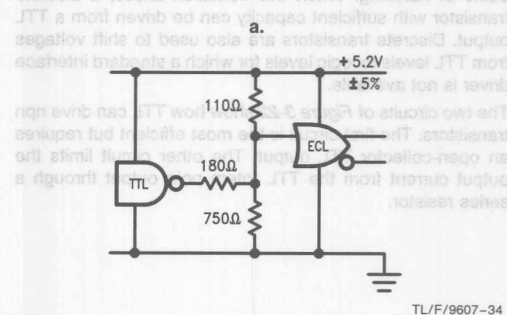
While TTL is the dominating logic family, and many systems use TTL exclusively, there are cases where different semiconductor technologies are used in one system, either to improve the performance or to lower the cost, size and power dissipation. The following explains how TTL circuits can interface with ECL, CMOS and discrete transistors.

**Interfacing TTL and ECL**—Mixing ECL and TTL logic families offers the design engineer a new level of freedom and opens the entire VHF frequency spectrum to the advantages of digital measurement, control and logic operation.

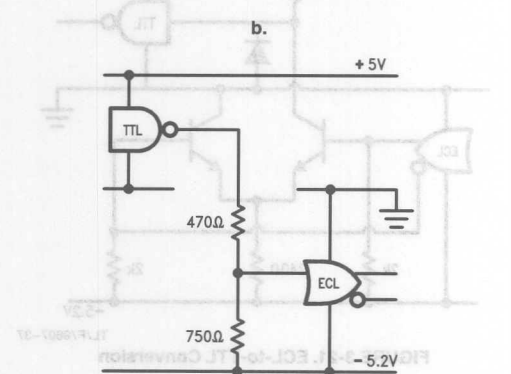
The main advantages gained with ECL are high speed, flexibility, design versatility and transmission line compatibility. But application and interfacing cost problems have traditionally discouraged the use of ECL in many areas, particularly in low cost, less sophisticated systems.

The most practical interfacing method for smaller systems involves using a common supply of +5.0V to +5.2V. Care must be exercised with both logic families when using this technique to assure proper bypassing of the power supply to prevent any coupling of noise between circuit families. When larger systems are operated on a common supply, separate power buses to each logic family help prevent problems. Otherwise, good high frequency bypassing techniques are usually sufficient.

ECL devices have high input impedance with input pull-down resistors ( $> 20$  k $\Omega$ ) to the negative supply. In the TTL to ECL interface circuits in Figure 3-20, it is assumed that the ECL devices have high input impedance.



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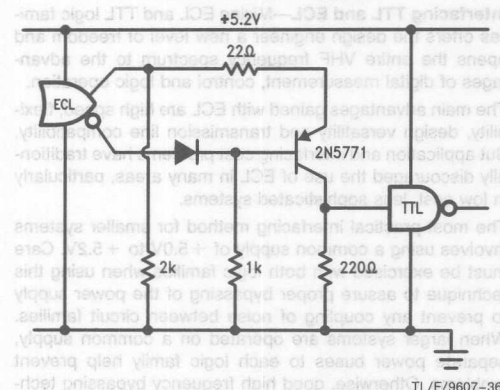
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FIGURE 3-20. TTL-to-ECL Conversion

All circuits described operate with  $\pm 5\%$  ECL and  $\pm 10\%$  TTL supply variations, except those with ECL and TTL on a common supply. In those cases, the supply can be  $\pm 10\%$  with ECL. All resistors are  $\frac{1}{4}W$ ,  $\pm 5\%$  composition type.

TTL to ECL conversion is easily accomplished with resistors, which simultaneously attenuate the TTL signal swing, shift the signal levels, and provide low impedance for damping and immunity to stray noise pick-up. The resistors should be located as near as possible to the ECL circuit for optimum effect. The circuits in Figure 3-20 assume an unloaded TTL gate as the standard TTL source. ECL input impedance is predominantly capacitive (approximately 3 pF); the net RC time constant of this capacitance with the indicated resistors assures a net propagation delay governed primarily by the TTL signal.

#### a. Common Power Supply



#### b. Separate Power Supplies

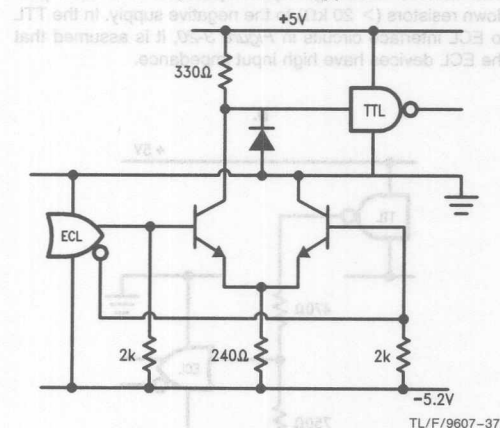


FIGURE 3-21. ECL-to-TTL Conversion

When interfacing between high voltage swing TTL logic and low voltage swing ECL logic, the more difficult conversion is from ECL to TTL. This requires a voltage amplifier to build up the 0.8V logic swing to a minimum of 2.5V. The circuits shown in Figure 3-21 may be used to interface from ECL to TTL.

The higher speed converters usually have the lowest fanout: only one or two TTL gates. This fanout can be increased simply by adding a TTL buffer gate to the output of the converter. Another option, where ultimate speed is required, is to use additional logic converters.

**Interfacing FAST and CMOS**—Due to their wide operating voltage range, CMOS devices will function outside of the standard  $\pm 5V \pm 10\%$  supply levels. For our purposes, only the case where both the FAST and CMOS devices are connected to the same voltage source will be considered.

FAST outputs can sink at least 20 mA in the LOW state. This is more than adequate to drive CMOS inputs to a valid LOW level. Due to their output designs, though, FAST outputs are unable to pull CMOS inputs to above approximately 4.0V. If the CMOS device does not have TTL-compatible input levels, the FAST output should be pulled with a resistor to  $V_{CC}$ . The value of this resistor will vary according to the system. Factors that affect the selection of the value are: edge rate—the smaller the resistor, the faster the edge rate; fanout—the smaller the resistor, the greater the fanout; and noise margins—the smaller the resistor, the greater the output HIGH noise margin and the smaller the output LOW noise margin. FAST outputs can directly drive TTL-compatible CMOS inputs, such as the inputs on ACT or HCT devices, without pull up registers.

Most CMOS outputs are capable of directly driving FAST inputs. Be aware, though, that TTL inputs have higher loading specifications than CMOS inputs. Care must be taken to insure that the CMOS outputs are not overloaded by the FAST input loading.

**TTL Driving Transistors**—Although high voltage, high current ICs are available, it is sometimes necessary to control greater currents or voltages than integrated circuits are capable of handling. When this condition arises, a discrete transistor with sufficient capacity can be driven from a TTL output. Discrete transistors are also used to shift voltages from TTL levels to logic levels for which a standard interface driver is not available.

The two circuits of Figure 3-22 show how TTL can drive npn transistors. The first circuit is the most efficient but requires an open-collector TTL output. The other circuit limits the output current from the TTL totem pole output through a series resistor.

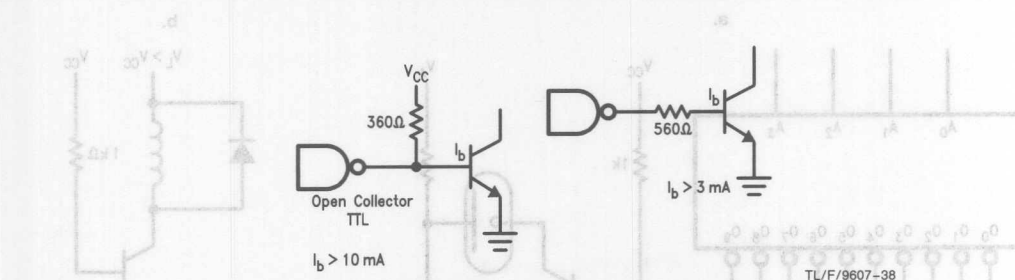


FIGURE 3-22. TTL Driving npn Transistors

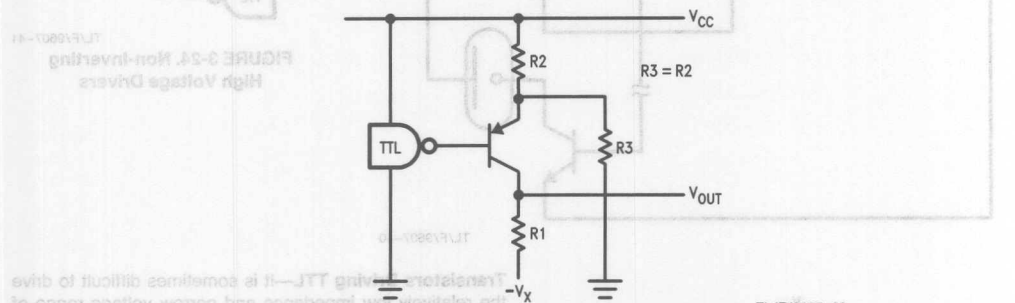


FIGURE 3-23. pnp Transistor Shifting TTL Output

**Shifting a TTL Output to Negative Levels**—The circuit of Figure 3-23 uses a pnp transistor to shift the TTL output to a negative level. When the TTL output is HIGH, the transistor is cut off and the output voltage is  $-V_x$ . When the TTL output is LOW, the transistor conducts and the output voltage is

$$V_{OUT} = -V_x + R_1/R_2 (V_{CC} - 2.0V)$$

if the transistor is not saturated, or slightly positive if the transistor is allowed to saturate.

**High Voltage Drivers**—A TTL output can be used to drive high voltage, low current loads through the simple, non-inverting circuits shown in Figure 3-24. This can be useful for driving gas discharge displays or small relays, where the TTL output can handle the current but not the voltage. Load current should not exceed  $I_{OL}$  ( $-4$  mA).

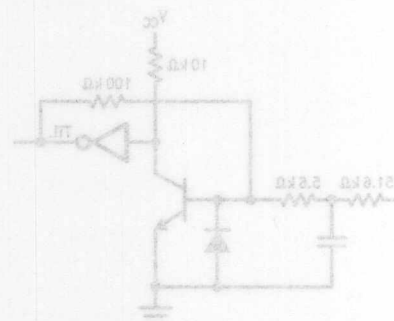


FIGURE 3-24. Transistor Driving TTL

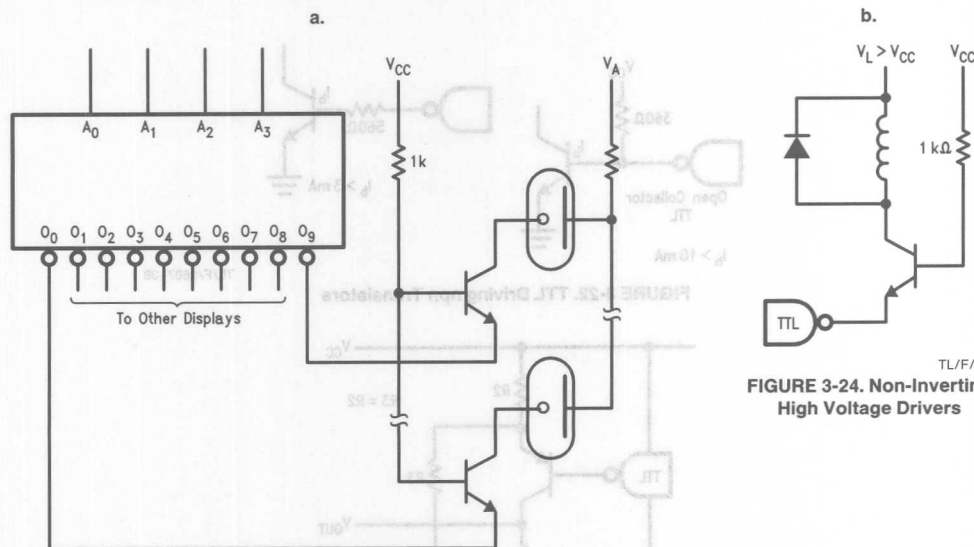


FIGURE 3-24. Non-Inverting High Voltage Drivers

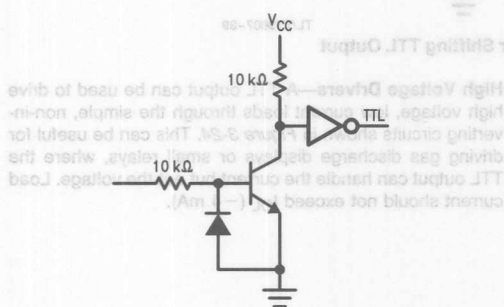


FIGURE 3-25. Transistors Driving TTL

**Transistors Driving TTL**—It is sometimes difficult to drive the relatively low impedance and narrow voltage range of TTL inputs directly from external sources, particularly in a rough, electrically noisy environment. The circuits shown in Figure 3-25 can handle input signal swings in excess of  $\pm 100V$  without harming the circuits. The second circuit has input RC filter that suppresses noise. Unambiguous TTL voltage levels are generated by the positive feedback (Schmitt trigger) connection.

#### OPEN COLLECTOR OUTPUTS

A number of available circuits have no pull-up circuit on the outputs. Open collector outputs are used for interfacing or for wired-OR (actually wired-AND) functions. The latter is achieved by connecting open collector outputs together and adding an external pull-up resistor.

The value of the pull-up resistor is determined by considering the fanout of the OR tie and the number of devices in the OR tie. The pull-up resistor value is chosen from a range between maximum value (established to maintain the required  $V_{OH}$  with all the OR-tied outputs HIGH) and a minimum value (established so that the OR tie fanout is not exceeded when only one output is LOW).

**MINIMUM AND MAXIMUM PULL-UP RESISTOR VALUES**

$$R_{X(MIN)} = \left( \frac{V_{CC(MAX)} - V_{OL}}{I_{OL} - N_2(LOW) \cdot 1.6 \text{ mA}} \right)$$

$$R_{X(MAX)} = \left( \frac{V_{CC(MIN)} - V_{OH}}{N_1 I_{OH} + N_2(HIGH) \cdot 40 \mu A} \right)$$

where:

$R_X$  = External pull-up resistor

$N_1$  = Number of wired-OR outputs

$N_2$  = Number of input unit loads being driven

$I_{OH} = I_{CEX}$  = Output HIGH leakage current

$I_{OL}$  = LOW level fanout current of driving element

$V_{OL}$  = Output LOW voltage level (0.5V)

$V_{OH}$  = Output HIGH voltage level (2.5V)

$V_{CC}$  = Power Supply Voltage

Example: four 'F524 gate outputs driving four other gates or MSI inputs.

$$R_{X(MIN)} = \left( \frac{5.5V - 0.5V}{8.0 \text{ mA} - 2.4 \text{ mA}} = \frac{5.0V}{5.6 \text{ mA}} \right) = 893\Omega$$

$$R_{X(MAX)} = \left( \frac{4.5V - 2.5V}{4 \cdot 250 \mu A + 2 \cdot 40 \mu A} = \frac{2.0V}{1.08 \text{ mA}} \right) = 1852\Omega$$

where:

$$N_1 = 4$$

$$N_2(HIGH) = 4 \cdot 0.5 \text{ U.L.} = 2 \text{ U.L.}$$

$$N_2(LOW) = 4 \cdot 0.375 \text{ U.L.} = 1.5 \text{ U.L.}$$

$$I_{OH} = 250 \mu A$$

$$I_{OL} = 8.0 \text{ mA}$$

$$V_{OL} = 0.5V$$

$$V_{OH} = 2.5V$$

Any values of pull-up resistor between 893 $\Omega$  and 1852 $\Omega$  can be used. The lower values yield the fastest speeds while the higher values yield the lowest power dissipation.

**INCREASING FANOUT**

To increase fanout, inputs and outputs of gates on the same package may be paralleled to those in a single package to avoid large transient supply currents due to different switching times of the gates. This is not detrimental to the devices, but could cause logic problems if the gates are being used as clock drivers.

**UNUSED INPUTS**

Theoretically, an unconnected input assumes the HIGH logic level, but practically speaking it is in an undefined logic state because it tends to act as an antenna for noise. Only a few hundred millivolts of noise may cause the unconnected input to go to the logic LOW state. On devices with memory (flip-flops, latches, registers, counters), it is particularly important to terminate unused inputs (MR, PE, PL, CP) properly since a noise spike on these inputs might change the contents of the memory. It is a poor design practice to leave unused inputs floating.

If the logic function calls for a LOW input, such as in NOR or OR gates, the input can be connected directly to ground. For a permanent HIGH signal, unused inputs can be tied directly to  $V_{CC}$ . An unused input may also be tied to a used input having the same logic function, such as NAND and AND gates, provided that the driver can handle the added  $I_{IH}$ . This practice is not recommended for diode-type inputs in a noisy environment, since each diode represents a small capacitor and two or more in parallel can act as an entry port for negative spikes superimposed on a HIGH level and cause momentary turn-off of Q2.







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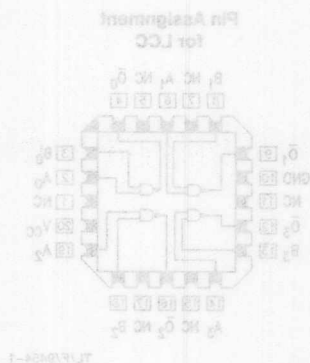
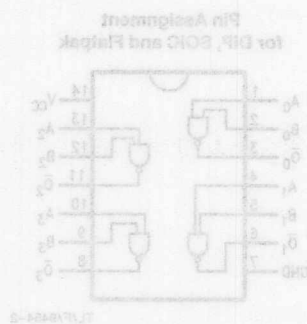
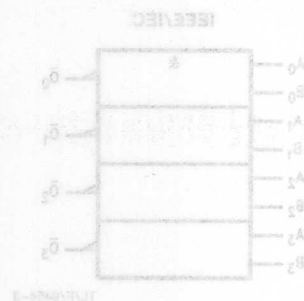
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Ordering Code: See Section 5

Logic Symbol



Unit Loading Fan Out: See Section 5 for U.L. definitions

Pin Name	Description	54F/74F	
		U.L. HIGH/LOW	Input/Output
A <sub>n</sub> , B <sub>n</sub>	Inputs	1.0/1.0	20 μA/1 – 8 mA
O <sub>n</sub>	Outputs	50/33.3	– 1 mA/20 mA





## 54F/74F00 Quad 2-Input NAND Gate

### General Description

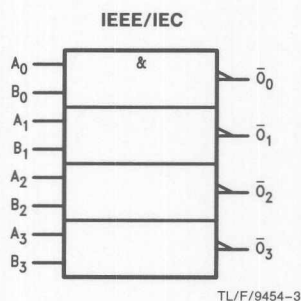
This device contains four independent gates, each of which performs the logic NAND function.

### Features

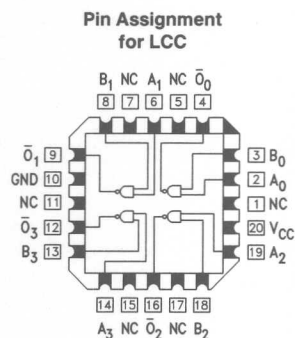
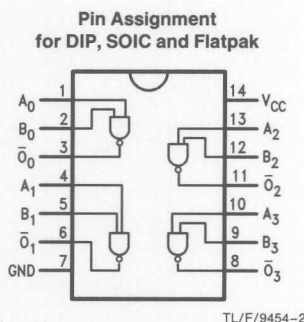
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

### Logic Symbol



### Connection Diagrams



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_n, B_n$	Inputs	1.0/1.0	20 $\mu$ A / -0.6 mA
$O_n$	Outputs	50/33.3	-1 mA / 20 mA

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
---	----------------

Input Voltage (Note 2)	-0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	-30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

ESD Last Passing Voltage (Min)	4000V
--------------------------------	-------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.5 2.7		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All other pins grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All other pins grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		1.9	2.8	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		6.8	10.2	mA	Max	V <sub>O</sub> = LOW

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	2.4	3.7	5.0	2.0	7.0	2.4	6.0		
$t_{PHL}$	$A_n, B_n$ to $\overline{O}_n$	1.5	3.2	4.3	1.5	6.5	1.5	5.3	ns	2-3



## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	−55°C to +125°C
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.5 2.7		V	Min	I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All other pins grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All other pins grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		3.7	5.6	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		8.7	13.0	mA	Max	V <sub>O</sub> = LOW

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{\text{PLH}}$	Propagation Delay	2.5	4.4	5.5	2.5	7.5	2.5	6.5	ns	2–3
$t_{\text{PHL}}$	$A_n, B_n \text{ to } \overline{O}_n$	1.5	3.2	4.3	1.5	6.5	1.5	5.3		



# 54F/74F04

## Hex Inverter

### General Description

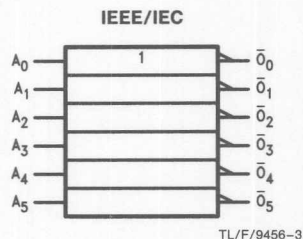
This device contains six independent gates, each of which performs the logic INVERT function.

### Features

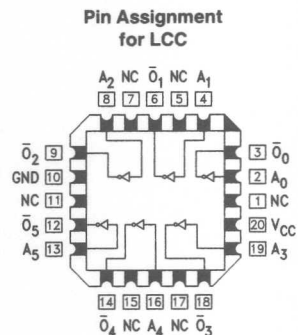
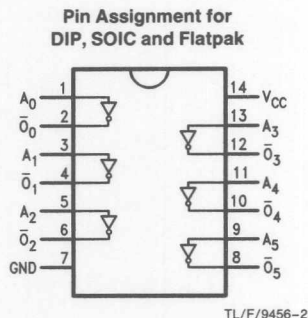
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

### Logic Symbol



### Connection Diagrams



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_n$	Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$O_n$	Outputs	50/33.3	-1 mA/20 mA

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
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Input Voltage (Note 2)	−0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	−30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
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ESD Last Passing Voltage (Min)	4000V
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**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5			V	Min	I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.5					I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>			0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>			0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F			20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F			5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F			100	μA	Max	V <sub>IN</sub> = 7.0V
		74F			7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F			50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All other pins grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All other pins grounded
I <sub>IL</sub>	Input LOW Current				−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60		−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current			2.8	4.2	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			10.2	15.3	mA	Max	V <sub>O</sub> = LOW

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	2.4	3.7	5.0	2.0	7.0	2.4	6.0	ns	2-3
$t_{PHL}$	$A_n$ to $\overline{O}_n$	1.5	3.2	4.3	1.5	6.5	1.5	5.3		

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Note 3: ESD Last Passing Voltage (Min) 4000V

Current Applied to Output in LOW State (Max) twice the rated  $I_{OL}$  (mA)

TRI-STATE® Output Standard Output in HIGH State (with  $V_{CC} = 0\text{V}$ ) Voltage Applied to Output Input Current (Note 2) -80 mA to +8.0 mA

## DC Electrical Characteristics

Symbol	Parameter	74F/54F			Units	$V_{CC}$	Conditions
		Min	Typ	Max			
$V_{IH}$	Input HIGH Voltage	2.0			V		Recognized as a HIGH signal
$V_{IL}$	Input LOW Voltage	0.8			V		Recognized as a LOW signal
$V_{CD}$	Input Clamp Diode Voltage	-1.5			V	Min	$I_{IN} = -18\text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.7	2.5	2.5	V	Min	$I_{OH} = -1\text{ mA}$ $I_{OH} = -1\text{ mA}$ $I_{OH} = -1\text{ mA}$
$V_{OL}$	Output LOW Voltage	0.5	0.5	0.5	V	Min	$I_{OL} = 20\text{ mA}$ $I_{OL} = 20\text{ mA}$
$I_{IH}$	Input HIGH Current	24F	20.0	20.0	$\mu\text{A}$	Max	$V_{IN} = 2.7\text{V}$
$I_{IHL}$	Input HIGH Current Breakdown Test	24F	100	7.0	$\mu\text{A}$	Max	$V_{IN} = 7.0\text{V}$
$I_{OEH}$	Output HIGH Leakage Current	24F	250	50	$\mu\text{A}$	Max	$V_{OUT} = V_{CC}$
$V_{ID}$	Input Leakage Test	24F	4.75		V	0.0	$I_D = 1.9\text{ mA}$ All other pins grounded
$I_{OD}$	Output Leakage Current	24F	3.75		$\mu\text{A}$	0.0	$V_{OD} = 1.60\text{ mV}$ All other pins grounded
$I_{IL}$	Input LOW Current	-0.8			mA	Max	$V_{IN} = 0.2\text{V}$
$I_{OSH}$	Output Short-Circuit Current	-80			mA	Max	$V_{OUT} = 0\text{V}$
$I_{OCH}$	Power Supply Current	2.8	4.2		mA	Max	$V_O = \text{HIGH}$
$I_{OCL}$	Power Supply Current	10.2	18.9		mA	Max	$V_O = \text{LOW}$



# 54F/74F08 Quad 2-Input AND Gate

## General Description

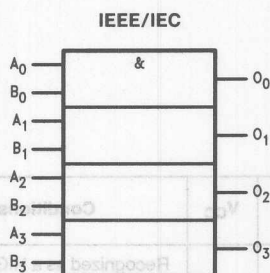
This device contains four independent gates, each of which performs the logic AND function.

## Features

- Guaranteed 4000V minimum ESD protection

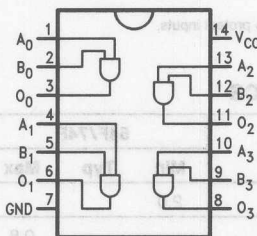
**Ordering Code:** See Section 5

## Logic Symbol



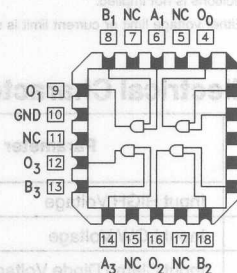
TL/F/9457-3

## Pin Assignment for DIP, SOIC and Flatpak



TL/F/9457-2

## Pin Assignment for LCC



TL/F/9457-1

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_n, B_n$	Inputs	1.0/1.0	20 $\mu$ A / -0.6 mA
$O_n$	Outputs	50/33.3	-1 mA / 20 mA

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA

Voltage Applied to Output

in HIGH State (with V<sub>CC</sub> = 0V)

Standard Output -0.5V to V<sub>CC</sub>

TRI-STATE® Output -0.5V to +5.5V

Current Applied to Output

in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

ESD Last Passing Voltage (Min) 4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	-55°C to +125°C
Military	0°C to +70°C
Commercial	
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F	20.0		μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F	100		μA	Max	V <sub>IN</sub> = 7.0V
		74F	7.0				
I <sub>CEX</sub>	Output HIGH Leakage Current	54F	250		μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F	50				
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		5.5	8.3	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		8.6	12.9	mA	Max	V <sub>O</sub> = LOW

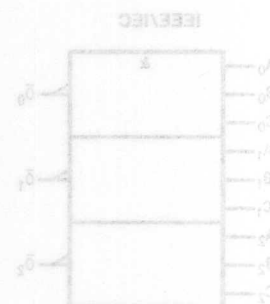
**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	3.0	4.2	5.6	2.5	7.5	3.0	6.6	ns	2-3
$t_{PHL}$	$A_n, B_n$ to $O_n$	2.5	4.0	5.3	2.0	7.5	2.5	6.3		

This device contains three independent gates, each of which performs the logic NAND function.

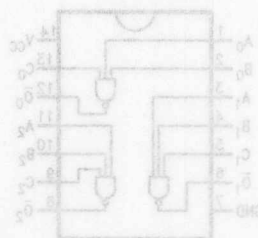
Ordering Code: See Section 2

Logic Symbol



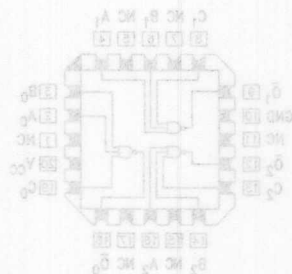
TLF1288-2

Pin Assignment for DIP, SOIC and Flatpak



TLF1288-3

Pin Assignment for LCC



TLF1288-1

Unit Loading Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	74F00	
		U.L.	Input/Output
$A_n, B_n, C_n$	Inputs	10/1.0	20 pA - 0.5 mA
$O_n$	Outputs	50/33.3	-1 mA/50 mA





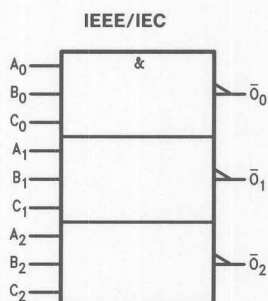
## 54F/74F10 Triple 3-Input NAND Gate

### General Description

This device contains three independent gates, each of which performs the logic NAND function.

### Ordering Code: See Section 5

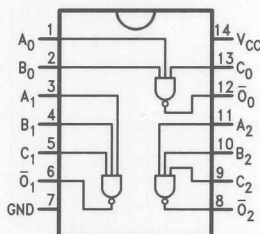
### Logic Symbol



TL/F/9458-3

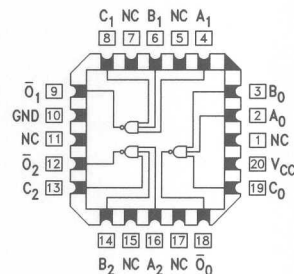
### Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak



TL/F/9458-2

Pin Assignment  
for LCC



TL/F/9458-1

### Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_n, B_n, C_n$	Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$O_n$	Outputs	50/33.3	-1 mA/20 mA

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
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Input Voltage (Note 2)	–0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	–30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	–0.5V to V <sub>CC</sub>
TRI-STATE® Output	–0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	–55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				–1.2	V	Min	I <sub>IN</sub> = –18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5			V	Min	I <sub>OH</sub> = –1 mA
		74F 10% V <sub>CC</sub>	2.5					I <sub>OH</sub> = –1 mA
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = –1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>			0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>			0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F			20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F			100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F			250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All other pins grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All other pins grounded
I <sub>IL</sub>	Input LOW Current				–0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		–60		–150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current			1.4	2.1	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			5.1	7.7	mA	Max	V <sub>O</sub> = LOW

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	2.4	3.7	5.0	2.0	7.0	2.4	6.0		
t <sub>PHL</sub>	A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> to $\overline{O}_n$	1.5	3.2	4.3	1.5	6.5	1.5	5.3	ns	2-3



Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V

Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All other pins grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All other pins grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		4.1	6.2	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		6.5	9.7	mA	Max	V <sub>O</sub> = LOW

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	3.0	4.2	5.6	2.5	7.5	3.0	6.6	ns	2-3
$t_{PHL}$	$A_n, B_n, C_n$ to $O_n$	2.5	4.1	5.5	2.0	7.5	2.5	6.5		

The 74F contains two 4-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, filtered output signals. In addition, they have a greater noise margin than conventional NAND gates.

Each circuit contains a 4-input Schmitt trigger followed by level shifting circuitry and a standard FAST<sup>®</sup> output structure.

## Features

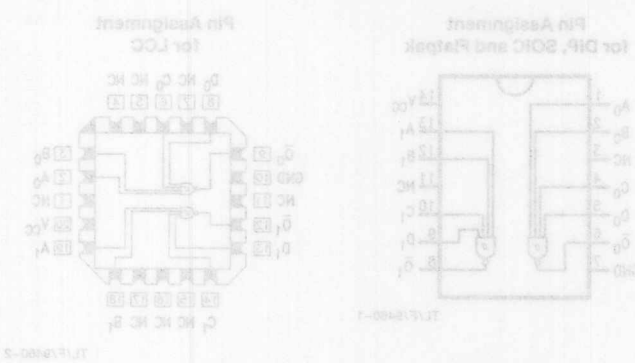
■ Guaranteed 4000V minimum ESD protection

Ordering Code: See Section 5

## Logic Symbol



## Connection Diagrams



Unit Loading/Fan Out: See Section 3 for U.L. definitions

Pin Names	Description	74F04	
		U.L.	Input/Output
$A_n, B_n, C_n, D_n$	Inputs	1.0/1.0	50 $\mu\text{A}$ / -0.8 mA
$O_n$	Outputs	50/33.3	-1 mA / 50 mA

## Function Table

Output	Inputs			
	A	B	C	D
Y	L	X	X	X
	X	L	X	X
	X	X	L	X
	X	X	X	L
	H	H	H	H

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Indifferent




**54F/74F13**

## Dual 4-Input NAND Schmitt Trigger

### General Description

The 'F13 contains two 4-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional NAND gates.

Each circuit contains a 4-input Schmitt trigger followed by level shifting circuitry and a standard FAST® output struc-

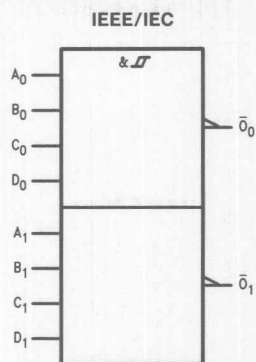
ture. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive- and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800 mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

### Features

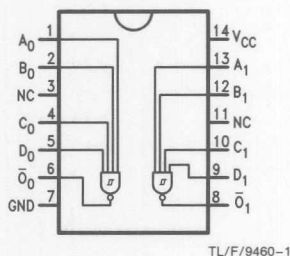
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

### Logic Symbol

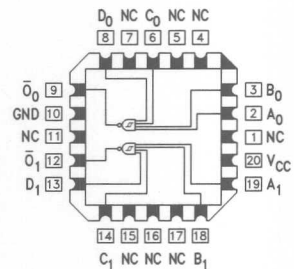


Pin Assignment  
for DIP, SOIC and Flatpak



### Connection Diagrams

Pin Assignment  
for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_n, B_n, C_n, D_n$	Inputs	1.0/1.0	20 $\mu$ A / -0.6 mA
$O_n$	Outputs	50/33.3	-1 mA / 20 mA

Function Table

Inputs				Output
A	B	C	D	$\bar{O}$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
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Input Voltage (Note 2)	−0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	−30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
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ESD Last Passing Voltage (Min)	4000V
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**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>T+</sub>	Positive-Going Threshold		1.5		2.0	V	5.0	
V <sub>T−</sub>	Negative-Going Threshold		0.7		1.1	V	5.0	
ΔV <sub>T</sub>	Hysteresis (V <sub>T+</sub> − V <sub>T−</sub> )		0.4		—	V	5.0	
V <sub>CD</sub>	Input Clamp Diode Voltage				−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.5 2.7			V	Min	I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>			0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F			20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F			100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F			250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current				−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60		−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current			4.5	8.5	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			7.0	10.0	mA	Max	V <sub>O</sub> = LOW

Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	5.0		10.5	3.0	16.0	4.5	12.0	ns	2-3
$t_{PHL}$	$A_n, B_n, C_n, D_n \text{ to } \bar{O}_n$	9.5		17.5	8.5	22.0	9.5	18.5		

Note 1: ESD limit is applicable to protect inputs.

Note 2: ESD limit is applicable to protect inputs.

Note 3: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not limited.

Note 4: Input current (Note 2) is  $-35\text{ mA}$  to  $+5.0\text{ mA}$ .

Note 5: Voltage Applied to Output in HIGH State with  $V_{CC} = 0\text{V}$  is  $-0.5\text{ V}$  to  $V_{CC}$ .

Note 6: TRI-STATE Output is  $-0.5\text{ V}$  to  $+0.5\text{ V}$ .

Note 7: Current Applied to Output in LOW State (Max) is twice the rated IOL (mA).

Note 8: ESD Last Remaining Voltage (Min) is  $4000\text{ V}$ .

### DC Electrical Characteristics

Symbol	Parameter	Test Type			Units	$V_{CC}$	Conditions
		Min	Typ	Max			
$V_{T+}$	Positive-Going Threshold	1.5		2.0	V	5.0	
$V_{T-}$	Negative-Going Threshold	0.7		1.1	V	5.0	
$\Delta V_T$	Hysteresis ( $V_{T+} - V_{T-}$ )	0.4		—	V	5.0	
$V_{OD}$	Input Clamp Diode Voltage	-1.2		—	V	Min	$I_{IN} = -18\text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.5		2.5	V	Min	$I_{OH} = -1\text{ mA}$ $I_{OL} = -1\text{ mA}$ $I_{OH} = -1\text{ mA}$
$V_{OL}$	Output LOW Voltage	0.2		0.2	V	Min	$I_{OL} = 20\text{ mA}$ $I_{OL} = 20\text{ mA}$
$I_{IH}$	Input HIGH Current	245		20.0	$\mu\text{A}$	Max	$V_{IN} = 2.7\text{ V}$
$I_{IL}$	Input LOW Current	245		100	$\mu\text{A}$	Max	$V_{IN} = 7.0\text{ V}$
$I_{EX}$	Output HIGH Leakage Current	245		250	$\mu\text{A}$	Max	$V_{OUT} = V_{CC}$
$V_{IO}$	Input Leakage Test	245		4.75	V	0.0	$I_D = 1.9\text{ mA}$ All Other Pins Grounded
$I_{OP}$	Output Leakage Current	245		2.75	$\mu\text{A}$	0.0	$V_{OD} = 150\text{ mV}$ All Other Pins Grounded
$I_{IL}$	Input LOW Current	-0.8		—	$\text{mA}$	Max	$V_{IN} = 0.5\text{ V}$
$I_{OS}$	Output Short-Circuit Current	-80		-150	$\text{mA}$	Max	$V_{OUT} = 0\text{ V}$
$I_{CH}$	Power Supply Current	4.5		8.5	$\text{mA}$	Max	$V_O = \text{HIGH}$
$I_{CL}$	Power Supply Current	7.0		10.0	$\text{mA}$	Max	$V_O = \text{LOW}$

# 54F/74F14

## Hex Inverter Schmitt Trigger

### General Description

The 'F14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feed back to

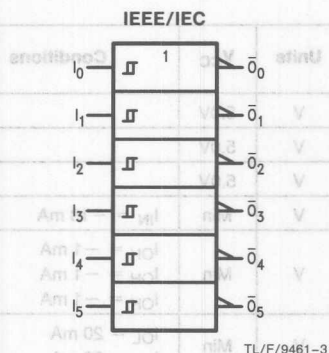
effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

### Features

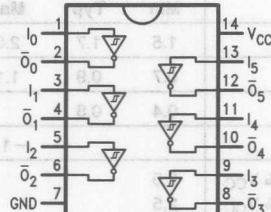
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

### Logic Symbol

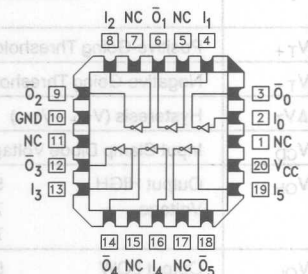


**Pin Assignment  
DIP, SOIC and Flatpak**



### Connection Diagrams

**Pin Assignment  
for LCC**



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$I_n$	Input	1.0/1.0	20 $\mu$ A / -0.6 mA
$O_n$	Output	50/33.3	-1 mA / 20 mA

**Function Table**

Input	Output
A	$\bar{O}$
L	H
H	L

H = HIGH Voltage Level  
L = LOW Voltage Level

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	–0.5V to V <sub>CC</sub>
TRI-STATE® Output	–0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	–55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>T+</sub>	Positive-Going Threshold	1.5	1.7	2.0	V	5.0V	
V <sub>T–</sub>	Negative-Going Threshold	0.7	0.9	1.1	V	5.0V	
ΔV <sub>T</sub>	Hysteresis (V <sub>T+</sub> – V <sub>T–</sub> )	0.4	0.8		V	5.0V	
V <sub>CD</sub>	Input Clamp Diode Voltage			–1.2	V	Min	I <sub>IN</sub> = –18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = –1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = –1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = –1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	Max	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			–0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		–60	–150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current			25	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			25	mA	Max	V <sub>O</sub> = LOW

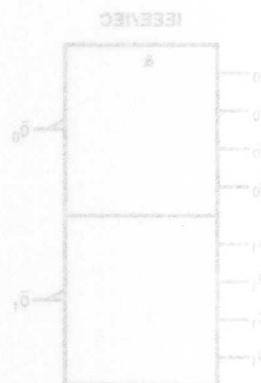
# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	4.0	10.5	4.0	14.0	4.0	11.5	ns	2-3
$t_{PHL}$	$I_n \rightarrow \overline{O}_n$	3.5	8.5	3.5	10.0	3.5	9.0		

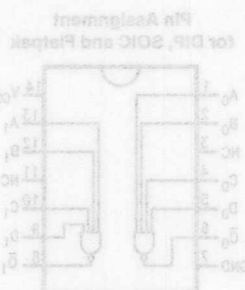
This device contains two independent gates, each of which performs the logic NAND function.

Ordering Code: See Section 2

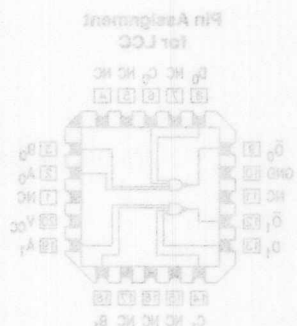
Logic Symbol



74F00-8



74F00-5



74F00-1

Unit Loading/Fan Out: See Section 2 for U.I. definitions

Pin Names	Description	74F00	
		U.I.	Input/Output
$A_1, A_2, C_1, D_1$	Inputs	1.0/1.0	50 $\mu\text{A}$ - 0.8 mA
$O_1$	Outputs	80/23.3	- 1 mA/50 mA





## 54F/74F20

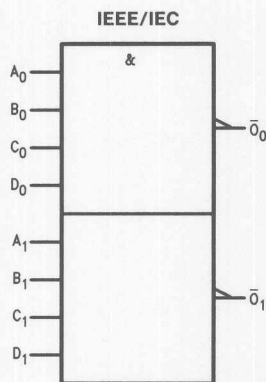
### Dual 4-Input NAND Gate

#### General Description

This device contains two independent gates, each of which performs the logic NAND function.

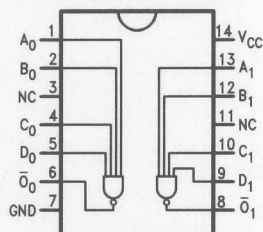
**Ordering Code:** See Section 5

#### Logic Symbol



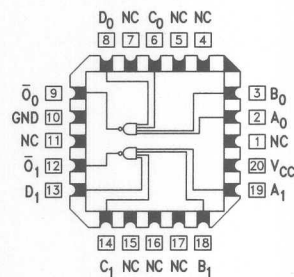
TL/F/9462-3

**Pin Assignment  
for DIP, SOIC and Flatpak**



TL/F/9462-2

**Pin Assignment  
for LCC**



TL/F/9462-1

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_n, B_n, C_n, D_n$ $\bar{O}_n$	Inputs Outputs	1.0/1.0 50/33.3	20 $\mu A$ / -0.6 mA -1 mA/20 mA

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V

Input Current (Note 2)	–30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	–0.5V to V <sub>CC</sub>
Standard Output	–0.5V to V <sub>CC</sub>
TRI-STATE® Output	–0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	–55°C to +125°C
Military	–55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			–1.2	V	Min	I <sub>IN</sub> = –18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = –1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = –1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = –1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All other pins grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All other pins grounded
I <sub>IL</sub>	Input LOW Current			–0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		–60	–150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		0.9	1.4	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		3.4	5.1	mA	Max	V <sub>O</sub> = LOW

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	2.4	3.7	5.0	2.0	7.0	2.4	6.0	ns	2-3
t <sub>PHL</sub>	A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> , D <sub>n</sub> to $\overline{O}_n$	1.5	3.2	4.3	1.5	6.5	1.5	5.3		

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or from the useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect input.

Current Applied to Output in LOW State (I<sub>OL</sub>) (mA)

TRI-STATE Output

Standard Output

Voltage Applied to Output in HIGH State (with V<sub>CC</sub> = 0V)

Input Current (Note 2)

Am 0.5 to +5.0 mA

## DC Electrical Characteristics

Symbol	Parameter	74F/54F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH signal
V <sub>IL</sub>	Input LOW Voltage	0.8			V		Recognized as a LOW signal
V <sub>OD</sub>	Input Clamp Diode Voltage	-1.2			V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	5.5			V	Min	I <sub>OH</sub> = -1 mA
		5.5					I <sub>OH</sub> = -1 mA
		5.7					I <sub>OH</sub> = -1 mA
		5.5					I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	0.5			V	Min	I <sub>OL</sub> = 20 mA
		0.5					I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	2.0			μA	Max	V <sub>IH</sub> = 2.7V
		2.0					V <sub>IH</sub> = 2.7V
I <sub>OH</sub>	Input HIGH Current	100			μA	Max	V <sub>IH</sub> = 2.0V
		7.0					V <sub>IH</sub> = 2.0V
I <sub>OH</sub>	Output HIGH Leakage Current	250			μA	Max	V <sub>OH</sub> = V <sub>CC</sub>
		80					V <sub>OH</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.5 μA All other pins grounded
I <sub>OD</sub>	Output Leakage	3.75			μA	0.0	V <sub>OD</sub> = 150 mV All other pins grounded
I <sub>IL</sub>	Input LOW Current	-0.8			mA	Max	V <sub>IL</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-150			mA	Max	V <sub>OH</sub> = 0V
I <sub>CC1</sub>	Power Supply Current	0.9			mA	Max	V <sub>O</sub> = HIGH
I <sub>CC2</sub>	Power Supply Current	3.4			mA	Max	V <sub>O</sub> = LOW



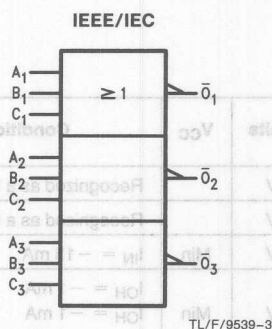
# 54F/74F27 Triple 3-Input NOR Gate

## General Description

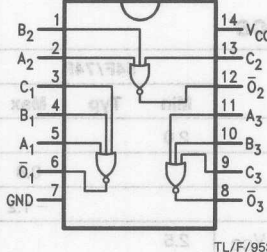
This device contains three independent gates, each of which performs the logic NOR function.

**Ordering Code:** See Section 5

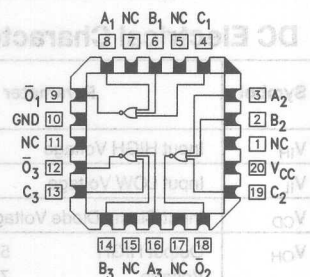
## Logic Symbol



## Pin Assignment for DIP, SOIC and Flatpak



## Pin Assignment for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_n, B_n, C_n$	Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$O_n$	Data Outputs	50/33.3	-1 mA/20 mA

Function Table

Inputs			Output
$A_n$	$B_n$	$C_n$	$O_n$
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

**Office/Distributors for availability and specifications.**

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA

**Voltage Applied to Output**

 in HIGH State (with V<sub>CC</sub> = 0V)

Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V

**Current Applied to Output**

 in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		4.0	5.5	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		8.7	12.0	mA	Max	V <sub>O</sub> = LOW







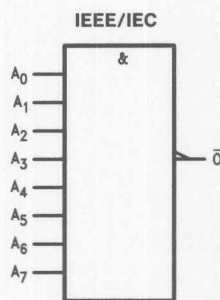
## 54F/74F30 8-Input NAND Gate

### General Description

This device contains a single gate, which performs the logic NAND function.

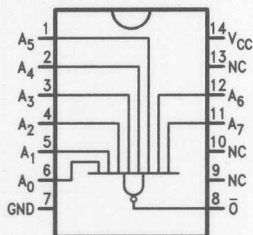
**Ordering Code:** See Section 5

### Logic Symbol



TL/F/9560-4

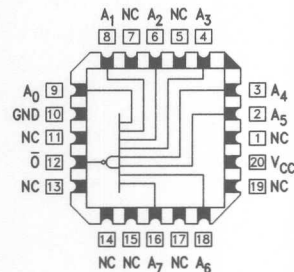
**Pin Assignment  
for DIP, Flatpak and SOIC**



TL/F/9560-1

### Connection Diagrams

**Pin Assignment  
for LCC**



TL/F/9560-2

**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
A <sub>0</sub> –A <sub>7</sub>	Inputs	1.0/1.0	20 $\mu$ A/ –0.6 mA
$\bar{O}$	Output	50/33.3	–1 mA/20 mA

**Function Table**

Inputs								Output
A0	A1	A2	A3	A4	A5	A6	A7	$\bar{O}$
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V

Input Current (Note 2)	–30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	–0.5V to V <sub>CC</sub>
TRI-STATE® Output	–0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
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**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	–55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			–1.2	V	Min	I <sub>IN</sub> = –18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = –1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = –1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = –1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			–0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		–60	–150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		0.5	1.5	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			4.5	mA	Max	V <sub>O</sub> = LOW

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	1.0	3.7	5.0			1.0	5.5		
t <sub>PHL</sub>	A <sub>n</sub> to $\bar{O}$	1.5	2.8	5.0			1.5	5.5	ns	2-3



## 54F/74F32 Quad 2-Input OR Gate

### General Description

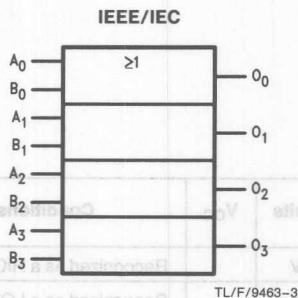
This device contains four independent gates, each of which performs the logic OR function.

### Features

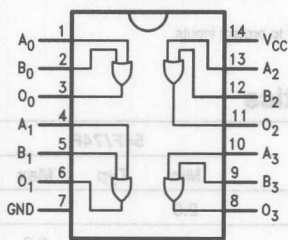
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

### Logic Symbol

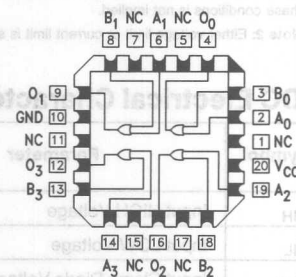


### Pin Assignment for DIP, SOIC and Flatpak



### Connection Diagrams

### Pin Assignment for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I <sub>IH</sub> /I <sub>IL</sub> Output I <sub>OH</sub> /I <sub>OL</sub>
A <sub>n</sub> , B <sub>n</sub>	Inputs	1.0/1.0	20 $\mu$ A / -0.6 mA
O <sub>n</sub>	Outputs	50/33.3	-1 mA/20 mA

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA

### Voltage Applied to Output

in HIGH State (with V<sub>CC</sub> = 0V)

Standard Output -0.5V to V<sub>CC</sub>

TRI-STATE® Output -0.5V to +5.5V

### Current Applied to Output

in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

ESD Last Passing Voltage (Min) 4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature

Military -55°C to +125°C

Commercial 0°C to +70°C

Supply Voltage

Military +4.5V to +5.5V

Commercial +4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.5 2.7		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		6.1	9.2	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		10.3	15.5	mA	Max	V <sub>O</sub> = LOW

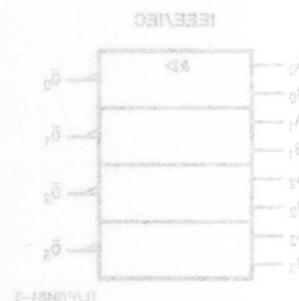
**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	3.0	4.2	5.6	3.0	7.5	3.0	6.6	ns	2-3
$t_{PHL}$	$A_n, B_n$ to $O_n$	3.0	4.0	5.3	2.5	7.5	3.0	6.3		

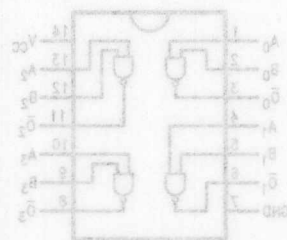
This device contains four independent gates, each of which performs the logic NAND function.

Ordering Code: See Section 5

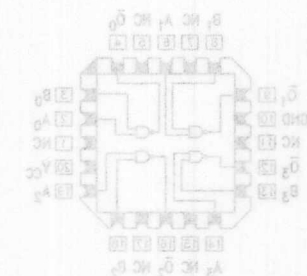
Logic Symbol



Pin Assignment  
for DIP, SOIC and Pinpak



Pin Assignment  
for LCC



Unit Loading/Fan Out: See Section 5 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L.	Input/Output
$A_n, B_n$	Inputs	1.0/5.0	20 $\mu\text{A}$ / -1.2 mA
$O_n$	Outputs	800/108.8 (80)	-12 mA/84 mA (48 mA)

Function Table

Output	Inputs	
	A	B
H	H	H
H	H	L
H	L	H
H	L	L
L	H	H
L	H	L
L	L	H
L	L	L

H = HIGH Voltage Level  
L = LOW Voltage Level




**54F/74F37**

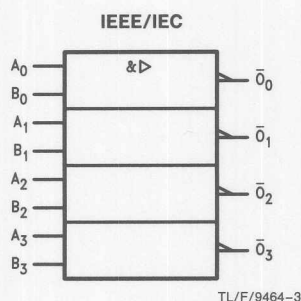
## Quad Two-Input NAND Buffer

### General Description

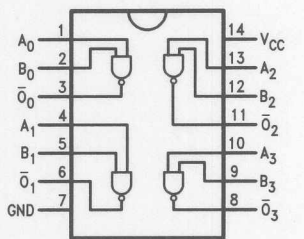
This device contains four independent gates, each of which performs the logic NAND function.

**Ordering Code:** See Section 5

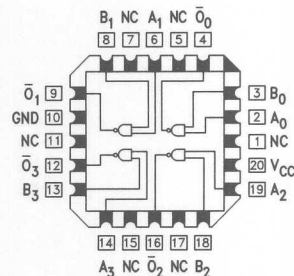
### Logic Symbol



Pin Assignment  
for DIP, SOIC and Flatpak



Pin Assignment  
for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_n, B_n$ $\bar{O}_n$	Inputs Outputs	1.0/2.0 600/106.6 (80)	20 $\mu A$ / -1.2 mA -12 mA/64 mA (48 mA)

Function Table

Inputs		Output
A	B	$\bar{O}$
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
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**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	−55°C to +125°C
Military	0°C to +70°C
Commercial	
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.4		V	Min	I <sub>OH</sub> = −3 mA
		54F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = −12 mA
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = −15 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.55	V	Min	I <sub>OL</sub> = 48 mA
		74F 10% V <sub>CC</sub>		0.55			I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
	74F			5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
	74F			7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
	74F			50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−1.2	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	−100		−225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		3.7	6.0	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		28.0	33.0	mA	Max	V <sub>O</sub> = LOW

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	2.0	3.2	5.5			1.5	6.5		2-3
t <sub>PHL</sub>	A <sub>n</sub> , B <sub>n</sub> to $\overline{O}_n$	1.5	2.4	4.5			1.0	5.0	ns	

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Note 3: Current Applied to Output  
Standard Output  
in HIGH State (with V<sub>CC</sub> = 0V)  
Voltage Applied to Output  
Input Current (Note 2)  
– 30 mA to +5.0 mA

## DC Electrical Characteristics

Symbol	Parameter	74F/54F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage		0.8		V		Recognized as a LOW Signal
V <sub>CC</sub>	Input Clamp Diode Voltage		–1.2		V	Min	I <sub>IN</sub> = –18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7 2.4 2.0 2.4 2.0 2.0			V	Min	I <sub>OH</sub> = –3 mA I <sub>OH</sub> = –12 mA I <sub>OH</sub> = –3 mA I <sub>OH</sub> = –12 mA I <sub>OH</sub> = –3 mA I <sub>OH</sub> = –12 mA
V <sub>OL</sub>	Output LOW Voltage	0.25 0.25			V	Min	I <sub>OL</sub> = 48 mA I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current	24F 24F	20.0 8.0		μA	Max	V <sub>IH</sub> = 2.7V
I <sub>IHL</sub>	Input HIGH Current Breakdown Test	24F 24F	100 7.0		μA	Max	V <sub>IH</sub> = 7.0V
I <sub>CCX</sub>	Output HIGH Leakage Current	24F 24F	280 50		μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>IO</sub>	Input Leakage Test	24F	4.75		V	0.0	I <sub>IO</sub> = 1.5 μA All Other Pins Grounded
I <sub>CO</sub>	Output Leakage Current	24F	3.75		μA	0.0	V <sub>IO</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current		–1.2		mA	Max	V <sub>IH</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		–100		mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		8.7		mA	Max	V <sub>O</sub> = HIGH
I <sub>CL</sub>	Power Supply Current		28.0		mA	Max	V <sub>O</sub> = LOW



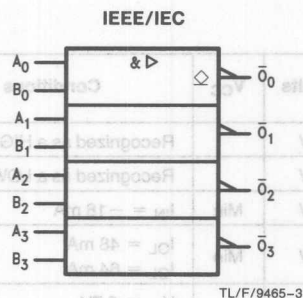
# 54F/74F38 Quad Two-Input NAND Buffer (Open Collector)

## General Description

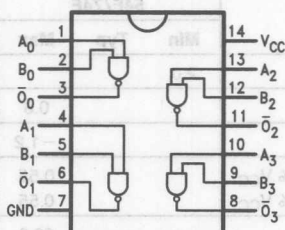
This device contains four independent gates, each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

**Ordering Code:** See Section 5

## Logic Symbol

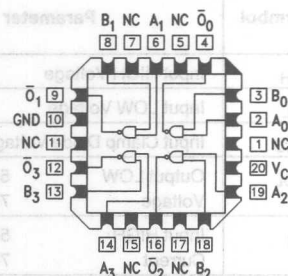


Pin Assignment  
for DIP, SOIC and Flatpak



TL/F/9465-1

Pin Assignment  
for LCC



TL/F/9465-2

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_n, B_n$	Inputs	1.0/2.0	20 $\mu$ A / -1.2 mA
$\bar{O}_n$	Outputs	OC* / 106.6 (80)	OC* / 64 mA (48 mA)

\*OC = Open Collector

Function Table

Inputs		Output
A	B	$\bar{O}$
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

**Office/Distributors for availability and specifications.**

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
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**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Free Air Ambient Temperature**

Military	−55°C to +125°C
Commercial	0°C to +70°C

**Supply Voltage**

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.55	V	Min	I <sub>OL</sub> = 48 mA I <sub>OL</sub> = 64 mA
				0.55			
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
				5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100	μA	Max	V <sub>IN</sub> = 7.0V
				7.0			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−1.2	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OHC</sub>	Open Collector, Output OFF Leakage Test			250	μA	Min	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>CCH</sub>	Power Supply Current		2.1	7.0	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		26.0	30.0	mA	Max	V <sub>O</sub> = LOW

Inputs	Outputs
A	B
H	L
H	H
H	L
L	H

H = HIGH Voltage Level  
L = LOW Voltage Level

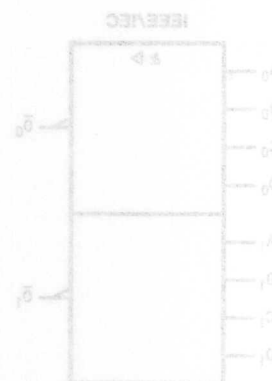
**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	6.5	9.7	12.5	6.5	14.5	6.5	13.0	ns	2-3
$t_{PHL}$	$A_n, B_n$ to $\overline{O}_n$	1.0	2.1	5.0	1.0	5.5	1.0	5.5		

This device contains two independent gates, each of which performs the logic NAND function.

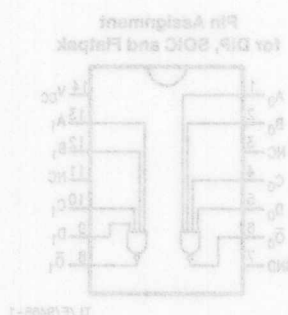
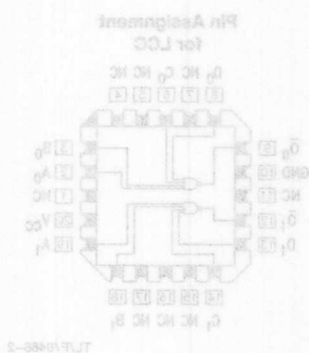
Ordering Code: See Section 2

Logic Symbol



TL7F10AB-3

Connection Diagrams



Unit Loading Fan Out: See Section 2 for U.L. definitions

Pin Name	Description	U.L.	Input Fan Out
$A_n, B_n, C_n, D_n$	Inputs	1.0/2.0	20 $\mu\text{A}$ / 1.5 mA
$\bar{O}_n$	Outputs	600/100 (80)	15 mA/8 mA (48 mA)

Function Table

Inputs	A	B	C	D	Output
L	X	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

H = HIGH Voltage Level  
L = LOW Voltage Level

X = Indifferent





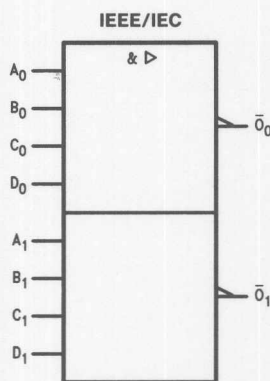
## 54F/74F40 Dual 4-Input NAND Buffer

### General Description

This device contains two independent gates, each of which performs the logic NAND function.

**Ordering Code:** See Section 5

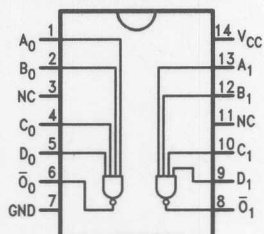
### Logic Symbol



TL/F/9466-3

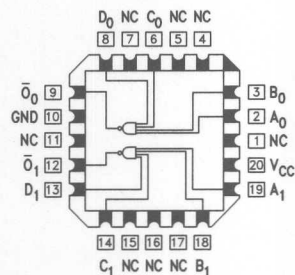
### Connection Diagrams

Pin Assignment  
for DIP, SOIC and Flatpak



TL/F/9466-1

Pin Assignment  
for LCC



TL/F/9466-2

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_n, B_n, C_n, D_n$ $\bar{O}_n$	Inputs Outputs	1.0/2.0 600/106.6 (80)	20 $\mu$ A/ - 1.2 mA - 12 mA/64 mA (48 mA)

Function Table

Inputs				Output
A	B	C	D	$\bar{O}$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

## Absolute Maximum Ratings (Note 1) Recommended Operating Conditions

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
---	----------------

Input Voltage (Note 2)	-0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	-30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

Free Air Ambient Temperature

Military -55°C to +125°C

Commercial 0°C to +70°C

Supply Voltage

Military +4.5V to +5.5V

Commercial +4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.4			V	Min	I <sub>OH</sub> = -3 mA
		54F 10% V <sub>CC</sub>	2.0					I <sub>OH</sub> = -12 mA
		74F 10% V <sub>CC</sub>	2.4					I <sub>OH</sub> = -3 mA
		74F 10% V <sub>CC</sub>	2.0					I <sub>OH</sub> = -15 mA
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = -3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>			0.55	V	Min	I <sub>OL</sub> = 48 mA
		74F 10% V <sub>CC</sub>			0.55			I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current	54F			20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F			5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F			100	μA	Max	V <sub>IN</sub> = 7.0V
		74F			7.0			
I <sub>CEX</sub>	Output High Leakage Current	54F			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F			50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current				-1.2	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-100		-225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current			1.6	4.0	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			13.0	17.0	mA	Max	V <sub>O</sub> = LOW

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	2.0	3.0	6.0			1.5	7.0		2-3
$t_{PHL}$	$A_n, B_n, C_n, D_n$ to $\bar{O}_n$	1.5	2.5	5.0			1.0	5.5	ns	

Note 1: Absolute maximum ratings and values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

Current Applied to Output in LOW State (Max)

TRI-STATE<sup>®</sup> Output

Standard Output

Voltage Applied to Output in HIGH State (with  $V_{CC} = 0\text{V}$ )

Input Current (Note 2)

Input Voltage (Note 2)

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	$V_{CC}$	Conditions
		Min	Typ	Max			
$V_{IH}$	Input HIGH Voltage	2.0			V		Recognized as a HIGH signal
$V_{IL}$	Input LOW Voltage	0.8			V		Recognized as a LOW signal
$V_{CD}$	Input Clamp Diode Voltage	-1.2			V	Min	$I_{IN} = -18\text{mA}$
$V_{OH}$	Output HIGH Voltage	2.4			V	Min	$I_{OH} = -3\text{mA}$
		2.0					$I_{OH} = -12\text{mA}$
		2.4					$I_{OH} = -3\text{mA}$
		2.0					$I_{OH} = -12\text{mA}$
		2.7					$I_{OH} = -3\text{mA}$
$V_{OL}$	Output LOW Voltage	0.25			V	Min	$I_{OL} = 48\text{mA}$
		0.55					$I_{OL} = 84\text{mA}$
$I_{IH}$	Input HIGH Current	20.0			$\mu\text{A}$	Max	$V_{IN} = 2.7\text{V}$
		5.0					
$I_{BI}$	Input HIGH Current Breakdown Test	100			$\mu\text{A}$	Max	$V_{IN} = 7.0\text{V}$
		7.0					
$I_{OEX}$	Output High Leakage Current	350			$\mu\text{A}$	Max	$V_{OUT} = V_{CC}$
		50					
$I_{IP}$	Input Leakage Test	4.75			V	0.0	$I_{IN} = 1.8\text{mA}$ All Other Pins Grounded
$I_{OP}$	Output Leakage Circuit Current	3.75			$\mu\text{A}$	0.0	$V_{OD} = 150\text{mV}$ All Other Pins Grounded
$I_{IL}$	Input LOW Current	-1.2			mA	Max	$V_{IN} = 0.5\text{V}$
$I_{OS}$	Output Short-Circuit Current	-100			mA	Max	$V_{OUT} = 0\text{V}$
$I_{CCH}$	Power Supply Current HIGH	1.8			mA	Max	$V_{O} = \text{HIGH}$
$I_{CCL}$	Power Supply Current LOW	13.0			mA	Max	$V_{O} = \text{LOW}$



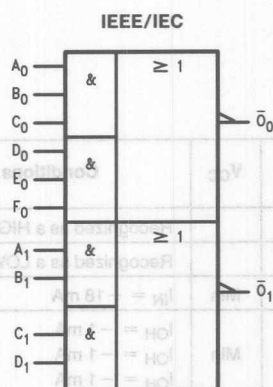
# 54F/74F51 2-2-2-3 AND-OR-Invert Gate

## General Description

This device contains two independent logic units, one performing a 2-2 AND-OR-INVERT and the other performing a 3-3 AND-OR-INVERT function.

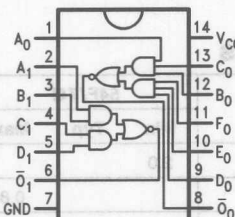
**Ordering Code:** See Section 5

## Logic Symbol



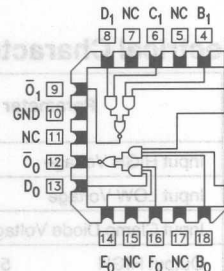
TL/F/9468-4

## Pin Assignment for DIP, SOIC and Flatpak



TL/F/9468-2

## Pin Assignment for LCC



TL/F/9468-1

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L.	Input I <sub>IH</sub> /I <sub>IL</sub> Output I <sub>OH</sub> /I <sub>OL</sub>
A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> , D <sub>n</sub> , E <sub>n</sub> , F <sub>n</sub>	Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
O <sub>n</sub>	Outputs	50/33.3	-1 mA/20 mA

## Function Table for 3-Input Gates

Inputs						Output O <sub>0</sub>
A <sub>0</sub>	B <sub>0</sub>	C <sub>0</sub>	D <sub>0</sub>	E <sub>0</sub>	F <sub>0</sub>	
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

## Function Table for 2-Input Gates

Inputs				Output O <sub>1</sub>
A <sub>1</sub>	B <sub>1</sub>	C <sub>1</sub>	D <sub>1</sub>	
H	H	X	X	L
X	X	H	H	L
All other combinations				H

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA

Voltage Applied to Output in HIGH State (with V<sub>CC</sub> = 0V)

Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output

in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature

Military	-55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5			V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5					I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>			0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>			0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F			20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F			5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F			100	μA	Max	V <sub>IN</sub> = 7.0V
		74F			7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F			50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All other pins grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All other pins grounded
I <sub>IL</sub>	Input LOW Current				-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current			1.9	3.0	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			5.3	8.5	mA	Max	V <sub>O</sub> = LOW

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Indeterminate

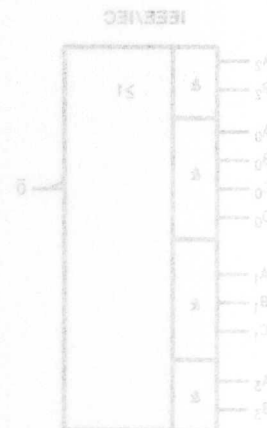
# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Comm}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	2.0	3.7	6.0			1.5	6.5	ns	2-3
$t_{PHL}$	$A_n, B_n, C_n, D_n, E_n, F_n \text{ to } \overline{O}_n$	1.0	2.6	4.0			1.0	4.5		

This device contains gates configured to perform a 4-3-2 input AND-OR-INVERT function.

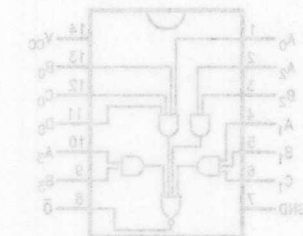
Ordering Code: See Section 5

Logic Symbol



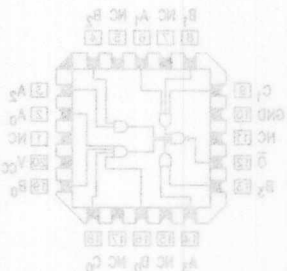
74F00-2

Pin Assignment for DIP, SOIC and Flatpak



74F00-3

Pin Assignment for LCC



74F00-4

Unit Loading/Fan Out: See Section 5 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L.	Input/Output
$A_n, B_n, C_n, D_n$	Inputs	10/1.0	50 pA/-0.8 mA
$\bar{O}_n$	Output	50/33.3	-1 mA/50 mA



# 54F/74F64

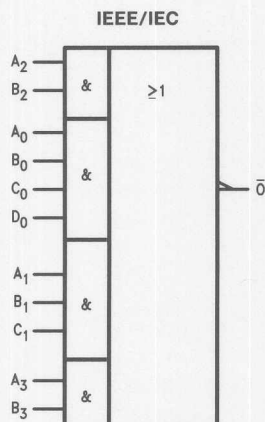
## 4-2-3-2-Input AND-OR-Invert Gate

### General Description

This device contains gates configured to perform a 4-2-3-2 input AND-OR-INVERT function.

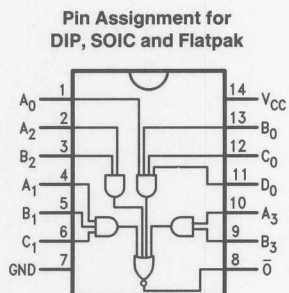
**Ordering Code:** See Section 5

### Logic Symbol

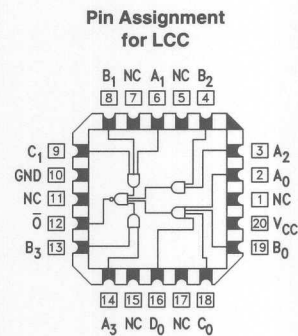


TL/F/9467-3

### Connection Diagrams



TL/F/9467-2



TL/F/9467-1

**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_n, B_n, C_n, D_n$	Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
O	Output	50/33.3	-1 mA/20 mA

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
---	----------------

Input Voltage (Note 2)	−0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	−30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.5 2.7		V	Min	I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output High Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		1.9	2.8	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		3.1	4.7	mA	Max	V <sub>O</sub> = LOW

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	2.5	4.6	6.5	2.5	8.5	2.5	7.5		2-3
$t_{PHL}$	$A_n, B_n, C_n, D_n$ to $\overline{O}$	1.5	3.2	4.5	1.5	6.5	1.5	5.5	ns	

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect input.

Note 3: Either voltage limit or current limit is sufficient to protect input.

## DC Electrical Characteristics

Symbol	Parameter	74F/54F		Units	$V_{CC}$	Conditions
		Min	Typ			
$V_{IH}$	Input HIGH Voltage	2.0		V		Recognized as a HIGH signal
$V_{IL}$	Input LOW Voltage	0.8		V		Recognized as a LOW signal
$V_{OD}$	Input Clamp Diode Voltage	-1.2		V	Min	$I_{IN} = -18\text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.8		V	Min	$I_{OH} = -1\text{ mA}$
		2.5		V	Min	$I_{OH} = -1\text{ mA}$
		2.3		V	Min	$I_{OH} = -1\text{ mA}$
		2.2		V	Min	$I_{OH} = -1\text{ mA}$
$V_{OL}$	Output LOW Voltage	0.8		V	Min	$I_{OL} = 20\text{ mA}$
		0.8		V	Min	$I_{OL} = 20\text{ mA}$
$I_{IH}$	Input HIGH Current	50		$\mu\text{A}$	Max	$V_{IN} = 2.7\text{V}$
		50		$\mu\text{A}$	Max	$V_{IN} = 2.7\text{V}$
$I_{BI}$	Input BIAS Current	100		$\mu\text{A}$	Max	$V_{IN} = 2.7\text{V}$
		100		$\mu\text{A}$	Max	$V_{IN} = 2.7\text{V}$
$I_{OZH}$	Output High Leakage Current	250		$\mu\text{A}$	Max	$V_{OUT} = V_{CC}$
		50		$\mu\text{A}$	Max	$V_{OUT} = V_{CC}$
$I_{ID}$	Input Leakage Test	4.75		$\mu\text{A}$	0.0	$I_D = 1.8\text{ mA}$ All Other Pins Grounded
$I_{OD}$	Output Leakage Circuit Current	3.75		$\mu\text{A}$	0.0	$V_{IO} = 150\text{ mV}$ All Other Pins Grounded
$I_{IL}$	Input LOW Current	-0.6		$\text{mA}$	Max	$V_{IN} = 0.3\text{V}$
$I_{OS}$	Output Short-Circuit Current	-80		$\text{mA}$	Max	$V_{OUT} = 0\text{V}$
$I_{OCH}$	Power Supply Current	1.5	2.8	$\text{mA}$	Max	$V_O = \text{HIGH}$
$I_{OCL}$	Power Supply Current	3.1	4.7	$\text{mA}$	Max	$V_O = \text{LOW}$

## 54F/74F74

# Dual D-Type Positive Edge-Triggered Flip-Flop

## General Description

The 'F74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary (Q,  $\bar{Q}$ ) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

## Asynchronous Inputs:

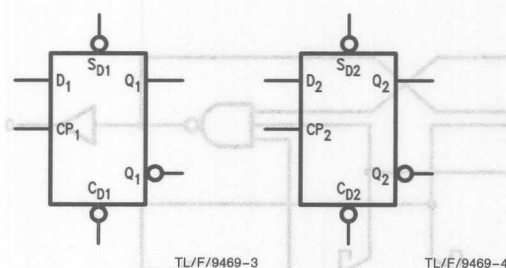
LOW input to  $\bar{S}_D$  sets Q to HIGH level  
LOW input to  $\bar{C}_D$  sets Q to LOW level  
Clear and Set are independent of clock  
Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$   
makes both Q and  $\bar{Q}$  HIGH

## Features

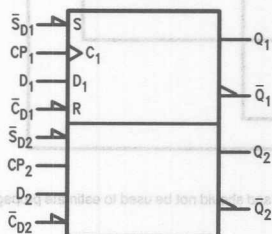
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

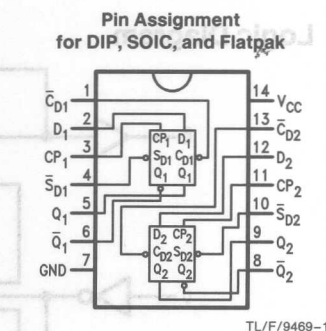
## Logic Symbols



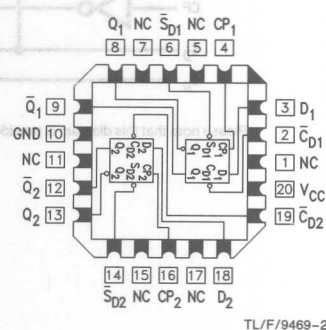
IEEE/IEC



TL/F/9469-6



Pin Assignment  
for LCC



TL/F/9469-2

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$D_1, D_2$	Data Inputs	1.0/1.0	$20 \mu A / -0.6 \text{ mA}$
$CP_1, CP_2$	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0	$20 \mu A / -0.6 \text{ mA}$
$\overline{CD}_1, \overline{CD}_2$	Direct Clear Inputs (Active LOW)	1.0/3.0	$20 \mu A / -1.8 \text{ mA}$
$\overline{SD}_1, \overline{SD}_2$	Direct Set Inputs (Active LOW)	1.0/3.0	$20 \mu A / -1.8 \text{ mA}$
$Q_1, \overline{Q}_1, Q_2, \overline{Q}_2$	Outputs	50/33.3	$-1 \text{ mA} / 20 \text{ mA}$

**Truth Table**

Inputs				Outputs	
$\overline{SD}$	$\overline{CD}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	$\nearrow$	h	H	L
H	H	$\searrow$	l	L	H
H	H	L	X	$Q_0$	$\overline{Q}_0$

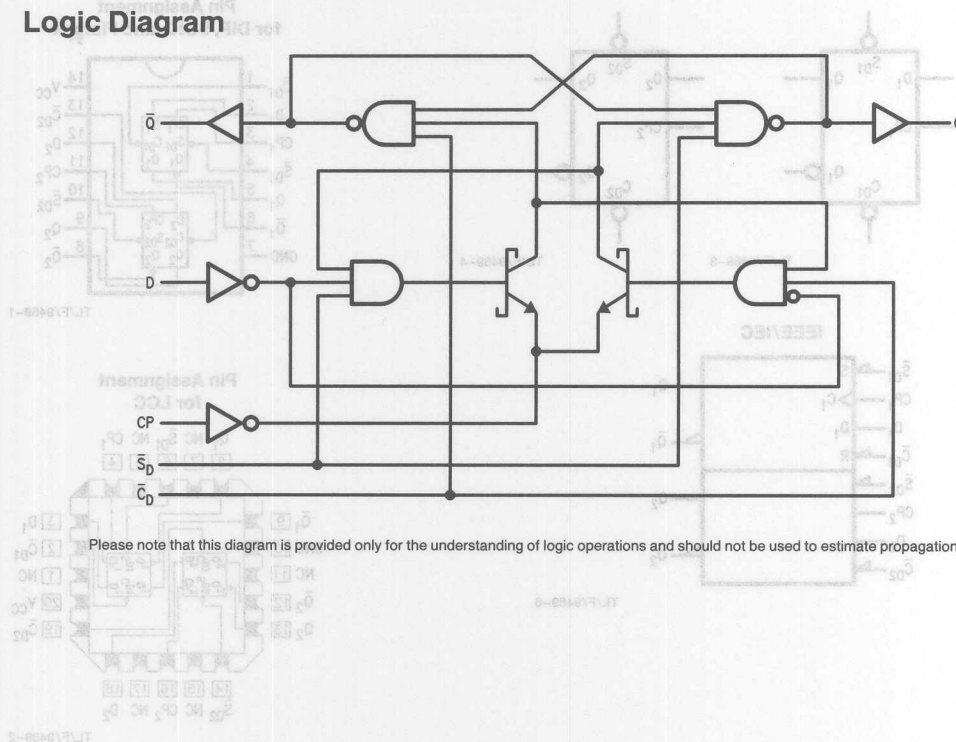
H (h) = HIGH Voltage Level

L (l) = LOW Voltage Level

X = Immaterial

 $Q_0$  = Previous Q (Q) before LOW-to-HIGH Clock Transition

Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

**Logic Diagram**


TL/F/9469-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	–0.5V to V <sub>CC</sub>
TRI-STATE® Output	–0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

ESD Last Passing Voltage (Min)	4000V
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**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	–55°C to +125°C
Military	0°C to +70°C
Commercial	
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			–1.2	V	Min	I <sub>IN</sub> = –18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.5 2.7		V	Min	I <sub>OH</sub> = –1 mA I <sub>OH</sub> = –1 mA I <sub>OH</sub> = –1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			–0.6 –1.8	mA	Max	V <sub>IN</sub> = 0.5V V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		–60	–150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		10.5	16.0	mA	Max	





# 54F/74F86

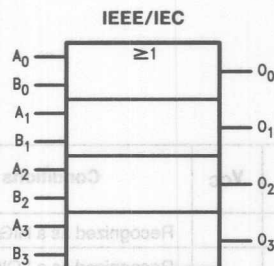
## 2-Input Exclusive-OR Gate

### General Description

This device contains four independent gates, each of which performs the logic exclusive-OR function.

**Ordering Code:** See Section 5

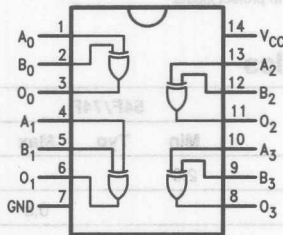
### Logic Symbol



TL/F/9470-3

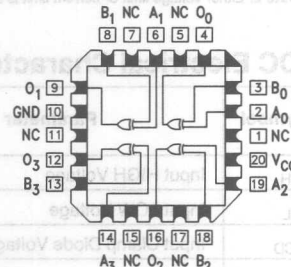
### Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9470-2

Pin Assignment for LCC



TL/F/9470-1

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_n, B_n$	Inputs	1.0/1.0	20 $\mu$ A / -0.6 mA
$O_n$	Outputs	50/33.3	-1 mA / 20 mA

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA

Voltage Applied to Output  
in HIGH State (with V<sub>CC</sub> = 0V)

Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output  
in LOW State (Max)

twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature

Military	-55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All other pins grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All other pins grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		12	18	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		18	28	mA	Max	V <sub>O</sub> = LOW

# **AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n, B_n$ to $O_n$ (Other Input LOW)	3.0 3.0	4.0 4.2	5.5 5.5	2.5 3.0	7.0 7.0	3.0 3.0	6.5 6.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n, B_n$ to $O_n$ (Other Input HIGH)	3.5 3.0	5.3 4.7	7.0 6.5	3.5 3.0	8.5 8.0	3.5 3.0	8.0 7.5	ns	2-3

HIGH

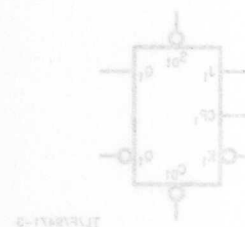
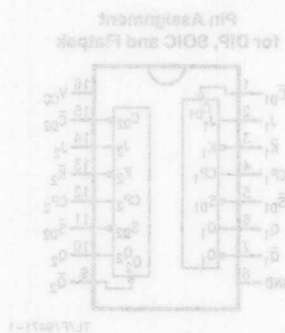
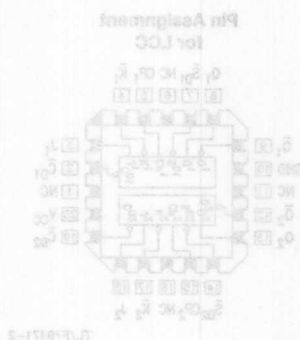
Features

Guaranteed 4000V minimum ESD protection.

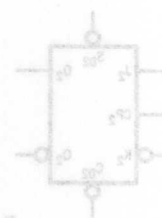
Ordering Code: See Section 5

Connection Diagrams

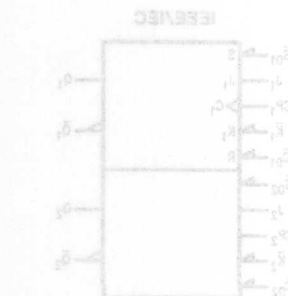
Logic Symbols



TLV3071-2



TLV3071-4



TLV3071-6


**54F/74F109**

## Dual JK Positive Edge-Triggered Flip-Flop

### General Description

The 'F109 consists of two high-speed, completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D flip-flop (refer to 'F74 data sheet) by connecting the J and  $\bar{K}$  inputs.

### Asynchronous Inputs:

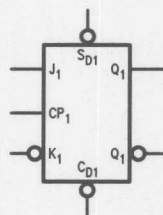
LOW input to  $\bar{S}_D$  sets Q to HIGH level  
 LOW input to  $\bar{C}_D$  sets Q to LOW level  
 Clear and Set are independent of clock  
 Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both Q and  $\bar{Q}$  HIGH

### Features

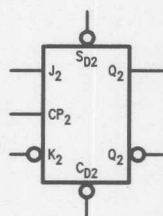
- Guaranteed 4000V minimum ESD protection.

**Ordering Code:** See Section 5

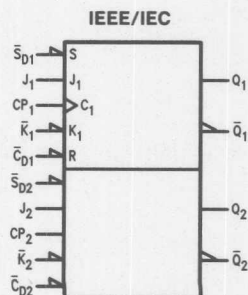
### Logic Symbols



TL/F/9471-3



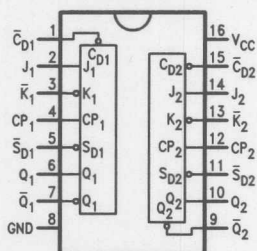
TL/F/9471-4



TL/F/9471-6

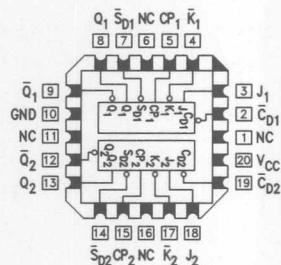
### Connection Diagrams

Pin Assignment  
for DIP, SOIC and Flatpak



TL/F/9471-1

Pin Assignment  
for LCC



TL/F/9471-2

# Unit Loading/Fan Out: See Section 2 for U.L. definitions

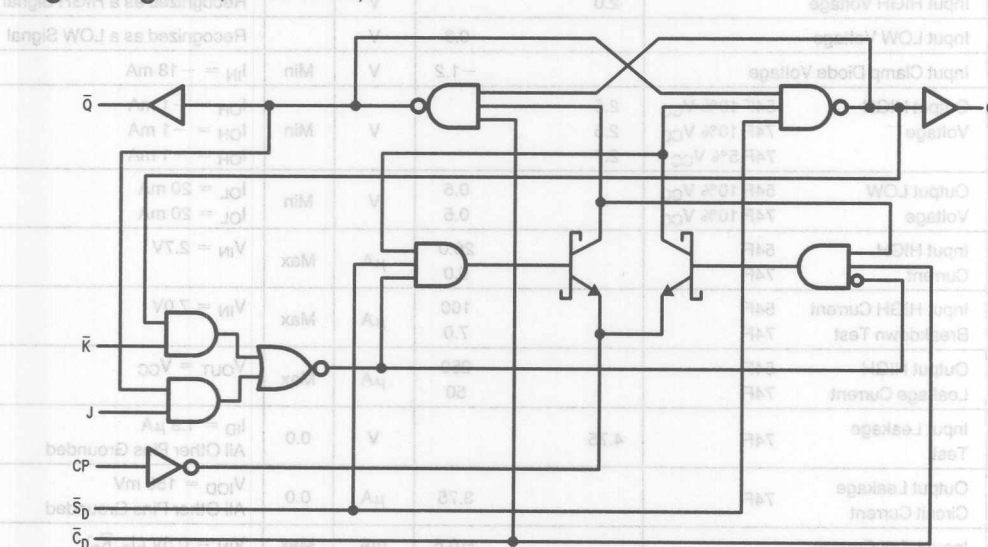
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$J_1, J_2, \bar{K}_1, \bar{K}_2$	Data Inputs	1.0/1.0	20 $\mu$ A / -0.6 mA
$CP_1, CP_2$	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0	20 $\mu$ A / -0.6 mA
$\bar{C}_D1, \bar{C}_D2$	Direct Clear Inputs (Active LOW)	1.0/3.0	20 $\mu$ A / -1.8 mA
$\bar{S}_D1, \bar{S}_D2$	Direct Set Inputs (Active LOW)	1.0/3.0	20 $\mu$ A / -1.8 mA
$Q_1, Q_2, \bar{Q}_1, \bar{Q}_2$	Outputs	50/33.3	1 mA / 20 mA

## Truth Table

Inputs					Outputs	
$\bar{S}_D$	$\bar{C}_D$	CP	J	$\bar{K}$	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	$\nearrow$	l	l	L	H
H	H	$\nearrow$	h	l	Toggle	
H	H	$\nearrow$	l	h	$Q_0$	$\bar{Q}_0$
H	H	$\nearrow$	h	h	H	L
H	H	L	X	X	$Q_0$	$\bar{Q}_0$

H (h) = HIGH Voltage Level  
L (l) = LOW Voltage Level  
 $\nearrow$  = LOW-to-HIGH Transition  
X = Immaterial  
 $Q_0$  ( $\bar{Q}_0$ ) = Before LOW-to-HIGH Transition of Clock  
Lower case letters indicate the state of the referenced output one setup time prior to the LOW-to-HIGH clock transition.

## Logic Diagram (One Half Shown)



TL/F/9471-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



Storage Temperature  
Ambient Temperature under Bias  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
Junction Temperature under Bias  $-55^{\circ}\text{C}$  to  $+175^{\circ}\text{C}$   
 $V_{CC}$  Pin Potential to Ground Pin  $-0.5\text{V}$  to  $+7.0\text{V}$   
Input Voltage (Note 2)  $-0.5\text{V}$  to  $+7.0\text{V}$   
Input Current (Note 2)  $-30\text{ mA}$  to  $+5.0\text{ mA}$   
Voltage Applied to Output in HIGH State (with  $V_{CC} = 0\text{V}$ )  
Standard Output  $-0.5\text{V}$  to  $V_{CC}$   
TRI-STATE® Output  $-0.5\text{V}$  to  $+5.5\text{V}$   
Current Applied to Output in LOW State (Max) twice the rated  $I_{OL}$  (mA)  
ESD Last Passing Voltage (Min) 4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

Supply Voltage  
Military  $+4.5\text{V}$  to  $+5.5\text{V}$   
Commercial  $+4.5\text{V}$  to  $+5.5\text{V}$

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	$V_{CC}$	Conditions
		Min	Typ	Max			
$V_{IH}$	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
$V_{IL}$	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
$V_{CD}$	Input Clamp Diode Voltage			-1.2	V	Min	$I_{IN} = -18\text{ mA}$
$V_{OH}$	Output HIGH Voltage	54F 10% $V_{CC}$	2.5		V	Min	$I_{OH} = -1\text{ mA}$
		74F 10% $V_{CC}$	2.5				$I_{OH} = -1\text{ mA}$
		74F 5% $V_{CC}$	2.7				$I_{OH} = -1\text{ mA}$
$V_{OL}$	Output LOW Voltage	54F 10% $V_{CC}$		0.5	V	Min	$I_{OL} = 20\text{ mA}$
		74F 10% $V_{CC}$		0.5			$I_{OL} = 20\text{ mA}$
$I_{IH}$	Input HIGH Current	54F		20.0	$\mu\text{A}$	Max	$V_{IN} = 2.7\text{V}$
		74F		5.0			
$I_{BVI}$	Input HIGH Current Breakdown Test	54F		100	$\mu\text{A}$	Max	$V_{IN} = 7.0\text{V}$
		74F		7.0			
$I_{CEX}$	Output HIGH Leakage Current	54F		250	$\mu\text{A}$	Max	$V_{OUT} = V_{CC}$
		74F		50			
$V_{ID}$	Input Leakage Test	74F	4.75		V	0.0	$I_{ID} = 1.9\text{ }\mu\text{A}$ All Other Pins Grounded
$I_{OD}$	Output Leakage Circuit Current	74F		3.75	$\mu\text{A}$	0.0	$V_{IOD} = 150\text{ mV}$ All Other Pins Grounded
$I_{IL}$	Input LOW Current			-0.6	$\text{mA}$	Max	$V_{IN} = 0.5\text{V}$ ( $J_n, \bar{K}_n$ )
				-1.8	$\text{mA}$	Max	$V_{IN} = 0.5\text{V}$ ( $\bar{C}_{Dn}, \bar{S}_{Dn}$ )
$I_{OS}$	Output Short-Circuit Current		-60	-150	$\text{mA}$	Max	$V_{OUT} = 0\text{V}$
$I_{CC}$	Power Supply Current		11.7	17.0	$\text{mA}$	Max	$CP = 0\text{V}$

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	100	125		50		90		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	3.8	5.3	7.0	3.8	9.0	3.8	8.0	ns	2-3
$t_{\text{PHL}}$	$\text{CP}_n$ to $\text{Q}_n$ or $\overline{\text{Q}}_n$	4.4	6.2	8.0	4.4	10.5	4.4	9.2		
$t_{\text{PLH}}$	Propagation Delay	3.2	5.2	7.0	3.2	9.0	3.2	8.0	ns	2-3
$t_{\text{PHL}}$	$\overline{\text{C}}_{\text{Dn}}$ or $\overline{\text{S}}_{\text{Dn}}$ to $\text{Q}_n$ or $\overline{\text{Q}}_n$	3.5	7.0	9.0	3.5	11.5	3.5	10.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	3.0		3.0		3.0		ns	2-6
$t_s(\text{L})$	$J_n$ or $\overline{K}_n$ to $\text{CP}_n$	3.0		5.0		3.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	1.0		1.0		1.0		ns	2-4
$t_h(\text{L})$	$J_n$ or $\overline{K}_n$ to $\text{CP}_n$	1.0		1.0		1.0			
$t_w(\text{H})$	$\text{CP}_n$ Pulse Width	4.0		4.0		4.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	5.0		5.0		5.0			
$t_w(\text{L})$	$\overline{\text{C}}_{\text{Dn}}$ or $\overline{\text{S}}_{\text{Dn}}$ Pulse Width, LOW	4.0		4.0		4.0		ns	2-4
$t_{\text{rec}}$	Recovery Time $\overline{\text{C}}_{\text{Dn}}$ or $\overline{\text{S}}_{\text{Dn}}$ to CP	2.0		2.0		2.0		ns	2-6


**54F/74F112**

## Dual JK Negative Edge-Triggered Flip-Flop

### General Description

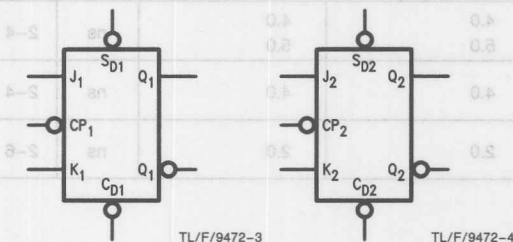
The 'F112 contains two independent, high-speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on  $\bar{S}_D$  or  $\bar{C}_D$  prevents clocking and forces Q or  $\bar{Q}$  HIGH, respectively. Simultaneous LOW signals on  $\bar{S}_D$  and  $\bar{C}_D$  force both Q and  $\bar{Q}$  HIGH.

### Asynchronous Inputs:

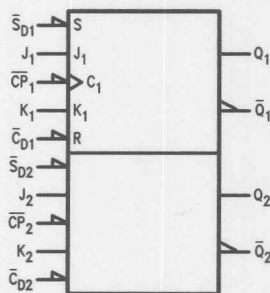
- LOW input to  $\bar{S}_D$  sets Q to HIGH level
- LOW input to  $\bar{C}_D$  sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both Q and  $\bar{Q}$  HIGH

**Ordering Code:** See Section 5

### Logic Symbols



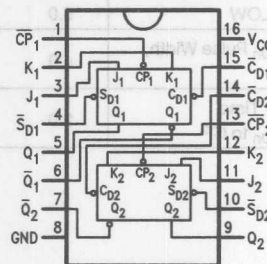
IEEE/IEC



TL/F/9472-6

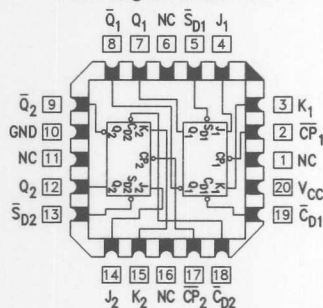
### Connection Diagrams

#### Pin Assignment for DIP, SOIC and Flatpak



TL/F/9472-1

#### Pin Assignment for LCC



TL/F/9472-2

# Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$J_1, J_2, K_1, K_2$	Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{CP}_1, \overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	1.0/4.0	20 $\mu$ A/ -2.4 mA
$\overline{CD}_1, \overline{CD}_2$	Direct Clear Inputs (Active LOW)	1.0/5.0	20 $\mu$ A/ -3.0 mA
$\overline{SD}_1, \overline{SD}_2$	Direct Set Inputs (Active LOW)	1.0/5.0	20 $\mu$ A/ -3.0 mA
$Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$	Outputs	50/33.3	-1 mA/20 mA

## Truth Table

Inputs					Outputs	
$\overline{SD}$	$\overline{CD}$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	$\sim$	h	h	$\overline{Q}_0$	$Q_0$
H	H	$\sim$	l	h	L	H
H	H	$\sim$	h	l	H	L
H	H	$\sim$	l	l	$Q_0$	$\overline{Q}_0$

H(h) = HIGH Voltage Level

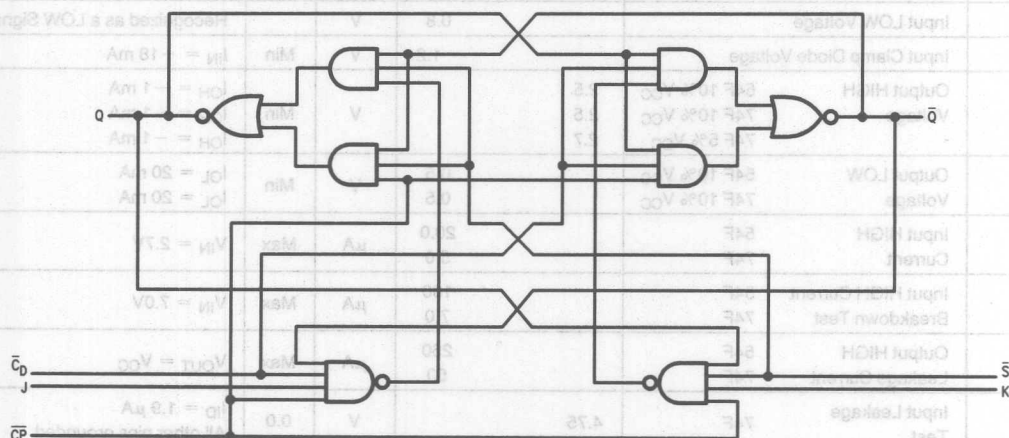
L(l) = LOW Voltage Level

X = Immaterial

 $\sim$  = HIGH-to-LOW Clock Transition $Q_0(\overline{Q}_0)$  = Before HIGH-to-LOW Transition of Clock

Lower case letters indicate the state of the referenced input or output one setup time prior to the HIGH-to-LOW clock transition.

## Logic Diagram (One Half Shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

TL/F/9472-5

**Office/Distributors for availability and specifications.**

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA

Voltage Applied to Output  
in HIGH State (with V<sub>CC</sub> = 0V)

Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output  
in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

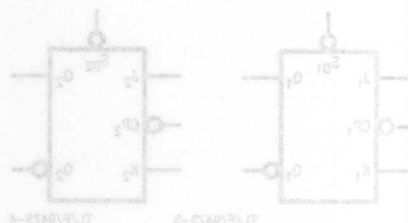
Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All other pins grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All other pins grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V (J <sub>N</sub> , K <sub>N</sub> )
				-2.4			V <sub>IN</sub> = 0.5V ( $\overline{C_P}$ <sub>N</sub> )
				-3.0			V <sub>IN</sub> = 0.5V ( $\overline{C_D}$ <sub>N</sub> , $\overline{S_D}$ <sub>N</sub> )
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		12	19	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		12	19	mA	Max	V <sub>O</sub> = LOW

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	85	105				80		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay $\overline{\text{CP}}_n$ to $Q_n$ or $\overline{Q}_n$	2.0	5.0	6.5			2.0	7.5	ns	2-3
$t_{\text{PHL}}$	Propagation Delay $\overline{\text{CP}}_n$ to $Q_n$ or $\overline{Q}_n$	2.0	5.0	6.5			2.0	7.5	ns	2-3
$t_{\text{PLH}}$	Propagation Delay $\overline{\text{CD}}_n, \overline{\text{SD}}_n$ to $\overline{Q}_n, \overline{Q}_n$	2.0	4.5	6.5			2.0	7.5	ns	2-3
$t_{\text{PHL}}$	Propagation Delay $\overline{\text{CD}}_n, \overline{\text{SD}}_n$ to $\overline{Q}_n, \overline{Q}_n$	2.0	4.5	6.5			2.0	7.5	ns	2-3

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $J_n$ or $K_n$ to $\overline{\text{CP}}_n$	4.0 3.0				5.0 3.5		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $J_n$ or $K_n$ to $\overline{\text{CP}}_n$	0 0				0 0			
$t_w(\text{H})$ $t_w(\text{L})$	$\overline{\text{CP}}$ Pulse Width HIGH or LOW	4.5 4.5				5.0 5.0		ns	2-4
$t_w(\text{L})$	Pulse Width, LOW $\overline{\text{CD}}_n$ or $\overline{\text{SD}}_n$	4.5				5.0		ns	2-4
$t_{\text{rec}}$	Recovery Time $\overline{\text{SD}}_n, \overline{\text{CD}}_n$ to $\overline{\text{CP}}$	4.0				5.0		ns	2-6



Unit Loadings: See Section 2 for U.I. Definitions

Pin Names	Description	U.I.	
		LOW	HIGH
$J_n, K_n, \overline{\text{CP}}_n$	Data Inputs	1.0V/0.1	1.0V/0.1
$\overline{\text{CP}}_n, \overline{\text{SD}}_n$	Clock Pulse Inputs (Active Falling Edge)	1.0V/0.1	1.0V/0.1
$\overline{\text{SD}}_n, \overline{\text{CD}}_n$	Direct Set Inputs (Active LOW)	1.0V/0.1	1.0V/0.1
$Q_n, \overline{Q}_n$	Outputs	80V/3.3	80V/3.3




**54F/74F113**

## Dual JK Negative Edge-Triggered Flip-Flop

### General Description

The 'F113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is HIGH and the flip-flop will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

Asynchronous input:

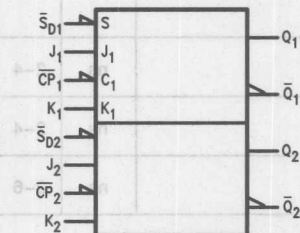
LOW input to  $\bar{S}_D$  sets Q to HIGH level

Set is independent of clock

**Ordering Code:** See Section 5

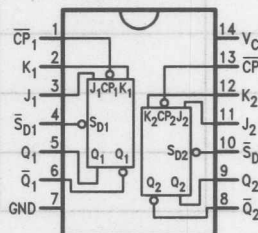
### Logic Symbols

IEEE/IEC



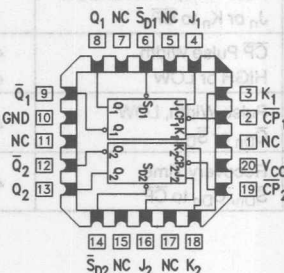
TL/F/9473-6

Pin Assignment for  
DIP, SOIC and Flatpak

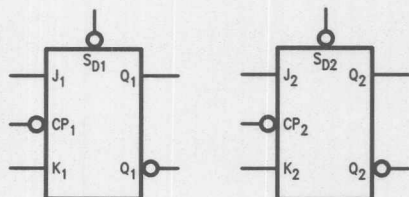


TL/F/9473-1

Pin Assignment  
for LCC



TL/F/9473-2



TL/F/9473-3

TL/F/9473-4

**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$J_1, J_2, K_1, K_2$	Data Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
$CP_1, CP_2$	Clock Pulse Inputs (Active Falling Edge)	1.0/4.0	20 $\mu A$ / -2.4 mA
$\bar{S}_{D1}, \bar{S}_{D2}$	Direct Set Inputs (Active LOW)	1.0/5.0	20 $\mu A$ / -3.0 mA
$Q_1, Q_2, \bar{Q}_1, \bar{Q}_2$	Outputs	50/33.3	-1 mA / 20 mA



**Office/Distributors for availability and specifications.**

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA

Voltage Applied to Output  
in HIGH State (with V<sub>CC</sub> = 0V)

Standard Output -0.5V to V<sub>CC</sub>

TRI-STATE® Output -0.5V to +5.5V

Current Applied to Output

in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

Military			-55°C to +125°C
Commercial	X	X	0°C to +70°C
Supply Voltage	H	H	
Military	H	H	+4.5V to +5.5V
Commercial	H	H	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6 -2.4 -3.0	mA	Max	V <sub>IN</sub> = 0.5V (J <sub>n</sub> , K <sub>n</sub> ) V <sub>IN</sub> = 0.5V (CP <sub>n</sub> ) V <sub>IN</sub> = 0.5V (SD <sub>n</sub> )
I <sub>OZH</sub>	Output Leakage Current			50			V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			-50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		12	19	mA	Max	

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	85	105				80		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	2.0	4.0	6.0			2.0	7.0	ns	2-3
$t_{\text{PHL}}$	$\overline{\text{CP}}_n$ to $Q_n$ or $\overline{Q}_n$	2.0	4.0	6.0			2.0	7.0		
$t_{\text{PLH}}$	Propagation Delay	2.0	4.5	6.5			2.0	7.5	ns	2-3
$t_{\text{PHL}}$	$\overline{\text{SD}}_n$ to $Q_n$ or $\overline{Q}_n$	2.0	4.5	6.5			2.0	7.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	4.0				5.0			
$t_s(\text{L})$	$J_n$ or $K_n$ to $\overline{\text{CP}}_n$	3.0				3.5		ns	2-6
$t_h(\text{H})$	Hold Time, HIGH or LOW	0				0			
$t_h(\text{L})$	$J_n$ or $K_n$ to $\overline{\text{CP}}_n$	0				0			
$t_w(\text{H})$	$\overline{\text{CP}}_n$ Pulse Width	4.5				5.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	4.5				5.0			
$t_w(\text{L})$	$\overline{\text{SD}}_n$ Pulse Width, LOW	4.5				5.0		ns	2-4
$t_{\text{rec}}$	$\overline{\text{SD}}_n$ to $\overline{\text{CP}}_n$ Recovery Time	4.0				5.0		ns	2-6


**54F/74F114**

## Dual JK Negative Edge-Triggered Flip-Flop with Common Clocks and Clears

### General Description

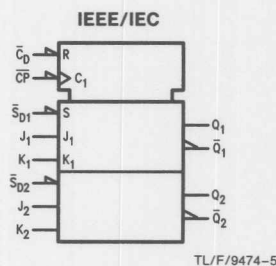
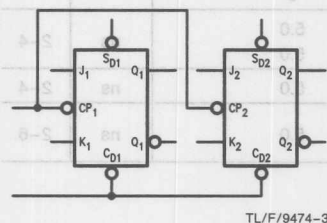
The 'F114 contains two high-speed JK flip-flops with common Clock and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on  $\bar{S}_D$  or  $\bar{C}_D$  prevents clocking and forces Q or  $\bar{Q}$  HIGH, respectively. Simultaneous LOW signals on  $\bar{S}_D$  and  $\bar{C}_D$  force both Q and  $\bar{Q}$  HIGH.

### Asynchronous Inputs:

LOW input to  $\bar{S}_D$  sets Q to HIGH level  
LOW input to  $\bar{C}_D$  sets Q to LOW level  
Clear and Set are independent of Clock  
Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$   
makes both Q and  $\bar{Q}$  HIGH

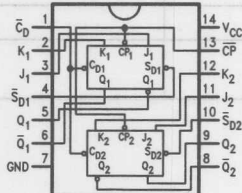
**Ordering Code:** See Section 5

### Logic Symbols

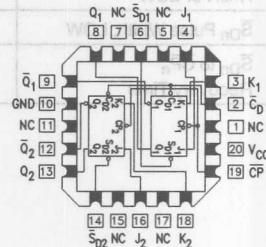


### Connection Diagrams

**Pin Assignment  
for DIP, SOIC and Flatpak**



**Pin Assignment  
for LCC**



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$J_1, J_2, K_1, K_2$	Data Inputs	1.0/1.0	20 $\mu$ A/ - 0.6 mA
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	1.0/8.0	20 $\mu$ A/ - 4.8 mA
$\overline{CD}$	Direct Clear Input (Active LOW)	1.0/10.0	20 $\mu$ A/ - 6.0 mA
$\overline{SD}_1, \overline{SD}_2$	Direct Set Inputs (Active LOW)	1.0/5.0	20 $\mu$ A/ - 3.0 mA
$Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$	Outputs	50/33.3	- 1 mA/20 mA

**Truth Table**

Inputs					Outputs	
$\overline{SD}$	$\overline{CD}$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	$\sim$	h	h	$\overline{Q}_0$	$Q_0$
H	H	$\sim$	l	h	L	H
H	H	$\sim$	h	l	H	L
H	H	$\sim$	l	l	$Q_0$	$\overline{Q}_0$

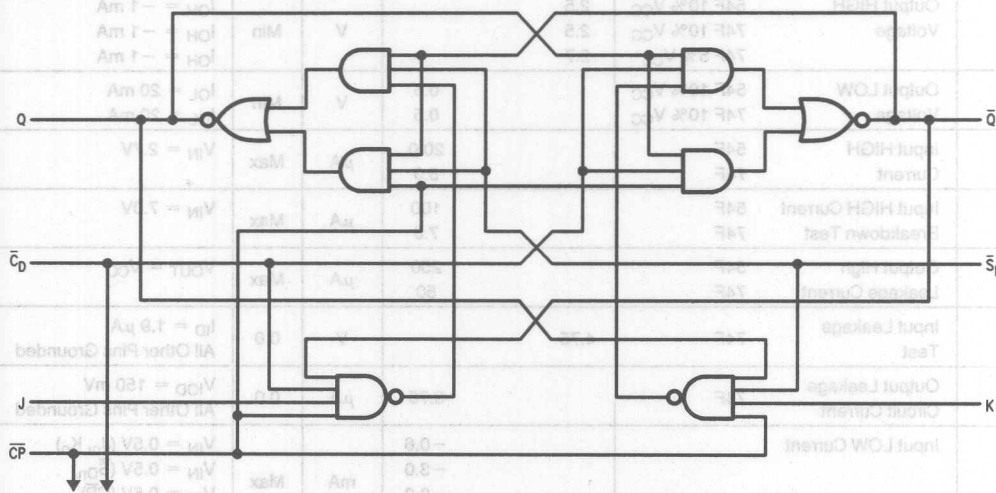
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

 $\sim$  = HIGH-to-LOW Clock Transition $Q_0$  ( $\overline{Q}_0$ ) = Before HIGH-to-LOW Transition of Clock

Lower case letters indicate the state of the referenced input or output one setup time prior to the HIGH-to-LOW clock transition.

**Logic Diagram** (one half shown)


TL/F/9474-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

Ambient Temperature under Bias  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Junction Temperature under Bias  $-55^{\circ}\text{C}$  to  $+175^{\circ}\text{C}$

$V_{CC}$  Pin Potential to Ground Pin  $-0.5\text{V}$  to  $+7.0\text{V}$

Input Voltage (Note 2)  $-0.5\text{V}$  to  $+7.0\text{V}$

Input Current (Note 2)  $-30\text{ mA}$  to  $+5.0\text{ mA}$

Voltage Applied to Output in HIGH State (with  $V_{CC} = 0\text{V}$ )

Standard Output  $-0.5\text{V}$  to  $V_{CC}$

TRI-STATE® Output  $-0.5\text{V}$  to  $+5.5\text{V}$

Current Applied to Output in LOW State (Max) twice the rated  $I_{OL}$  (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
Commercial  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$

Supply Voltage

Military  $+4.5\text{V}$  to  $+5.5\text{V}$   
Commercial  $+4.5\text{V}$  to  $+5.5\text{V}$

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	$V_{CC}$	Conditions
		Min	Typ	Max			
$V_{IH}$	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
$V_{IL}$	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
$V_{CD}$	Input Clamp Diode Voltage			-1.2	V	Min	$I_{IN} = -18\text{ mA}$
$V_{OH}$	Output HIGH Voltage	54F 10% $V_{CC}$	2.5		V	Min	$I_{OH} = -1\text{ mA}$
		74F 10% $V_{CC}$	2.5				$I_{OH} = -1\text{ mA}$
		74F 5% $V_{CC}$	2.7				$I_{OH} = -1\text{ mA}$
$V_{OL}$	Output LOW Voltage	54F 10% $V_{CC}$		0.5	V	Min	$I_{OL} = 20\text{ mA}$
		74F 10% $V_{CC}$		0.5			$I_{OL} = 20\text{ mA}$
$I_{IH}$	Input HIGH Current	54F		20.0	$\mu\text{A}$	Max	$V_{IN} = 2.7\text{V}$
		74F		5.0			
$I_{BVI}$	Input HIGH Current Breakdown Test	54F		100	$\mu\text{A}$	Max	$V_{IN} = 7.0\text{V}$
		74F		7.0			
$I_{CEX}$	Output High Leakage Current	54F		250	$\mu\text{A}$	Max	$V_{OUT} = V_{CC}$
		74F		50			
$V_{ID}$	Input Leakage Test	74F	4.75		V	0.0	$I_{ID} = 1.9\text{ }\mu\text{A}$ All Other Pins Grounded
$I_{OD}$	Output Leakage Circuit Current	74F		3.75	$\mu\text{A}$	0.0	$V_{IOD} = 150\text{ mV}$ All Other Pins Grounded
$I_{IL}$	Input LOW Current			-0.6	mA	Max	$V_{IN} = 0.5\text{V}$ ( $J_n$ , $K_n$ )
				-3.0			$V_{IN} = 0.5\text{V}$ ( $\overline{S}_{Dn}$ )
				-8.0			$V_{IN} = 0.5\text{V}$ ( $\overline{CP}$ )
				-10.0			$V_{IN} = 0.5\text{V}$ ( $\overline{C}_{Dn}$ )
$I_{OS}$	Output Short-Circuit Current	-60		-150	mA	Max	$V_{OUT} = 0\text{V}$
$I_{CCH}$	Power Supply Current		12.0	19.0	mA	Max	$V_O = \text{HIGH}$
$I_{CCL}$	Power Supply Current		12.0	19.0	mA	Max	$V_O = \text{LOW}$

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	75	95				70		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	3.0	5.0	6.5			3.0	7.5	ns	2-3
$t_{\text{PHL}}$	$\overline{\text{CP}}$ to $Q_n$ or $\overline{Q}_n$	3.0	5.5	7.5			3.0	8.5		
$t_{\text{PLH}}$	Propagation Delay	3.0	4.5	6.5			3.0	7.5	ns	2-3
$t_{\text{PHL}}$	$\overline{\text{CD}}_n$ or $\overline{\text{SD}}_n$ to $Q_n$ or $\overline{Q}_n$	3.0	4.5	6.5			3.0	7.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	4.0				5.0		ns	2-6
$t_s(\text{L})$	$J_n$ or $K_n$ to $\overline{\text{CP}}$	3.0				3.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0				0		ns	2-4
$t_h(\text{L})$	$J_n$ or $K_n$ to $\overline{\text{CP}}$	0				0			
$t_w(\text{H})$	$\overline{\text{CP}}$ Pulse Width	4.5				5.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	4.5				5.0			
$t_w(\text{L})$	$\overline{\text{CD}}_n$ or $\overline{\text{SD}}_n$ Pulse Width, LOW	4.5				5.0		ns	2-4
$t_{\text{rec}}$	Recovery Time $\overline{\text{SD}}_n, \overline{\text{CD}}_n$ , to $\overline{\text{CP}}$	4.0				5.0		ns	2-6

Pin Number	Description	74F	
		Input	Output
$\overline{A}_n, \overline{B}_n$	Inputs	1.0/0.033	50 $\mu\text{A}$ - 50 $\mu\text{A}$
$Q_n$	Outputs	600/108.8 (80)	12 mA/84 mA (48 mA)

Function Table

Output	Inputs	
$Q$	$\overline{A}_n$	$\overline{B}_n$
L	L	L
H	H	H
$\Sigma$	X	X

H = High Voltage Level  
L = Low Voltage Level  
 $\Sigma$  = High Impedance  
X = Indeterminate



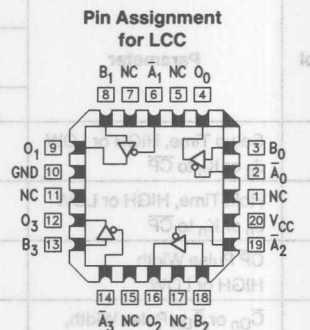
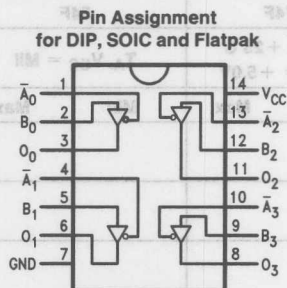
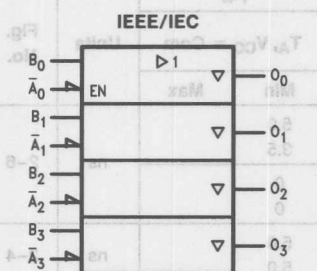
# 54F/74F125 Quad Buffer (TRI-STATE®)

## Features

- High impedance base inputs for reduced loading

**Ordering Code:** See Section 5

## Logic Symbol



**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\bar{A}_n, B_n$	Inputs	1.0/0.033	20 $\mu A$ / -20 $\mu A$
$O_n$	Outputs	600/106.6 (80)	-12 mA/64 mA (48 mA)

Function Table

Inputs		Output
$\bar{A}_n$	$B_n$	O
L	L	L
L	H	H
H	X	Z

H = High Voltage Level  
L = LOW Voltage Level  
Z = High Impedance  
X = Immaterial

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output	−0.5V to +5.5V
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.4 2.0 2.4 2.0 2.7 2.0		V	Min	I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −12 mA I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −12 mA I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −15 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.55 0.55	V	Min	I <sub>OL</sub> = 48 mA I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current			20	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			100	μA	0.0V	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current			−20.0	μA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	−100		−225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CEX</sub>	Output HIGH Leakage Current			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>ZZ</sub>	Buss Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current		18.5	24.0	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		31.7	40.0	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		27.6	35.0	mA	Max	V <sub>O</sub> = HIGH Z

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay	2.0	4.0	6.0			2.0	6.5	ns	2-3
		3.0	4.6	7.5			3.0	8.0		
$t_{PZH}$ $t_{PZL}$	Output Enable Time	3.5	4.7	7.5			3.0	8.5	ns	2-5
		3.5	5.3	8.0			3.5	9.0		
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time	1.5	3.9	5.5			1.5	6.0	ns	2-5
		1.5	4.0	6.0			1.5	6.5		

Note 1: Error voltage limit or current limit is sufficient to protect inputs.  
 Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.  
 Note 3: In LOW State (Max) in LOW State (Max) Current Applied to Output twice the rated  $I_{OL}$  (mA).

## DC Electrical Characteristics

Symbol	Parameter	74F/54F			Units	$V_{CC}$	Conditions
		Min	Typ	Max			
$V_{IH}$	Input HIGH Voltage	2.0			V		Recognized as a HIGH signal
$V_{IL}$	Input LOW Voltage	0.8			V		Recognized as a LOW signal
$V_{CD}$	Input Clamp Diode Voltage	-1.5			V	Min	$I_{IN} = -18\text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.4			V	Min	$I_{OH} = -3\text{ mA}$
		2.0					$I_{OH} = -12\text{ mA}$
		2.4					$I_{OH} = -3\text{ mA}$
		2.0					$I_{OH} = -12\text{ mA}$
		2.7					$I_{OH} = -3\text{ mA}$
		2.0					$I_{OH} = -12\text{ mA}$
$V_{OL}$	Output LOW Voltage	0.55			V	Min	$I_{OL} = 48\text{ mA}$
		0.55					$I_{OL} = 84\text{ mA}$
$I_{IH}$	Input HIGH Current	50			$\mu\text{A}$	Max	$V_{IN} = 5.5\text{ V}$
$I_{IHI}$	Input HIGH Current Breakdown Test	100			$\mu\text{A}$	0.0 V	$V_{IN} = 7.0\text{ V}$
$I_{IL}$	Input LOW Current	-20.0			$\mu\text{A}$	Max	$V_{IN} = 0.5\text{ V}$
$I_{OLH}$	Output Leakage Current	50			$\mu\text{A}$	Max	$V_{OUT} = 5.5\text{ V}$
$I_{OLZ}$	Output Leakage Current	50			$\mu\text{A}$	Max	$V_{OUT} = 0.5\text{ V}$
$I_{OS}$	Output Short-Circuit Current	-100			mA	Max	$V_{OUT} = 0\text{ V}$
$I_{OEX}$	Output HIGH Leakage Current	250			$\mu\text{A}$	Max	$V_{OUT} = V_{CC}$
$I_{OZ}$	Output Drainage Test	300			$\mu\text{A}$	0.0 V	$V_{OUT} = 5.5\text{ V}$
$I_{OCH}$	Power Supply Current	18.5			mA	Max	$V_O = \text{HIGH}$
$I_{OCL}$	Power Supply Current	31.7			mA	Max	$V_O = \text{LOW}$
$I_{OCS}$	Power Supply Current	27.8			mA	Max	$V_O = \text{HIGH } Z$



**54F/74F132**

## Quad 2-Input NAND Schmitt Trigger

### General Description

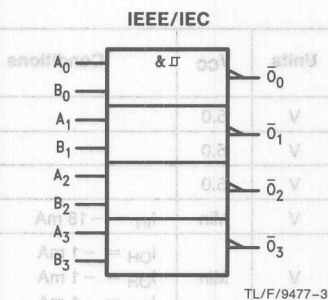
The 'F132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional NAND gates.

Each circuit contains a 2-input Schmitt trigger followed by level shifting circuitry and a standard FAST® output structure. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800 mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

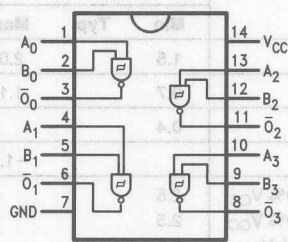
Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

### Logic Symbol

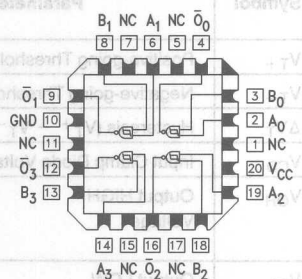


**Pin Assignment for DIP, SOIC and Flatpak**



### Connection Diagrams

**Pin Assignment for LCC**



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_n, B_n$	Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$O_n$	Outputs	50/33.3	-1 mA/20 mA

**Function Table**

Inputs		Outputs	
A	B	O	
L	L	H	Am
L	H	H	Am
H	L	H	Am
H	H	L	Am

H = HIGH Voltage Level

L = LOW Voltage Level



## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	−55°C to +125°C
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>T+</sub>	Positive-going Threshold	1.5		2.0	V	5.0	
V <sub>T−</sub>	Negative-going Threshold	0.7		1.1	V	5.0	
ΔV <sub>T</sub>	Hysteresis (V <sub>T+</sub> − V <sub>T−</sub> )	0.4			V	5.0	
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current			17.0	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			18.0	mA	Max	V <sub>O</sub> = LOW

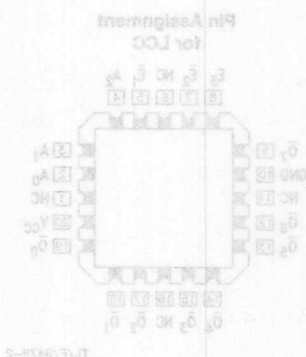
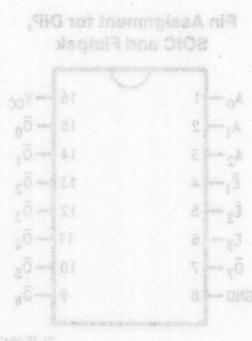
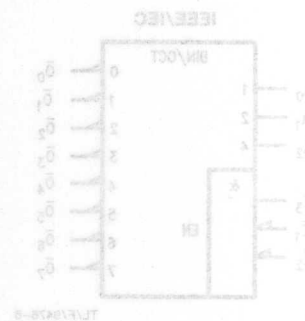
# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	4.0		10.5	2.0	13.0	3.5	12.0	ns	2-3
$t_{PHL}$	$A_n, B_n$ to $O_n$	5.0		12.5	4.5	16.0	5.0	13.0		

The 'F138 is a high-speed 1-of-8 decoder/multiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-32 decoder using just three 'F138 devices or a 1-of-32 decoder using four 'F138 devices and one inverter.

Ordering Code: See Section 5

Logic Symbols



Unit Loading/Fan Out: See Section 5 for U.L. Definitions

Pin Name	Description	74F138	
		U.L.	Input/Output
$A_0-A_2$	Address inputs	1.0V/0	Output for fan out
$E_0, E_1$	Enable inputs (Active LOW)	1.0V/0	Output for fan out
$E_2$	Enable input (Active HIGH)	1.0V/0	Output for fan out
$\bar{O}_0-\bar{O}_7$	Outputs (Active LOW)	50/23.3	Input for fan out


**54F/74F138**

# 1-of-8 Decoder/Demultiplexer

## General Description

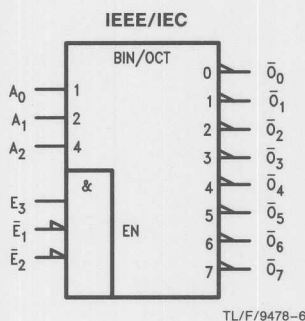
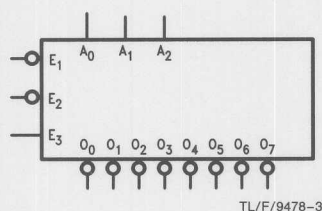
The 'F138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 'F138 devices or a 1-of-32 decoder using four 'F138 devices and one inverter.

## Features

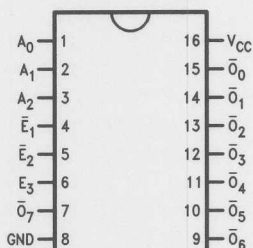
- Demultiplexing capability
- Multiple input enable for easy expansion
- Active LOW mutually exclusive outputs
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

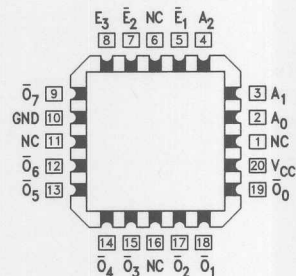
## Logic Symbols



Pin Assignment for DIP,  
SOIC and Flatpak



Pin Assignment  
for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_0-A_2$	Address Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
$\bar{E}_1, \bar{E}_2$	Enable Inputs (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$E_3$	Enable Input (Active HIGH)	1.0/1.0	20 $\mu A$ / -0.6 mA
$\bar{O}_0-\bar{O}_7$	Outputs (Active LOW)	50/33.3	-1 mA/20 mA

## Functional Description

The 'F138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs ( $A_0$ ,  $A_1$ ,  $A_2$ ) and, when enabled, provides eight mutually exclusive active LOW outputs ( $\bar{O}_0$ – $\bar{O}_7$ ). The 'F138 features three Enable inputs, two active LOW ( $\bar{E}_1$ ,  $\bar{E}_2$ ) and one active HIGH ( $E_3$ ). All outputs will be HIGH unless  $\bar{E}_1$  and  $\bar{E}_2$  are LOW and  $E_3$  is HIGH. This multiple enable function allows easy parallel expansion

of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 'F138 devices and one inverter (See Figure 7). The 'F138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

## Truth Table

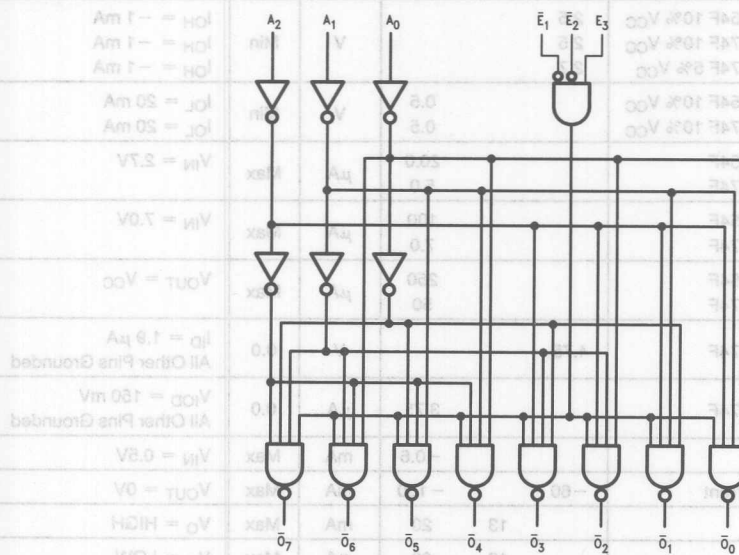
Inputs						Outputs								
$\bar{E}_1$	$\bar{E}_2$	$E_3$	$A_0$	$A_1$	$A_2$	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$	$\bar{O}_4$	$\bar{O}_5$	$\bar{O}_6$	$\bar{O}_7$	
H	X	X	X	X	X	H	H	H	H	H	H	H	H	
X	H	X	X	X	X	H	H	H	H	H	H	H	H	
X	X	L	X	X	X	H	H	H	H	H	H	H	H	
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
L	L	H	L	H	L	H	H	L	H	H	H	H	H	
L	L	H	H	H	L	H	H	H	L	H	H	H	H	
L	L	H	L	L	H	H	H	H	H	L	H	H	H	
L	L	H	H	L	H	H	H	H	H	L	H	H	H	
L	L	H	L	H	H	H	H	H	H	H	L	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	L	H	

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$   
 Ambient Temperature under Bias  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
 Junction Temperature under Bias  $-55^{\circ}\text{C}$  to  $+175^{\circ}\text{C}$

$V_{CC}$  Pin Potential to Ground Pin  $-0.5\text{V}$  to  $+7.0\text{V}$

Input Voltage (Note 2)  $-0.5\text{V}$  to  $+7.0\text{V}$

Input Current (Note 2)  $-30\text{ mA}$  to  $+5.0\text{ mA}$

Voltage Applied to Output in HIGH State (with  $V_{CC} = 0\text{V}$ )

Standard Output  $-0.5\text{V}$  to  $V_{CC}$

TRI-STATE® Output  $-0.5\text{V}$  to  $+5.5\text{V}$

Current Applied to Output in LOW State (Max) twice the rated  $I_{OL}$  (mA)

ESD Last Passing Voltage (Min)  $4000\text{V}$

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature

Military  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Commercial  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$

Supply Voltage

Military  $+4.5\text{V}$  to  $+5.5\text{V}$

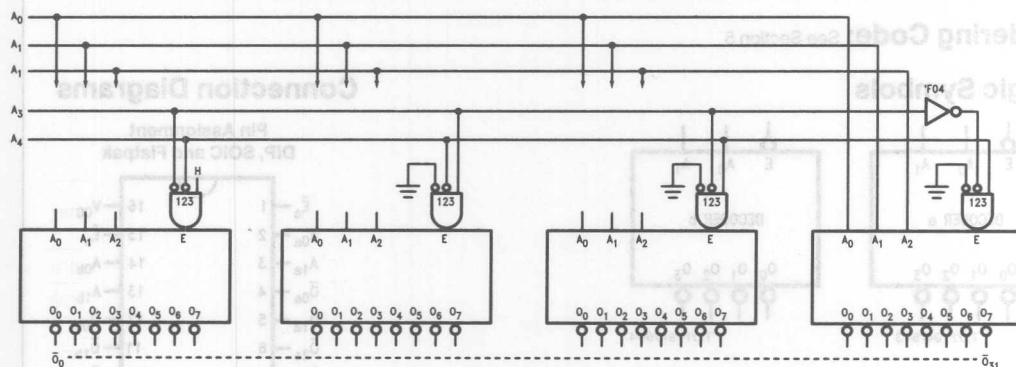
Commercial  $+4.5\text{V}$  to  $+5.5\text{V}$

## DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	$V_{CC}$	Conditions
			Min	Typ	Max			
$V_{IH}$	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
$V_{IL}$	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
$V_{CD}$	Input Clamp Diode Voltage				-1.2	V	Min	$I_{IN} = -18\text{ mA}$
$V_{OH}$	Output HIGH Voltage	54F 10% $V_{CC}$	2.5			V	Min	$I_{OH} = -1\text{ mA}$
		74F 10% $V_{CC}$	2.5					$I_{OH} = -1\text{ mA}$
		74F 5% $V_{CC}$	2.7					$I_{OH} = -1\text{ mA}$
$V_{OL}$	Output LOW Voltage	54F 10% $V_{CC}$			0.5	V	Min	$I_{OL} = 20\text{ mA}$
		74F 10% $V_{CC}$			0.5			$I_{OL} = 20\text{ mA}$
$I_{IH}$	Input HIGH Current	54F			20.0	$\mu\text{A}$	Max	$V_{IN} = 2.7\text{V}$
		74F			5.0			
$I_{BVI}$	Input HIGH Current Breakdown Test	54F			100	$\mu\text{A}$	Max	$V_{IN} = 7.0\text{V}$
		74F			7.0			
$I_{CEX}$	Output HIGH Leakage Current	54F			250	$\mu\text{A}$	Max	$V_{OUT} = V_{CC}$
		74F			50			
$V_{ID}$	Input Leakage Test	74F	4.75			V	0.0	$I_{ID} = 1.9\text{ }\mu\text{A}$ All Other Pins Grounded
$I_{OD}$	Output Leakage Circuit Current	74F			3.75	$\mu\text{A}$	0.0	$V_{IOD} = 150\text{ mV}$ All Other Pins Grounded
$I_{IL}$	Input LOW Current				-0.6	mA	Max	$V_{IN} = 0.5\text{V}$
$I_{OS}$	Output Short-Circuit Current		-60		-150	mA	Max	$V_{OUT} = 0\text{V}$
$I_{CCH}$	Power Supply Current			13	20	mA	Max	$V_O = \text{HIGH}$
$I_{CCL}$	Power Supply Current			13	20	mA	Max	$V_O = \text{LOW}$

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n$ to $\bar{O}_n$	3.5 4.0	5.6 6.1	7.5 8.0	3.5 4.0	12.0 9.5	3.5 4.0	8.5 9.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{E}_1$ or $\bar{E}_2$ to $\bar{O}_n$	3.5 3.0	5.4 5.3	7.0 7.0	3.5 3.0	11.0 8.0	3.5 3.0	8.0 7.5	ns	2-4
$t_{PLH}$ $t_{PHL}$	Propagation Delay $E_3$ to $\bar{O}_n$	4.0 3.5	6.2 5.6	8.0 7.5	4.0 3.5	12.5 8.5	4.0 3.5	9.0 8.5	ns	2-4


**FIGURE 1. Expansion to 1-of-32 Decoding**

TL/F/9478-5

Pin Name	Description	U.L.	Input/Output
$A_0$ - $A_2$	Address Inputs	1.0/1.0	Input/Output
$E_1$ - $E_3$	Enable Inputs (Active LOW)	1.0/1.0	Input/Output
$O_0$ - $O_31$	Outputs (Active LOW)	80/32.3	Output




**54F/74F139**

## Dual 1-of-4 Decoder/Demultiplexer

### General Description

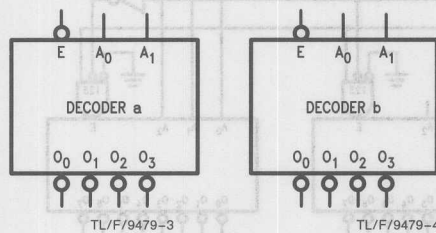
The 'F139 is a high-speed, dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the 'F139 can be used as a function generator providing all four minterms of two variables.

### Features

- Multifunction capability
- Two completely independent 1-of-4 decoders
- Active LOW mutually exclusive outputs
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

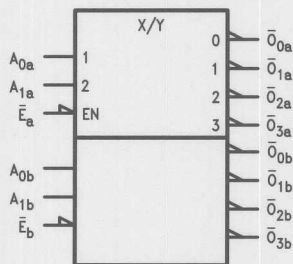
### Logic Symbols



TL/F/9479-3

TL/F/9479-4

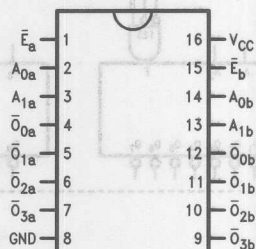
### IEEE/IEC



TL/F/9479-7

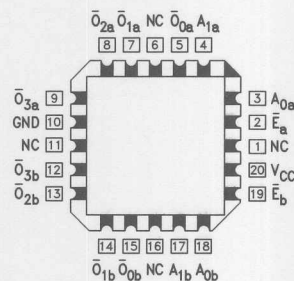
### Connection Diagrams

#### Pin Assignment DIP, SOIC and Flatpak



TL/F/9479-1

#### Pin Assignment for LCC



TL/F/9479-2

**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_0, A_1$	Address Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
$\bar{E}$	Enable Inputs (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$\bar{O}_0 - \bar{O}_3$	Outputs (Active LOW)	50/33.3	-1 mA / 20 mA

## Functional Description

The 'F139 is a high-speed dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each of which accepts two binary weighted inputs ( $A_0$ - $A_1$ ) and provides four mutually exclusive active LOW Outputs ( $\bar{O}_0$ - $\bar{O}_3$ ). Each decoder has an active LOW enable ( $\bar{E}$ ). When  $\bar{E}$  is HIGH all outputs are forced HIGH. The enable can be used

## Truth Table

Inputs			Outputs			
$\bar{E}$	$A_0$	$A_1$	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	L	L	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

as the data input for a 4-output demultiplexer application. Each half of the 'F139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Figure 1, and thereby reducing the number of packages required in a logic network.

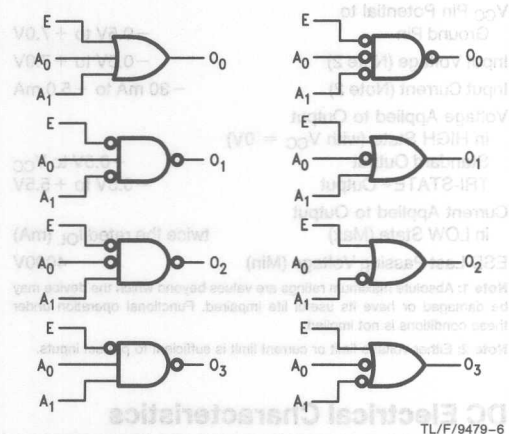
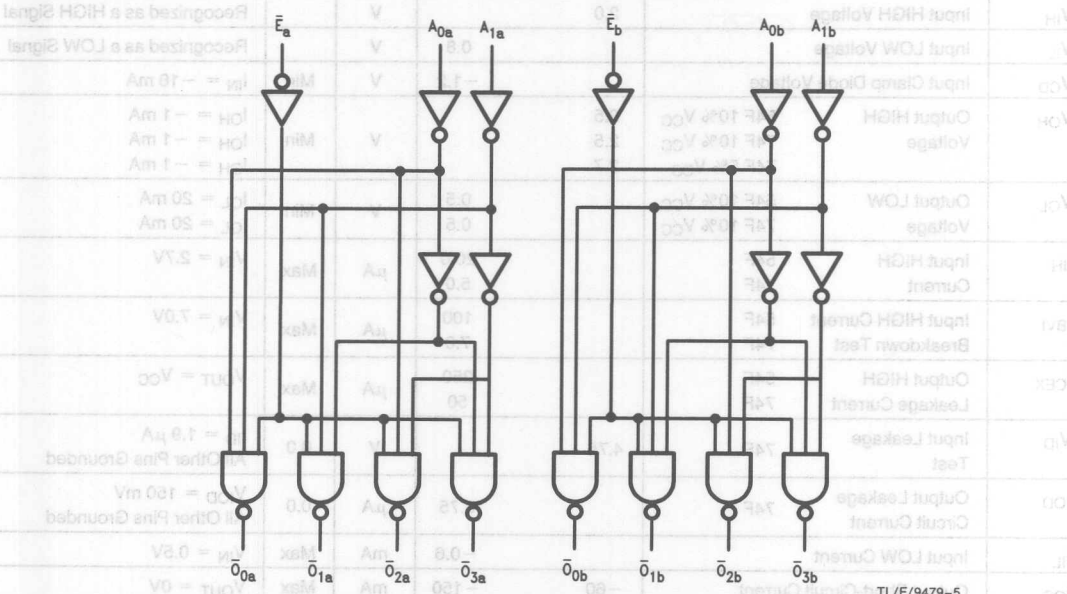


FIGURE 1. Gate Functions (each half)

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	– 65°C to + 150°C
Ambient Temperature under Bias	– 55°C to + 125°C
Junction Temperature under Bias	– 55°C to + 175°C

V <sub>CC</sub> Pin Potential to Ground Pin	– 0.5V to + 7.0V
---	------------------

Input Voltage (Note 2)	– 0.5V to + 7.0V
------------------------	------------------

Input Current (Note 2)	– 30 mA to + 5.0 mA
------------------------	---------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	– 0.5V to V <sub>CC</sub>
TRI-STATE® Output	– 0.5V to + 5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

ESD Last Passing Voltage (Min)	4000V
--------------------------------	-------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature

Military	– 55°C to + 125°C
Commercial	0°C to + 70°C

Supply Voltage

Military	+ 4.5V to + 5.5V
Commercial	+ 4.5V to + 5.5V

Outputs				Inputs		
O <sub>2</sub>	O <sub>1</sub>	O <sub>0</sub>	O <sub>0</sub>	A <sub>1</sub>	A <sub>0</sub>	E
H	H	H	H	X	X	H
H	H	H	L	L	L	L
H	H	L	H	L	H	L
H	L	H	H	L	L	L
L	H	H	H	H	H	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Indeterminate

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			– 1.2	V	Min	I <sub>IN</sub> = – 18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = – 1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = – 1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = – 1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			– 0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		– 60	– 150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		13	20	mA	Max	

		$C_L = 50 \text{ pF}$			$C_L = 50 \text{ pF}$		$C_L = 50 \text{ pF}$		ns	No.
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	3.5	5.3	7.5	2.5	12.0	3.0	8.5	ns	2-3
$t_{PHL}$	$A_0$ or $A_1$ to $\overline{O}_n$	4.0	6.1	8.0	3.5	9.5	4.0	9.0		
$t_{PLH}$	Propagation Delay	3.5	5.4	7.0	3.0	9.0	3.5	8.0	ns	2-3
$t_{PHL}$	$E_1$ to $\overline{O}_n$	3.0	4.7	6.5	2.5	8.0	3.0	7.5		

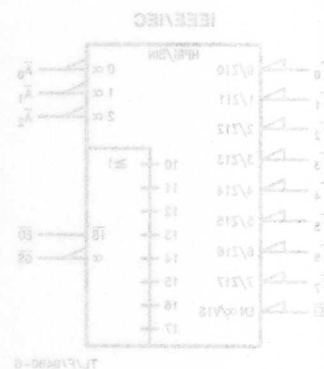
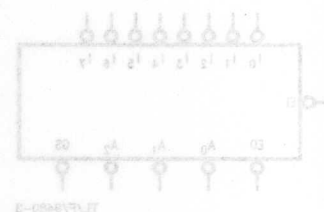
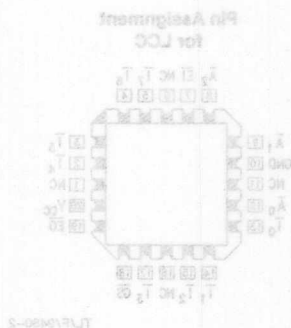
photon encoding over many bits.  
is easily expanded via input and output enables to provide  
The F148 provides 16 bits of binary code output and 16 bits of binary code input, encoding 3-2 binary code.

Carryable for priority encoding of n bits.  
Signals when data is present on any input

Ordering Code: See Section 5

## Connection Diagrams

## Logic Symbols



Unit Loading/Fan Out: See Section 5 for U.L. definitions

Pin Name	Description	U.L.	REF. 148
$\overline{A}_0$ - $\overline{A}_7$	Address Outputs (Active LOW)	50/33.3	-1 mA/20 mA
$\overline{E}_0$	Group Signal Output (Active LOW)	50/33.3	-1 mA/20 mA
$\overline{E}_1$	Enable Output (Active LOW)	50/33.3	-1 mA/20 mA
$\overline{E}_2$	Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/-0.8 mA
$\overline{E}_3$	Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/-0.8 mA
$\overline{E}_4$	Priority Input (Active LOW)	1.0/1.0	20 $\mu$ A/-0.8 mA
$\overline{E}_5$	Priority Input (Active LOW)	1.0/1.0	20 $\mu$ A/-0.8 mA
$\overline{E}_6$	Priority Input (Active LOW)	1.0/1.0	20 $\mu$ A/-0.8 mA
$\overline{E}_7$	Priority Input (Active LOW)	1.0/1.0	20 $\mu$ A/-0.8 mA


**54F/74F148**

## 8-Line to 3-Line Priority Encoder

### General Description

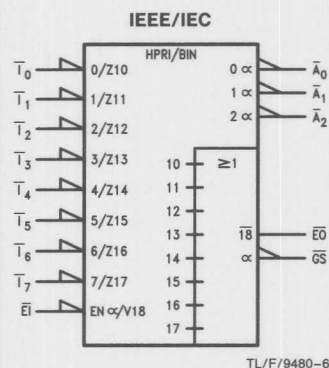
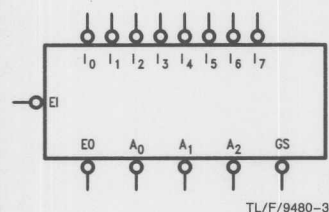
The 'F148 provides three bits of binary coded output representing the position of the highest order active input, along with an output indicating the presence of any active input. It is easily expanded via input and output enables to provide priority encoding over many bits.

### Features

- Encodes eight data lines in priority
- Provides 3-bit binary priority code
- Input enable capability
- Signals when data is present on any input
- Cascadable for priority encoding of n bits

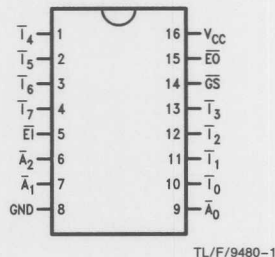
**Ordering Code:** See Section 5

### Logic Symbols

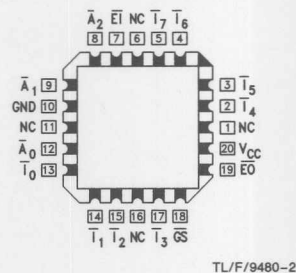


### Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak



Pin Assignment  
for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\bar{I}_0$	Priority Input (Active LOW)	1.0/1.0	20 $\mu$ A / -0.6 mA
$\bar{I}_1$ - $\bar{I}_7$	Priority Inputs (Active LOW)	1.0/2.0	20 $\mu$ A / -1.2 mA
$\bar{EI}$	Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A / -0.6 mA
$\bar{EO}$	Enable Output (Active LOW)	50/33.3	-1 mA / 20 mA
$\bar{GS}$	Group Signal Output (Active LOW)	50/33.3	-1 mA / 20 mA
$\bar{A}_0$ - $\bar{A}_2$	Address Outputs (Active LOW)	50/33.3	-1 mA / 20 mA

## Functional Description

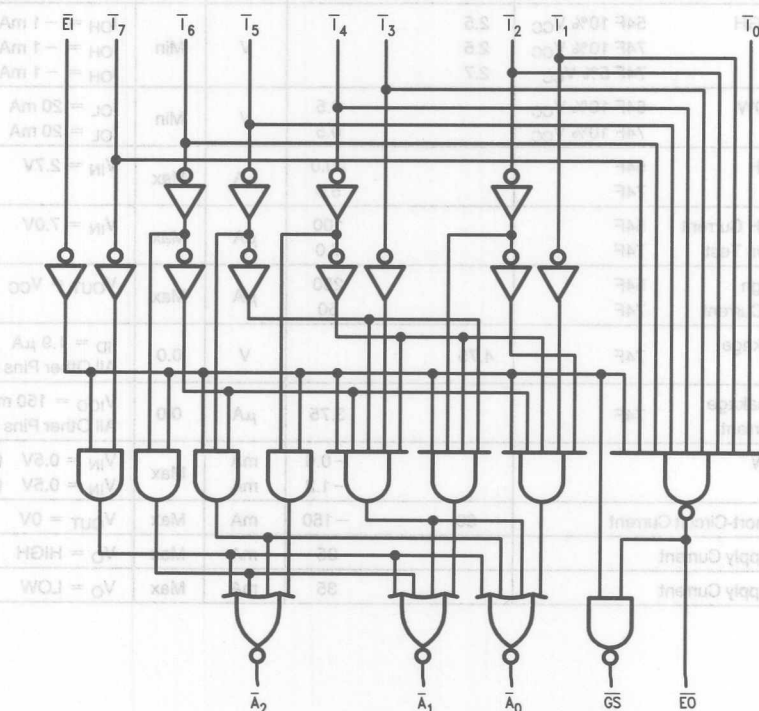
The 'F148 8-input priority encoder accepts data from eight active LOW inputs ( $\bar{I}_0$ – $\bar{I}_7$ ) and provides a binary representation on the three active LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority. A HIGH on the Enable Input ( $\bar{E}_1$ ) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs.

## Truth Table

Inputs									Outputs				
E <sub>I</sub>	I <sub>0</sub>	I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>4</sub>	I <sub>5</sub>	I <sub>6</sub>	I <sub>7</sub>	G <sub>S</sub>	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	E <sub>O</sub>
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	L	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

## Logic Diagram



TL/F/9480-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



Storage Temperature —65°C to +150°C  
 Ambient Temperature under Bias —55°C to +125°C  
 Junction Temperature under Bias —55°C to +175°C  
 $V_{CC}$  Pin Potential to Ground Pin —0.5V to +7.0V  
 Input Voltage (Note 2) —0.5V to +7.0V  
 Input Current (Note 2) —30 mA to +5.0 mA

Commercial 0°C to +70°C  
 Supply Voltage  
 Military +4.5V to +5.5V  
 Commercial +4.5V to +5.5V

Voltage Applied to Output  
 in HIGH State (with  $V_{CC} = 0V$ )  
 Standard Output —0.5V to  $V_{CC}$   
 TRI-STATE® Output —0.5V to +5.5V

Current Applied to Output  
 in LOW State (Max) twice the rated  $I_{OL}$  (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

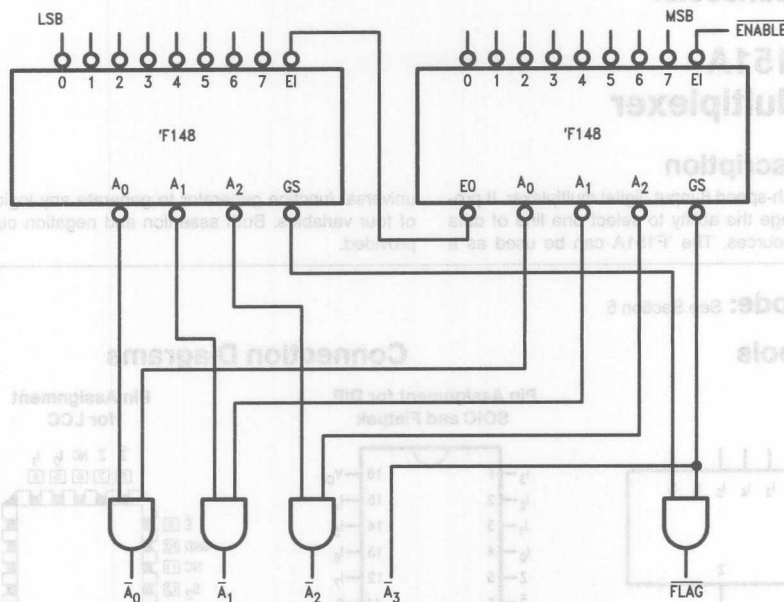
**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	$V_{CC}$	Conditions
			Min	Typ	Max			
$V_{IH}$	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
$V_{IL}$	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
$V_{CD}$	Input Clamp Diode Voltage				–1.2	V	Min	$I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	54F 10% $V_{CC}$	2.5			V	Min	$I_{OH} = -1 \text{ mA}$
		74F 10% $V_{CC}$	2.5					$I_{OH} = -1 \text{ mA}$
		74F 5% $V_{CC}$	2.7					$I_{OH} = -1 \text{ mA}$
$V_{OL}$	Output LOW Voltage	54F 10% $V_{CC}$			0.5	V	Min	$I_{OL} = 20 \text{ mA}$
		74F 10% $V_{CC}$			0.5			$I_{OL} = 20 \text{ mA}$
$I_{IH}$	Input HIGH Current	54F			20.0	$\mu\text{A}$	Max	$V_{IN} = 2.7V$
		74F			5.0			
$I_{BVI}$	Input HIGH Current Breakdown Test	54F			100	$\mu\text{A}$	Max	$V_{IN} = 7.0V$
		74F			7.0			
$I_{CEX}$	Output High Leakage Current	54F			250	$\mu\text{A}$	Max	$V_{OUT} = V_{CC}$
		74F			50			
$V_{ID}$	Input Leakage Test	74F	4.75			V	0.0	$I_{ID} = 1.9 \mu\text{A}$ All Other Pins Grounded
$I_{OD}$	Output Leakage Circuit Current	74F			3.75	$\mu\text{A}$	0.0	$V_{IOD} = 150 \text{ mV}$ All Other Pins Grounded
$I_{IL}$	Input LOW Current				–0.6	mA	Max	$V_{IN} = 0.5V$ ( $\bar{I}_0, \bar{E}_1$ )
					–1.2			$V_{IN} = 0.5V$ ( $\bar{I}_1 - \bar{I}_7$ )
$I_{OS}$	Output Short-Circuit Current		–60		–150	mA	Max	$V_{OUT} = 0V$
$I_{CCH}$	Power Supply Current				35	mA	Max	$V_O = \text{HIGH}$
$I_{CCL}$	Power Supply Current				35	mA	Max	$V_O = \text{LOW}$

## Application

### 16-Input Priority Encoder



TL/F/9480-5

### AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{I}_n$ to $\bar{A}_n$	3.0 3.0	7.0 8.0	9.0 10.5			3.0 3.0	10.0 12.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{I}_n$ to $\bar{E}\bar{O}$	2.5 2.5	5.0 5.5	6.5 7.5			2.5 2.5	7.5 8.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{I}_n$ to $\bar{G}\bar{S}$	2.5 2.5	7.0 6.0	9.0 8.0			2.5 2.5	10.0 9.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{E}\bar{I}$ to $\bar{A}_n$	2.5 2.5	6.5 6.0	8.5 8.0			2.5 2.5	9.5 9.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{E}\bar{I}$ to $\bar{G}\bar{S}$	2.5 2.5	5.0 6.0	7.0 7.5			2.5 2.5	8.0 8.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{E}\bar{I}$ to $\bar{E}\bar{O}$	2.5 3.0	5.5 8.0	7.0 10.5			2.5 3.0	8.0 12.0	ns	2-3



## 54F/74F151A 8-Input Multiplexer

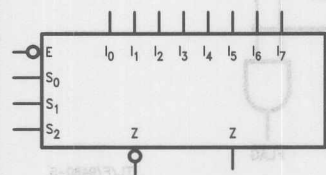
### General Description

The 'F151A is a high-speed 8-input digital multiplexer. It provides in one package the ability to select one line of data from up to eight sources. The 'F151A can be used as a

universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

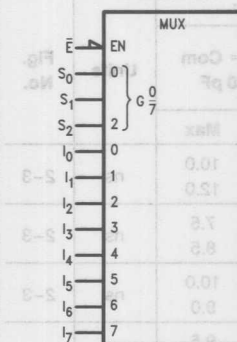
**Ordering Code:** See Section 5

### Logic Symbols



TL/F/9481-3

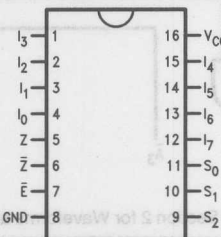
IEEE/IEC



TL/F/9481-5

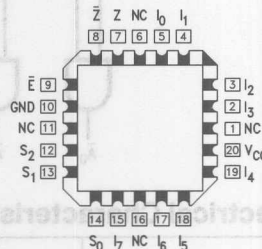
### Connection Diagrams

Pin Assignment for DIP,  
SOIC and Flatpak



TL/F/9481-1

Pin Assignment  
for LCC



TL/F/9481-2

**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_H/I_L$ Output $I_{OH}/I_{OL}$
$I_0-I_7$	Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$S_0-S_2$	Select Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
E	Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
Z	Data Output	50/33.3	-1 mA/20 mA
$\bar{Z}$	Inverted Data Output	50/33.3	-1 mA/20 mA

## Functional Description

The 'F151A is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs,  $S_0$ ,  $S_1$ ,  $S_2$ . Both assertion and negation outputs are provided. The Enable input ( $\bar{E}$ ) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \bar{E} \cdot (I_0 \bar{S}_2 \bar{S}_1 \bar{S}_0 + I_1 \bar{S}_2 \bar{S}_1 S_0 + I_2 \bar{S}_2 S_1 \bar{S}_0 + I_3 \bar{S}_2 S_1 S_0 + I_4 S_2 \bar{S}_1 \bar{S}_0 + I_5 S_2 \bar{S}_1 S_0 + I_6 S_2 S_1 \bar{S}_0 + I_7 S_2 S_1 S_0)$$

The 'F151A provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 'F151A can provide any logic function of four variables and its negation.

## Truth Table

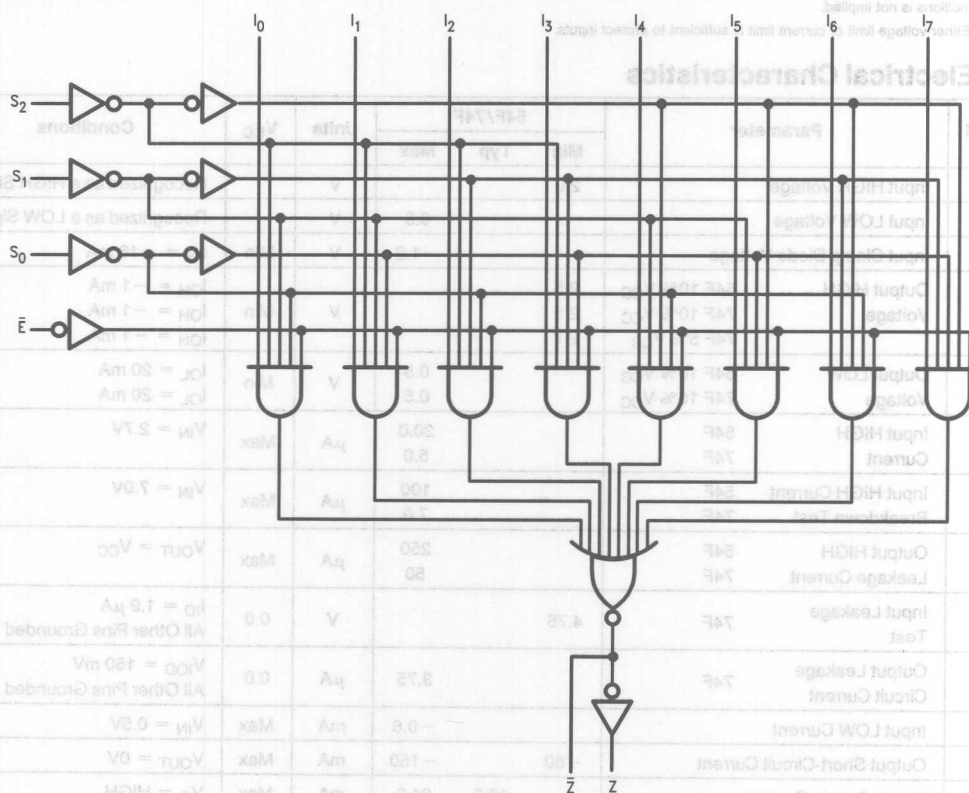
Inputs				Outputs	
$\bar{E}$	$S_2$	$S_1$	$S_0$	$\bar{Z}$	$Z$
H	X	X	X	H	L
L	L	L	L	$\bar{I}_0$	$I_0$
L	L	L	H	$\bar{I}_1$	$I_1$
L	L	H	L	$\bar{I}_2$	$I_2$
L	L	H	H	$\bar{I}_3$	$I_3$
L	H	L	L	$\bar{I}_4$	$I_4$
L	H	L	H	$\bar{I}_5$	$I_5$
L	H	H	L	$\bar{I}_6$	$I_6$
L	H	H	H	$\bar{I}_7$	$I_7$

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

TL/F/9481-4

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		13.5	21.0	mA	Max	V <sub>O</sub> = HIGH

**Recommended Operating Conditions**

Free Air Ambient Temperature

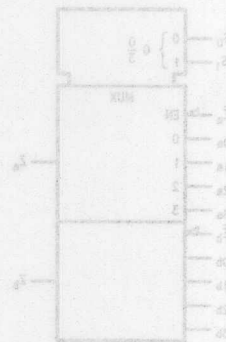
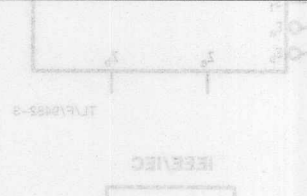
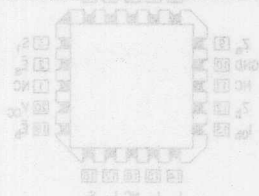
Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_n$ to $\bar{Z}$	4.0 3.2	6.2 5.2	9.0 7.5	3.5 3.0	11.5 8.0	3.5 3.2	9.5 7.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_n$ to $Z$	4.5 4.0	7.5 6.2	10.5 9.0	4.5 4.0	13.5 9.5	4.5 4.0	12.0 9.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{E}$ to $\bar{Z}$	3.0 3.0	4.7 4.4	6.1 6.0	3.0 2.5	7.5 6.5	3.0 2.5	7.0 6.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{E}$ to $Z$	5.0 3.5	7.0 5.3	9.5 7.0	4.0 3.0	12.0 8.0	4.0 3.0	10.5 7.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $I_n$ to $\bar{Z}$	3.0 1.5	4.8 2.5	6.5 4.0	2.5 1.5	7.5 6.0	3.0 1.5	7.0 5.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $I_n$ to $Z$	3.0 3.7	4.8 5.5	6.5 7.0	2.5 3.5	8.5 9.0	2.5 3.7	7.5 7.5	ns	2-3



Pin Names	Description	U.L.	
		HIGH/LOW	Input/Output
1A-13A	Side A Data Inputs	1.0/1.0	20 $\mu\text{A}$ - 0.8 mA
1A-13A	Side B Data Inputs	1.0/1.0	20 $\mu\text{A}$ - 0.8 mA
2A-14A	Common Select Inputs	1.0/1.0	20 $\mu\text{A}$ - 0.8 mA
2A-14A	Side A Enable Input (Active LOW)	1.0/1.0	20 $\mu\text{A}$ - 0.8 mA
2A-14A	Side B Enable Input (Active LOW)	1.0/1.0	20 $\mu\text{A}$ - 0.8 mA
2A-14A	Side A Output	50/50	1 mA/20 mA
2A-14A	Side B Output	50/50	1 mA/20 mA





## 54F/74F153 Dual 4-Input Multiplexer

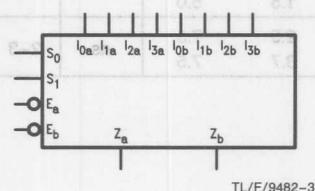
### General Description

The 'F153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The

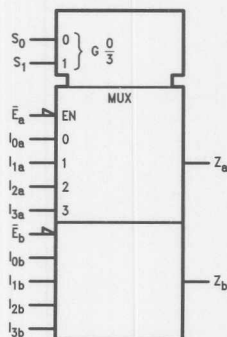
two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the 'F153 can generate any two functions of three variables.

**Ordering Code:** See Section 5

### Logic Symbols

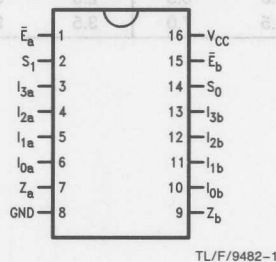


#### IEEE/IEC

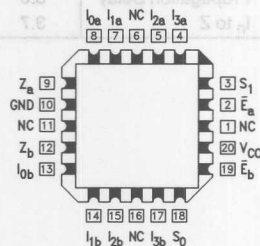


### Connection Diagrams

#### Pin Assignment for DIP, SOIC and Flatpak



#### Pin Assignment for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$I_{0a}-I_{3a}$	Side A Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$I_{0b}-I_{3b}$	Side B Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$S_0, S_1$	Common Select Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\bar{E}_a$	Side A Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\bar{E}_b$	Side B Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$Z_a$	Side A Output	50/33.3	-1 mA/20 mA
$Z_b$	Side B Output	50/33.3	-1 mA/20 mA

## Functional Description

The 'F153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs ( $S_0, S_1$ ). The two 4-input multiplexer circuits have individual active LOW Enables ( $\bar{E}_a, \bar{E}_b$ ) which can be used to strobe the outputs independently. When the Enables ( $\bar{E}_a, \bar{E}_b$ ) are HIGH, the corresponding outputs ( $Z_a, Z_b$ ) are forced LOW. The 'F153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are as follows:

$$Z_a = \bar{E}_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \bar{E}_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The 'F153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is as a function generator. The 'F153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

## Truth Table

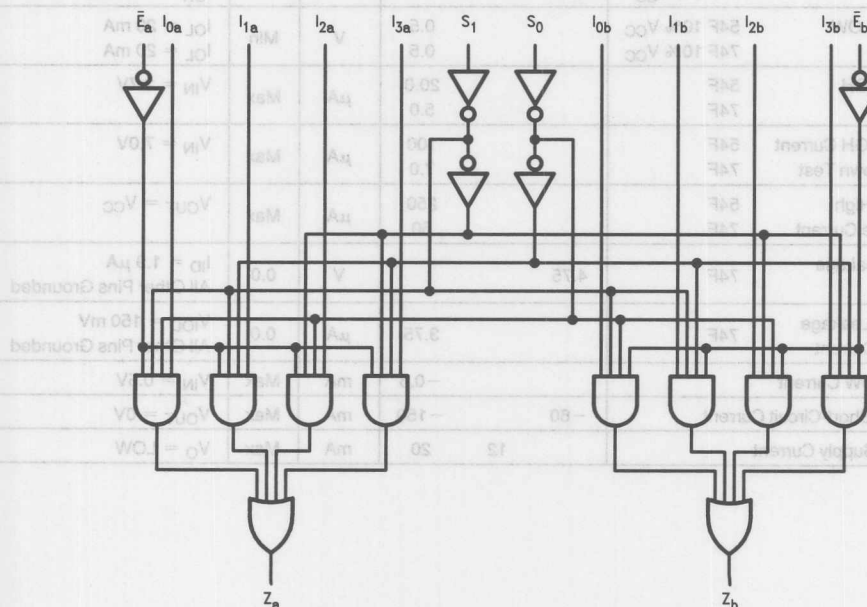
Select Inputs		Inputs (a or b)					Output
$S_0$	$S_1$	$\bar{E}$	$I_0$	$I_1$	$I_2$	$I_3$	$Z$
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	X
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level

L = LOW

X = Immaterial

## Logic Diagram



TL/F/9482-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

Ambient Temperature under Bias  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Junction Temperature under Bias  $-55^{\circ}\text{C}$  to  $+175^{\circ}\text{C}$

$V_{CC}$  Pin Potential to Ground Pin  $-0.5\text{V}$  to  $+7.0\text{V}$

Input Voltage (Note 2)  $-0.5\text{V}$  to  $+7.0\text{V}$

Input Current (Note 2)  $-30\text{ mA}$  to  $+5.0\text{ mA}$

Voltage Applied to Output in HIGH State (with  $V_{CC} = 0\text{V}$ )

Standard Output  $-0.5\text{V}$  to  $V_{CC}$

TRI-STATE® Output  $-0.5\text{V}$  to  $+5.5\text{V}$

Current Applied to Output in LOW State (Max) twice the rated  $I_{OL}$  (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	$V_{CC}$	Conditions
		Min	Typ	Max			
$V_{IH}$	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
$V_{IL}$	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
$V_{CD}$	Input Clamp Diode Voltage			-1.2	V	Min	$I_{IN} = -18\text{ mA}$
$V_{OH}$	Output HIGH Voltage	54F 10% $V_{CC}$	2.5		V	Min	$I_{OH} = -1\text{ mA}$
		74F 10% $V_{CC}$	2.5				$I_{OH} = -1\text{ mA}$
		74F 5% $V_{CC}$	2.7				$I_{OH} = -1\text{ mA}$
$V_{OL}$	Output LOW Voltage	54F 10% $V_{CC}$		0.5	V	Min	$I_{OL} = 20\text{ mA}$
		74F 10% $V_{CC}$		0.5			$I_{OL} = 20\text{ mA}$
$I_{IH}$	Input HIGH Current	54F		20.0	$\mu\text{A}$	Max	$V_{IN} = 2.7\text{V}$
		74F		5.0			
$I_{BVI}$	Input HIGH Current Breakdown Test	54F		100	$\mu\text{A}$	Max	$V_{IN} = 7.0\text{V}$
		74F		7.0			
$I_{CEX}$	Output High Leakage Current	54F		250	$\mu\text{A}$	Max	$V_{OUT} = V_{CC}$
		74F		50			
$V_{ID}$	Input Leakage Test	74F	4.75		V	0.0	$I_{ID} = 1.9\text{ }\mu\text{A}$ All Other Pins Grounded
$I_{OD}$	Output Leakage Circuit Current	74F		3.75	$\mu\text{A}$	0.0	$V_{IOD} = 150\text{ mV}$ All Other Pins Grounded
$I_{IL}$	Input LOW Current			-0.6	mA	Max	$V_{IN} = 0.5\text{V}$
$I_{OS}$	Output Short-Circuit Current		-60	-150	mA	Max	$V_{OUT} = 0\text{V}$
$I_{CCL}$	Power Supply Current		12	20	mA	Max	$V_O = \text{LOW}$

## Recommended Operating Conditions

Free Air Ambient Temperature

Military  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Commercial  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$

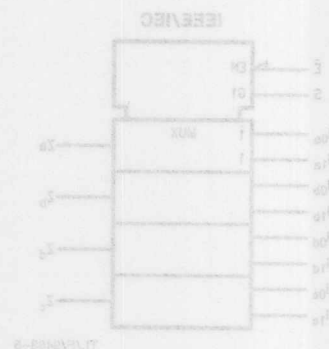
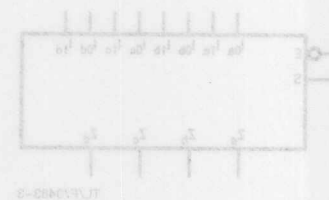
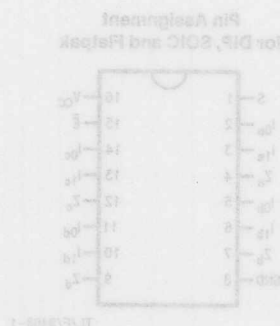
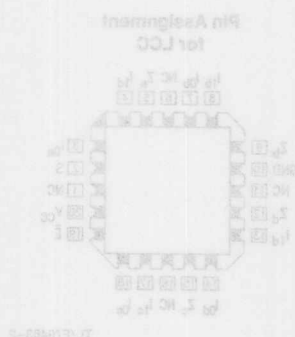
Supply Voltage

Military  $+4.5\text{V}$  to  $+5.5\text{V}$

Commercial  $+4.5\text{V}$  to  $+5.5\text{V}$

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	4.5	8.1	10.5	4.5	14.0	4.5	12.0	ns	2-3
$t_{PHL}$	$S_n$ to $Z_n$	3.5	7.0	9.0	3.5	11.0	3.5	10.5		
$t_{PLH}$	Propagation Delay	4.5	7.1	9.0	4.5	11.5	4.5	10.5	ns	2-3
$t_{PHL}$	$\bar{E}_n$ to $Z_n$	3.0	5.7	7.0	2.5	9.0	2.5	8.0		
$t_{PLH}$	Propagation Delay	3.0	5.3	7.0	2.5	9.0	3.0	8.0	ns	2-3
$t_{PHL}$	$I_n$ to $Z_n$	2.5	5.1	6.5	2.5	8.0	2.5	7.5		



Pin Names	Description	EAT/74F	
		U.L.	Input/Output
$I_{0-10}$	Source 0 Data Inputs	1.0/1.0	50 $\mu\text{A}$ - 0.8 mA
$I_{1-10}$	Source 1 Data Inputs	1.0/1.0	50 $\mu\text{A}$ - 0.8 mA
$\bar{E}$	Enable Input (Active LOW)	1.0/1.0	50 $\mu\text{A}$ - 0.8 mA
$S$	Select Input	1.0/1.0	50 $\mu\text{A}$ - 0.8 mA
$Z_{0-10}$	Outputs	50/33.3	- 1 mA/50 mA


**54F/74F157A**

## Quad 2-Input Multiplexer

### General Description

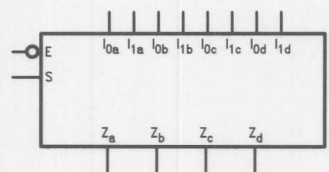
The 'F157A is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (non-inverted) form. The 'F157A can also be used to generate any four of the 16 different functions to two variables.

### Features

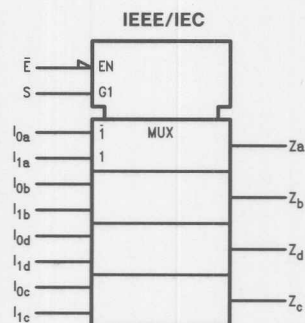
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

### Logic Symbols



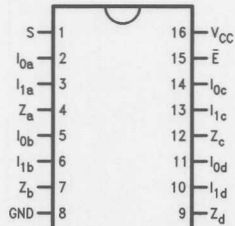
TL/F/9483-3



TL/F/9483-5

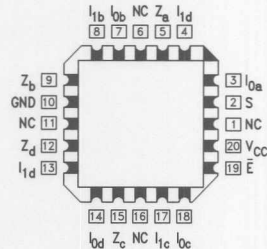
### Connection Diagrams

Pin Assignment  
for DIP, SOIC and Flatpak



TL/F/9483-1

Pin Assignment  
for LCC



TL/F/9483-2

**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$I_{0a}-I_{0d}$	Source 0 Data Inputs	1.0/1.0	20 $\mu$ A / -0.6 mA
$I_{1a}-I_{1d}$	Source 1 Data Inputs	1.0/1.0	20 $\mu$ A / -0.6 mA
$\bar{E}$	Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A / -0.6 mA
S	Select Input	1.0/1.0	20 $\mu$ A / -0.6 mA
$Z_a-Z_d$	Outputs	50/33.3	-1 mA/20 mA

Functional Description

The 'F157A is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ( $\bar{E}$ ) is active LOW. When  $\bar{E}$  is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The 'F157A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_n = \bar{E} \cdot (I_{1n} S + I_{0n} \bar{S})$$

A common use of the 'F157A is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The 'F157A can generate any four of the

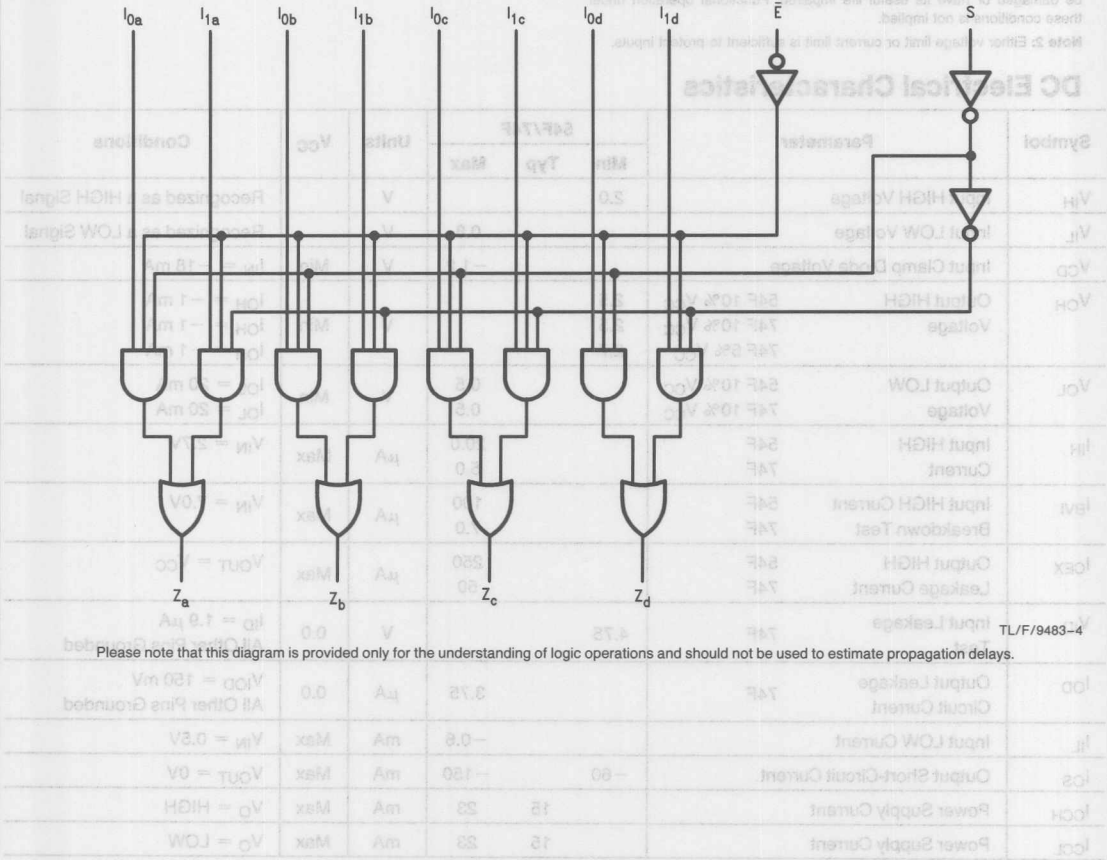
Absolute Maximum Ratings (Note 1)  
16 different functions of two variables, with one variable common. This is useful for implementing highly irregular logic.

Truth Table

Inputs				Output
$\bar{E}$	S	$I_0$	$I_1$	Z
H	X	X	X	L
L	H	X	X	H
L	L	X	X	L
L	L	L	H	L
L	L	H	L	H
L	L	L	L	L
L	L	H	H	H

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

Logic Diagram





**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature		-65°C to +150°C
Ambient Temperature under Bias		-55°C to +125°C
Junction Temperature under Bias		-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin		-0.5V to +7.0V
Input Voltage (Note 2)	X	-0.5V to +7.0V
Input Current (Note 2)	X	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	X	-0.5V to V <sub>CC</sub>
Standard Output	X	-0.5V to +5.5V
TRI-STATE® Output	H	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)		twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)		4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		15	23	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		15	23	mA	Max	V <sub>O</sub> = LOW

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	-55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay S to $Z_n$	4.0 3.0	7.0 5.0	10.0 7.0	4.0 3.0	12.0 9.0	4.0 3.0	11.0 8.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{E}$ to $Z_n$	5.0 2.5	7.0 4.5	9.5 6.5	5.0 2.5	13.0 7.5	5.0 2.5	11.0 7.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $I_n$ to $Z_n$	2.5 2.5	4.5 4.0	6.0 5.5	2.5 1.5	7.5 7.5	2.5 2.0	6.5 7.0	ns	2-3



54F/74F158A

## Quad 2-Input Multiplexer

## General Description

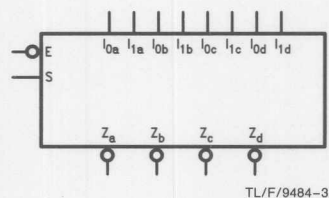
The 'F158A is a high speed quad 2-input multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four outputs present the selected data in the inverted form. The 'F158A can also generate any four of the 16 different functions of two variables.

## Features

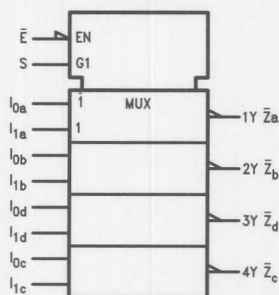
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

## Logic Symbols

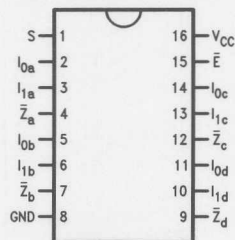


## IEEE/IEC

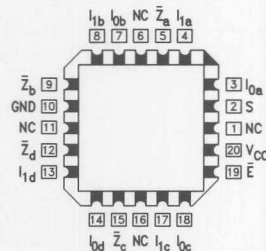


## Connection Diagrams

## Pin Assignment for DIP, SOIC and Flatpak



## Pin Assignment for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

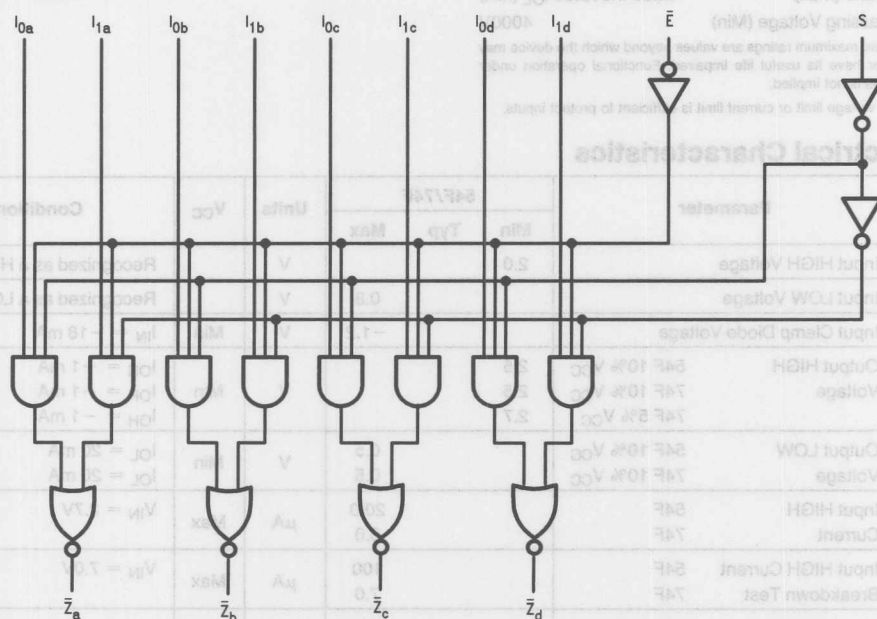
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$I_{0a}-I_{0d}$	Source 0 Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$I_{1a}-I_{1d}$	Source 1 Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\bar{E}$	Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
S	Select Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\bar{Z}_a-\bar{Z}_d$	Inverted Outputs	50/33.3	-1 mA/20 mA

## Functional Description

The 'F158A quad 2-input multiplexer selects four bits of data from two sources under the control of a common Select input (S) and presents the data in inverted form at the four outputs. The Enable input ( $\bar{E}$ ) is active LOW. When  $\bar{E}$  is HIGH, all of the outputs ( $\bar{Z}$ ) are forced HIGH regardless of all other inputs. The 'F158A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

A common use of the 'F158A is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The 'F158A can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Truth Table

Inputs				Outputs
$\bar{E}$	S	$I_0$	$I_1$	$\bar{Z}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

$Z_n = \bar{E} \times (I_{1n} S + I_{0n} \bar{S})$

TL/F/9484-4

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	-0.5V to V <sub>CC</sub>
Standard Output TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

ESD Last Passing Voltage (Min) 4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		10	15	mA	Max	V <sub>O</sub> = LOW

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	-55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

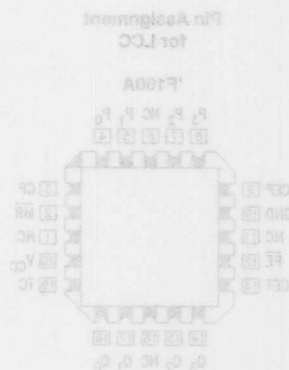
**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay S to $\bar{Z}_n$	3.0 2.5	5.5 4.5	8.5 6.5	3.0 2.5	10.5 8.0	3.0 2.5	9.5 7.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{E}$ to $\bar{Z}_n$	2.5 2.0	4.5 4.0	6.0 6.0	2.5 2.0	8.0 7.0	2.5 2.0	7.0 6.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $I_n$ to $\bar{Z}_n$	2.5 1.5	4.0 2.5	5.9 4.0	2.5 1.0	8.5 5.0	2.5 1.5	7.0 4.5	ns	2-3

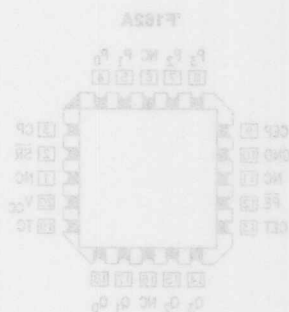
■ Synchronous counting and loading  
■ High-speed synchronous expansion  
■ Typical count rate of 150 MHz  
■ Guaranteed 500V minimum ESD protection

Ordering Code: See Section 2

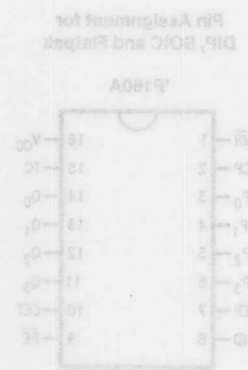
Connection Diagrams



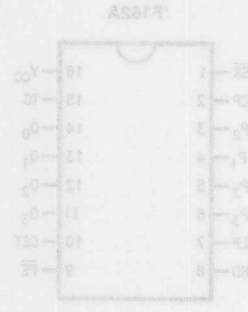
S-284965-5



S-284965-10



S-284965-1



S-284965-3





## 54F/74F160A • 54F/74F162A

### Synchronous Presettable BCD Decade Counter

#### General Description

The 'F160A and 'F162A are high-speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for applications in programmable dividers. There are two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'F160A has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'F162A has a Synchronous Reset input that overrides counting and parallel load-

ing and allows all outputs to be simultaneously reset on the rising edge of the clock. The 'F160A and 'F162A are high speed versions of the 'F160 and 'F162.

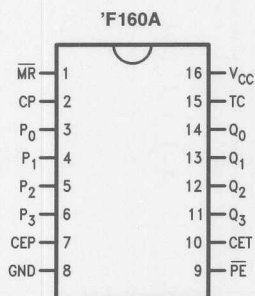
#### Features

- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count rate of 120 MHz
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

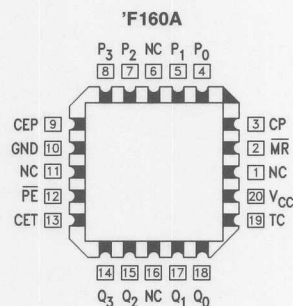
#### Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak

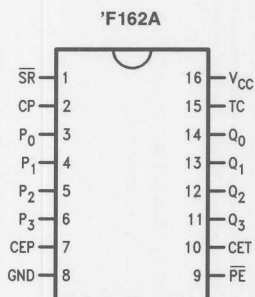


TL/F/9485-1

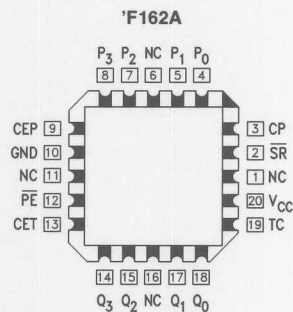
Pin Assignment  
for LCC



TL/F/9485-2

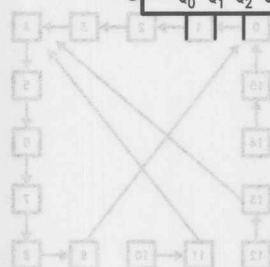
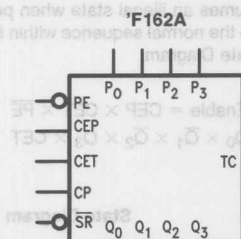


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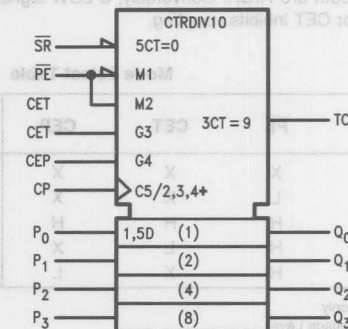


TL/F/9485-10

The diagram shows a square integrated circuit with pins numbered 0 to 3 on the top and bottom edges. On the left edge, pins are labeled PE, CEP, CET, CP, and MR. On the right edge, a pin is labeled TC. The top of the chip is labeled 'F160A and the bottom is labeled 'F162A.



TL/E/9485-8



TL/F/9485-7

4

## Functional Description

The 'F160A and 'F162A count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the 'F160A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('F160A), synchronous reset ('F162A), parallel load, count-up and hold. Five control inputs—Master Reset ( $\overline{MR}$ , 'F160A), Synchronous Reset ( $\overline{SR}$ , 'F162A), Parallel Enable ( $\overline{PE}$ ), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on  $\overline{MR}$  overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on  $\overline{SR}$  overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on  $\overline{PE}$  overrides counting and allows information on the Parallel Data ( $P_n$ ) inputs to be loaded into the flip-flops on the next rising edge of CP. With  $\overline{PE}$  and  $\overline{MR}$  ('F160A) or  $\overline{SR}$  ('F162A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

Mode Select Table

* $\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge ( $\nearrow$ )
L	X	X	X	Reset (Clear)
H	L	X	X	Load ( $P_n \rightarrow Q_n$ )
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

\*For 'F162A only  
H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

The 'F160A and 'F162A use D-type edge-triggered flip-flops and changing the  $\overline{SR}$ ,  $\overline{PE}$ , CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

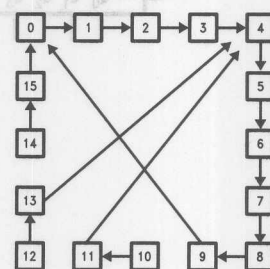
The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 9. To implement synchronous multi-stage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the 'F568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the 'F160A and 'F162A decade counters, the TC output is fully decoded and can only be HIGH in state 9. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the State Diagram.

Logic Equations:

$$\text{Count Enable} = \text{CEP} \times \text{CET} \times \overline{\text{PE}}$$

$$\text{TC} = Q_0 \times \overline{Q_1} \times \overline{Q_2} \times Q_3 \times \text{CET}$$

State Diagram



TL/F/9485-4

Pin Names	Description	U.L. HIGH/LOW	Input/Output
TC	Terminal Count Output	50/100	Am
Q <sub>0</sub> -Q <sub>3</sub>	Flip-Flop Outputs	50/100	Am
$\overline{PE}$	Parallel Enable Input (Active LOW)	50/100	Am
P <sub>0</sub> -P <sub>3</sub>	Parallel Data Inputs	50/100	Am
$\overline{SR}$ ('F162A)	Synchronous Reset Input (Active LOW)	50/100	Am
$\overline{MR}$ ('F160A)	Asynchronous Master Reset Input (Active LOW)	50/100	Am
CP	Clock Pulse Input (Active Rising Edge)	50/100	Am
CET	Count Enable Trickle Input	50/100	Am
CEP	Count Enable Parallel Input	50/100	Am



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**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage		0.8			V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage		−1.2			V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5			V	Min	I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.5					I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>	0.5			V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>	0.5					I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F	20.0			μA	Max	V <sub>IN</sub> = 2.7V
		74F	5.0					
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F	100			μA	Max	V <sub>IN</sub> = 7.0V
		74F	7.0					
I <sub>CEX</sub>	Output HIGH Leakage Current	54F	250			μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F	50					
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F	3.75			μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current				−0.6	mA	Max	V <sub>IN</sub> = 0.5V (CP, CEP, P <sub>n</sub> , $\overline{MR}$ ('F160A)) V <sub>IN</sub> = 0.5V (CET, $\overline{SR}$ ('F162A), $\overline{PE}$ )
					−1.2			
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150		mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		37	55		mA	Max	V <sub>O</sub> = HIGH

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Count Frequency	90	120		75		80		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay, Count	3.5	5.5	7.5	3.5	9.0	3.5	8.5	ns	2-3
$t_{\text{PHL}}$	CP to $Q_n$ ( $\overline{\text{PE}}$ Input HIGH)	3.5	7.5	10.0	3.5	11.5	3.5	11.0		
$t_{\text{PLH}}$	Propagation Delay, Load	4.0	6.0	8.5	4.0	10.0	4.0	9.5	ns	2-3
$t_{\text{PHL}}$	CP to $Q_n$ ( $\overline{\text{PE}}$ Input LOW)	4.0	6.0	8.5	4.0	10.0	4.0	9.5		
$t_{\text{PLH}}$	Propagation Delay	5.0	10.0	14.0	5.0	16.5	5.0	15.0	ns	2-3
$t_{\text{PHL}}$	CP to TC	5.0	10.0	14.0	5.0	15.5	5.0	15.0		
$t_{\text{PLH}}$	Propagation Delay	2.5	4.5	7.5	2.5	9.0	2.5	8.5	ns	2-3
$t_{\text{PHL}}$	CET to TC	2.5	4.5	7.5	2.5	9.0	2.5	8.5		
$t_{\text{PHL}}$	Propagation Delay MR to $Q_n$ ('F160A)	5.5	9.0	12.0	5.5	14.0	5.5	13.0	ns	2-3
$t_{\text{PHL}}$	Propagation Delay MR to TC ('F160A)	4.5	8.0	10.5	4.5	12.5	4.5	11.5	ns	2-3



**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $P_n$ to CP ('F160A)	4.0 5.0		5.5 5.5		4.0 5.0		ns	2-6
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $P_n$ to CP ('F162A)	5.0 5.0		5.5 5.5		5.0 5.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $P_n$ to CP	2.0 2.0		2.5 2.5		2.0 2.0			
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $\overline{\text{PE}}$ or $\overline{\text{SR}}$ to CP	11.0 8.5		13.5 10.5		11.5 9.5		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $\overline{\text{PE}}$ or $\overline{\text{SR}}$ to CP	2.0 0		2.0 0		2.0 0			
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW CEP or CET to CP	11.0 5.0		13.0 6.0		11.5 5.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW CEP or CET to CP	0 0		0 0		0 0			
$t_w(\text{H})$ $t_w(\text{L})$	Clock Pulse Width (Load) HIGH or LOW	5.0 5.0		5.0 5.0		5.0 5.0		ns	2-4
$t_w(\text{H})$ $t_w(\text{L})$	Clock Pulse Width (Count) HIGH or LOW	4.0 6.0		5.0 8.0		4.0 7.0		ns	2-4
$t_w(\text{L})$	$\overline{\text{MR}}$ Pulse Width, LOW ( 'F160A)	5.0		5.0		5.0			
$t_{\text{rec}}$	Recovery Time $\overline{\text{MR}}$ to CP ('F160A)	6.0		6.0		6.0		ns	2-6



## 54F/74F161A • 54F/74F163A Synchronous Presettable Binary Counter

### General Description

The 'F161A and 'F163A are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multi-stage counters. The 'F161A has an asynchronous Master-Reset input that overrides all other inputs and forces the outputs LOW. The 'F163A has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock. The 'F161A and 'F163A are high-speed versions of the 'F161 and 'F163.

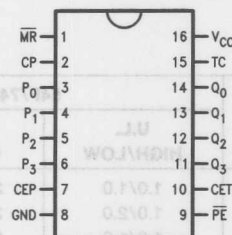
### Features

- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count frequency of 120 MHz
- Guaranteed 4000V minimum ESD protection

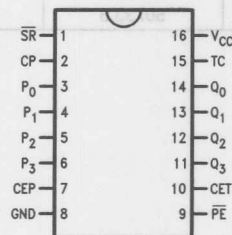
**Ordering Code:** See Section 5

### Connection Diagrams

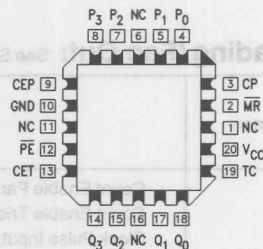
**Pin Assignment  
for DIP, SOIC and Flatpak  
'F161A**



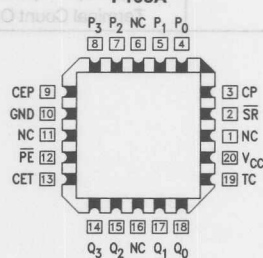
**Pin Assignment  
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'F163A**



**Pin Assignment  
for LCC  
'F161A**



**Pin Assignment  
for LCC  
'F163A**



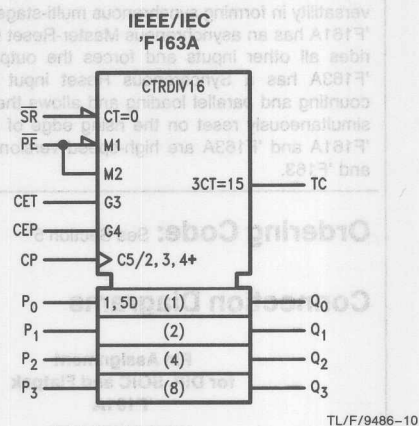
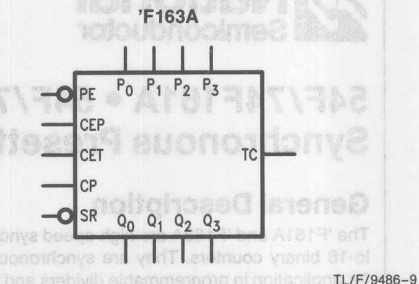
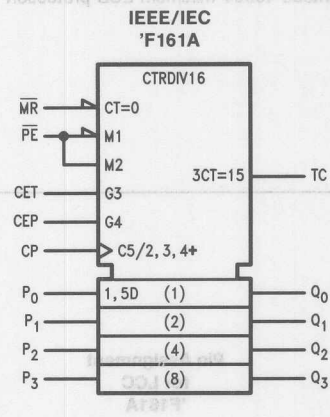
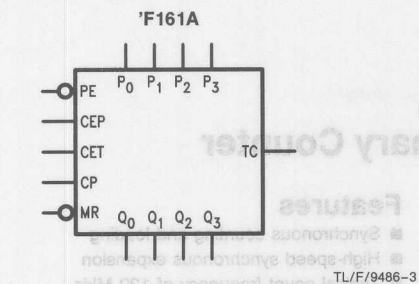
TL/F/9486-1

TL/F/9486-2

TL/F/9486-7

TL/F/9486-8

## Logic Symbols



## Unit Loading/Fan Out: See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I <sub>IH</sub> /I <sub>IL</sub> Output I <sub>OH</sub> /I <sub>OL</sub>
CEP	Count Enable Parallel Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
CET	Count Enable Trickle Input	1.0/2.0	20 $\mu$ A/ -1.2 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{MR}$ ('F161A)	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
SR ('F163A)	Synchronous Reset Input (Active LOW)	1.0/2.0	20 $\mu$ A/ -1.2 mA
P <sub>0</sub> -P <sub>3</sub>	Parallel Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/2.0	20 $\mu$ A/ -1.2 mA
Q <sub>0</sub> -Q <sub>3</sub>	Flip-Flop Outputs	50/33.3	-1 mA/20 mA
TC	Terminal Count Output	50/33.3	-1 mA/20 mA

## Functional Description

The 'F161A and 'F163A count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the 'F161A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('F161A), synchronous reset ('F163A), parallel load, count-up and hold. Five control inputs—Master Reset ( $\overline{MR}$ , 'F161A), Synchronous Reset ( $\overline{SR}$ , 'F163A), Parallel Enable ( $\overline{PE}$ ), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on  $\overline{MR}$  overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on  $\overline{SR}$  overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on  $\overline{PE}$  overrides counting and allows information on the Parallel Data ( $P_n$ ) inputs to be loaded into the

flip-flops on the next rising edge of CP. With  $\overline{PE}$  and  $\overline{MR}$  ('F161A) or  $\overline{SR}$  ('F163A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'F161A and 'F163A use D-type edge triggered flip-flops and changing the  $\overline{SR}$ ,  $\overline{PE}$ , CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in state 15. To implement synchronous multi-stage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the 'F568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

Logic Equations: Count Enable =  $\text{CEP} \cdot \text{CET} \cdot \overline{PE}$

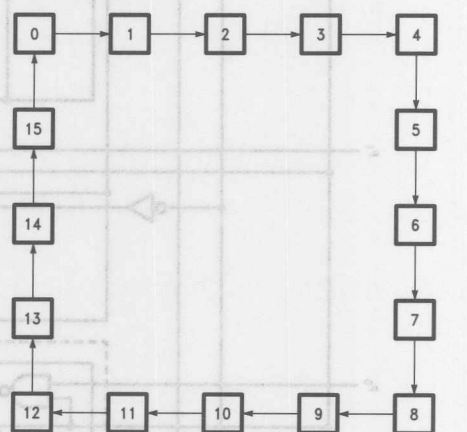
$$\text{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \text{CET}$$

Mode Select Table

* $\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge ( $\nearrow$ )
L	X	X	X	Reset (Clear)
H	L	X	X	Load ( $P_n \rightarrow Q_n$ )
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

\*For 'F163A only  
H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

## State Diagram



TL/F/9486-5

## 486-4

Ambient Temperature under Bias	−55°C to +125°C	Commercial	0°C to +70°C
Junction Temperature under Bias	−55°C to +175°C	Supply Voltage	
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V	Military	+4.5V to +5.5V
Input Voltage (Note 2)	−0.5V to +7.0V	Commercial	+4.5V to +5.5V
Input Current (Note 2)	−30 mA to +5.0 mA		
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)			
Standard Output	−0.5V to V <sub>CC</sub>		
TRI-STATE® Output	−0.5V to +5.5V		
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)		
ESD Last Passing Voltage (Min)	4000V		
<b>Note 1:</b> Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.			
<b>Note 2:</b> Either voltage limit or current limit is sufficient to protect inputs.			

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.5 2.7		V	Min	I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6 −1.2	mA	Max	V <sub>IN</sub> = 0.5V (CEP, CP, MR, P <sub>0</sub> –P <sub>3</sub> ) V <sub>IN</sub> = 0.5V (CET, PE, SR)
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		37	55	mA	Max	



**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Count Frequency	100	120		75		90		MHz	2-1
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $Q_n$ ( $\overline{\text{PE}}$ Input HIGH)	3.5 3.5	5.5 7.5	7.5 10.0	3.5 3.5	9.0 11.5	3.5 3.5	8.5 11.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $Q_n$ ( $\overline{\text{PE}}$ Input LOW)	4.0 4.0	6.0 6.0	8.5 8.5	4.0 4.0	10.0 10.0	4.0 4.0	9.5 9.5		
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to TC	5.0 5.0	10.0 10.0	14.0 14.0	5.0 5.0	16.5 15.5	5.0 5.0	15.0 15.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CET to TC	2.5 2.5	4.5 4.5	7.5 7.5	2.5 2.5	9.0 9.0	2.5 2.5	8.5 8.5	ns	2-3
$t_{\text{PHL}}$	Propagation Delay MR to $Q_n$ ('F161A)	5.5	9.0	12.0	5.5	14.0	5.5	13.0	ns	2-3
$t_{\text{PHL}}$	Propagation Delay MR to TC ('F161A)	4.5	8.0	10.5	4.5	12.5	4.5	11.5	ns	2-3

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	5.0		5.5		5.0		ns	2-6
$t_s(\text{L})$	$P_n$ to CP	5.0		5.5		5.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0		2.5		2.0		ns	2-6
$t_h(\text{L})$	$P_n$ to CP	2.0		2.5		2.0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	11.0		13.5		11.5		ns	2-6
$t_s(\text{L})$	$\overline{\text{PE}}$ or $\overline{\text{SR}}$ to CP	8.5		10.5		9.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0		3.6		2.0		ns	2-6
$t_h(\text{L})$	$\overline{\text{PE}}$ or $\overline{\text{SR}}$ to CP	0		0		0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	11.0		13.0		11.5		ns	2-6
$t_s(\text{L})$	CEP or CET to CP	5.0		6.0		5.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		0		0		ns	2-6
$t_h(\text{L})$	CEP or CET to CP	0		0		0			
$t_w(\text{H})$	Clock Pulse Width (Load)	5.0		5.0		5.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	5.0		5.0		5.0			
$t_w(\text{H})$	Clock Pulse Width (Count)	4.0		5.0		4.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	6.0		8.0		7.0			
$t_w(\text{L})$	$\overline{\text{MR}}$ Pulse Width, LOW ( $^{\circ}\text{F161A}$ )	5.0		5.0		5.0		ns	2-4
$t_{\text{rec}}$	Recovery Time $\overline{\text{MR}}$ to CP ( $^{\circ}\text{F161A}$ )	6.0		6.0		6.0		ns	2-6



## 54F/74F164A Serial-In, Parallel-Out Shift Register

### General Description

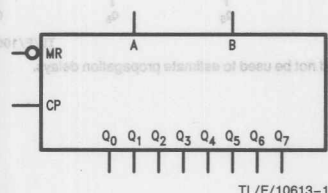
The 'F164A is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock. The 'F164A is a faster version of the 'F164.

### Features

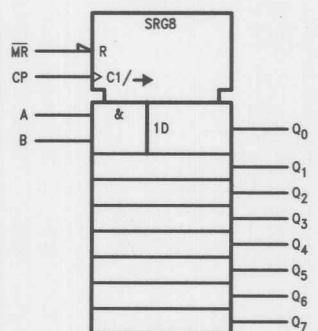
- Typical shift frequency of 90 MHz
- Asynchronous Master Reset
- Gated serial data input
- Fully synchronous data transfers
- Guaranteed 4000V min ESD protection
- 'F164A is a faster version of the 'F164

**Ordering Code:** See Section 5

### Logic Symbols



#### IEEE/IEC

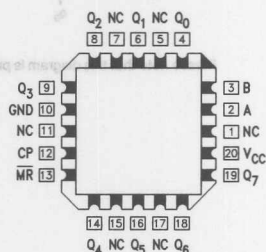


### Connection Diagrams

#### Pin Assignment for DIP, SOIC and Flatpak



#### Pin Assignment for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
A, B	Data Inputs	1.0/1.0	20 $\mu$ A / -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A / -0.6 mA
MR	Master Reset Input (Active LOW)	1.0/1.0	20 $\mu$ A / -0.6 mA
Q0-Q7	Outputs	50/33.3	-1 mA / 20 mA

## Functional Description

The 'F164A is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into  $Q_0$  the logical AND of the two data inputs ( $A \cdot B$ ) that existed before the rising clock edge. A LOW level on the Master Reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

Mode Select Table

Operating Mode	Inputs			Outputs	
	MR	A	B	$Q_0$	$Q_1-Q_7$
Reset (Clear)	L	X	X	L	L-L
Shift	H	l	l	L	$Q_0-Q_6$
	H	l	h	L	$Q_0-Q_6$
	H	h	l	L	$Q_0-Q_6$
	H	h	h	H	$Q_0-Q_6$

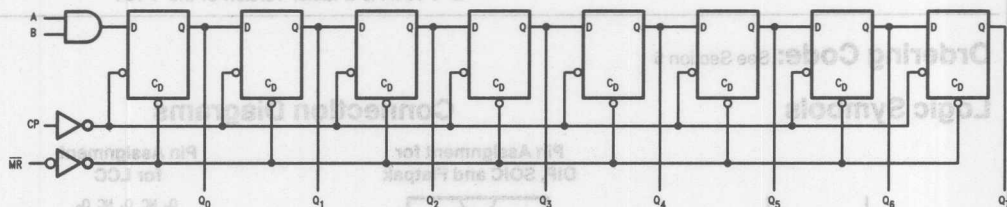
H(h) = HIGH Voltage Levels

L(l) = LOW Voltage Levels

X = Immaterial

$Q_n$  = Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
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Input Voltage (Note 2)	–0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	–30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	–0.5V to V <sub>CC</sub>
Standard Output	–0.5V to +5.5V
TRI-STATE® Output	–0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
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ESD Last Passing Voltage (Min)	4000V
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**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	–55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			–1.2	V	Min	I <sub>IN</sub> = –18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = –1 mA
		74F 10% V <sub>CC</sub>	2.5		V		I <sub>OH</sub> = –1 mA
		74F 5% V <sub>CC</sub>	2.7		V		I <sub>OH</sub> = –1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5	V		I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0	μA	Max	
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0	μA	Max	
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50	μA	Max	
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All other pins grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All other pins grounded
I <sub>IL</sub>	Input LOW Current			–0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	–60		–150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		35	55	mA	Max	CP = HIGH MR = GND, A, B = GND

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	80	120				80		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay CP to $Q_n$	3.0	4.8	7.5			3.0	7.5	ns	2-3
$t_{\text{PHL}}$	Propagation Delay CP to $Q_n$	3.5	5.0	8.0			3.5	8.0		
$t_{\text{PHL}}$	Propagation Delay $\overline{\text{MR}}$ to $Q_n$	5.0	7.0	10.0			5.0	10.5	ns	2-3

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	4.5				4.5		ns	2-6
$t_s(\text{L})$	A or B to CP	4.0				4.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	1.0				1.0		ns	2-4
$t_h(\text{L})$	A or B to CP	1.0				1.0			
$t_w(\text{H})$	CP Pulse Width	4.0				4.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	7.0				7.0			
$t_w(\text{L})$	$\overline{\text{MR}}$ Pulse Width, LOW	4.0				4.0		ns	2-4
$t_{\text{rec}}$	Recovery Time $\overline{\text{MR}}$ to CP	5.0				5.0		ns	2-6
$V_{OL}$	Output LOW Voltage	0.2		0.2		0.2			
$I_{IH}$	Input HIGH Current	20.0		20.0		20.0			
$I_{IL}$	Input LOW Current	100		100		100			
$I_{OZ}$	Output HIGH Leakage Current	250		250		250			
$V_{ID}$	Input Leakage Test	0.0		0.0		0.0			
$I_{OD}$	Output Leakage Current	2.5		2.5		2.5			
$I_{IL}$	Input LOW Current	0.0		0.0		0.0			
$I_{OS}$	Output Short-Circuit Current	150		150		150			
$I_{CC}$	Power Supply Current	25		25		25			

## 54F/74F168 • 54F/74F169 4-Stage Synchronous Bidirectional Counters

### General Description

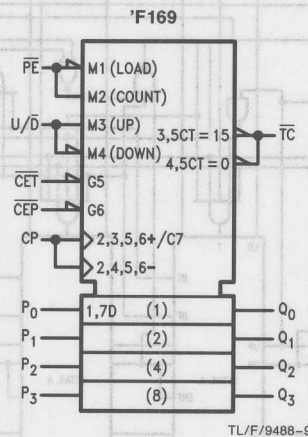
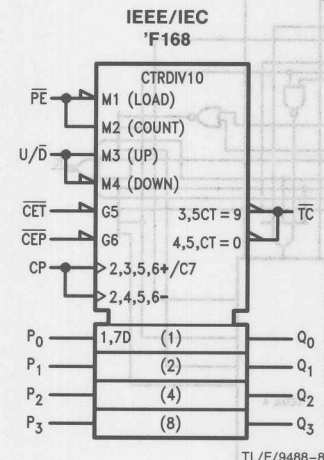
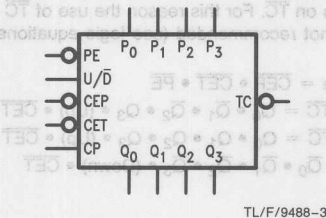
The 'F168 and 'F169 are fully synchronous 4-stage up/down counters. The 'F168 is a BCD decade counter; the 'F169 is a modulo-16 binary counter. Both feature a preset capability for programmable operation, carry lookahead for easy cascading and a U/D input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

### Features

- Asynchronous counting and loading
- Built-in lookahead carry capability
- Presettable for programmable operation

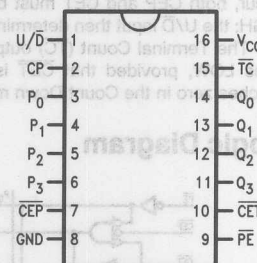
**Ordering Code:** See Section 5

### Logic Symbols

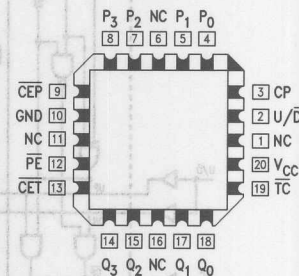


### Connection Diagrams

#### Pin Assignment for DIP, SOIC and Flatpak



#### Pin Assignment for LCC





**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

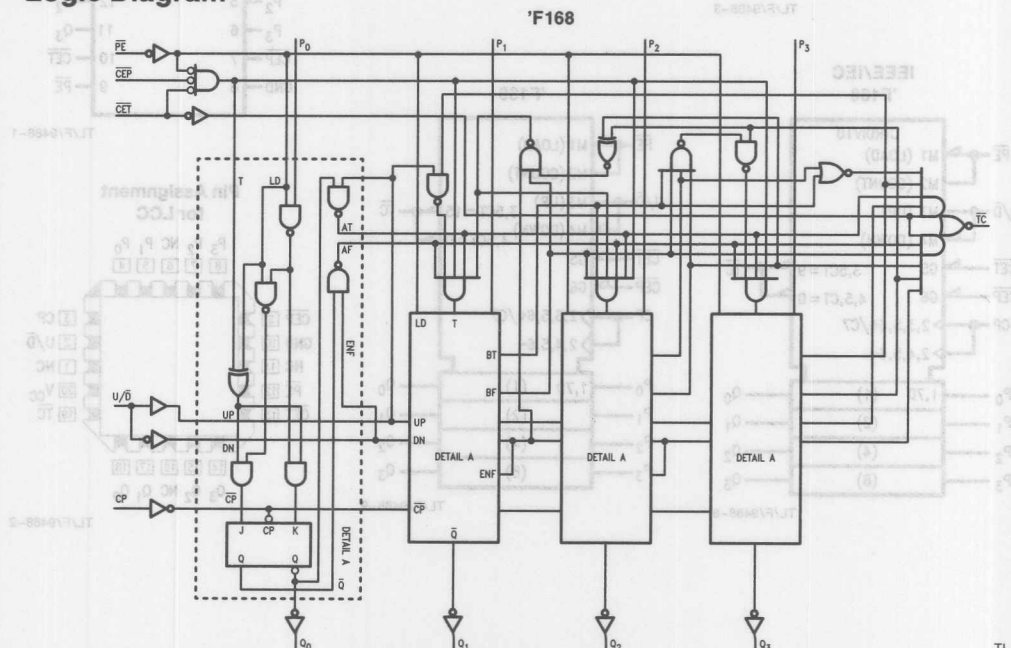
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	1.0/2.0	20 $\mu A$ / -1.2 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu A$ / -0.6 mA
$P_0-P_3$	Parallel Data Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$U/\overline{D}$	Up-Down Count Control Input	1.0/1.0	20 $\mu A$ / -0.6 mA
$Q_0-Q_3$	Flip-Flop Outputs	50/33.3	-1 mA/20 mA
TC	Terminal Count Output (Active LOW)	50/33.3	-1 mA/20 mA

**Functional Description**

The 'F168 and 'F169 use edge-triggered J-K type flip-flops and have no constraints on changing the control or data input signals in either state of the clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over other operations, as indicated in the Mode Select Table. When  $\overline{PE}$  is LOW, the data on the  $P_0-P_3$  inputs enters the flip-flops on the next rising edge of the clock. In order for counting to occur, both  $\overline{CEP}$  and  $\overline{CET}$  must be LOW and  $\overline{PE}$  must be HIGH; the  $U/\overline{D}$  input then determines the direction of counting. The Terminal Count ( $\overline{TC}$ ) output is normally HIGH and goes LOW, provided that  $\overline{CET}$  is LOW, when a counter reaches zero in the Count Down mode or reaches 9 (15 for

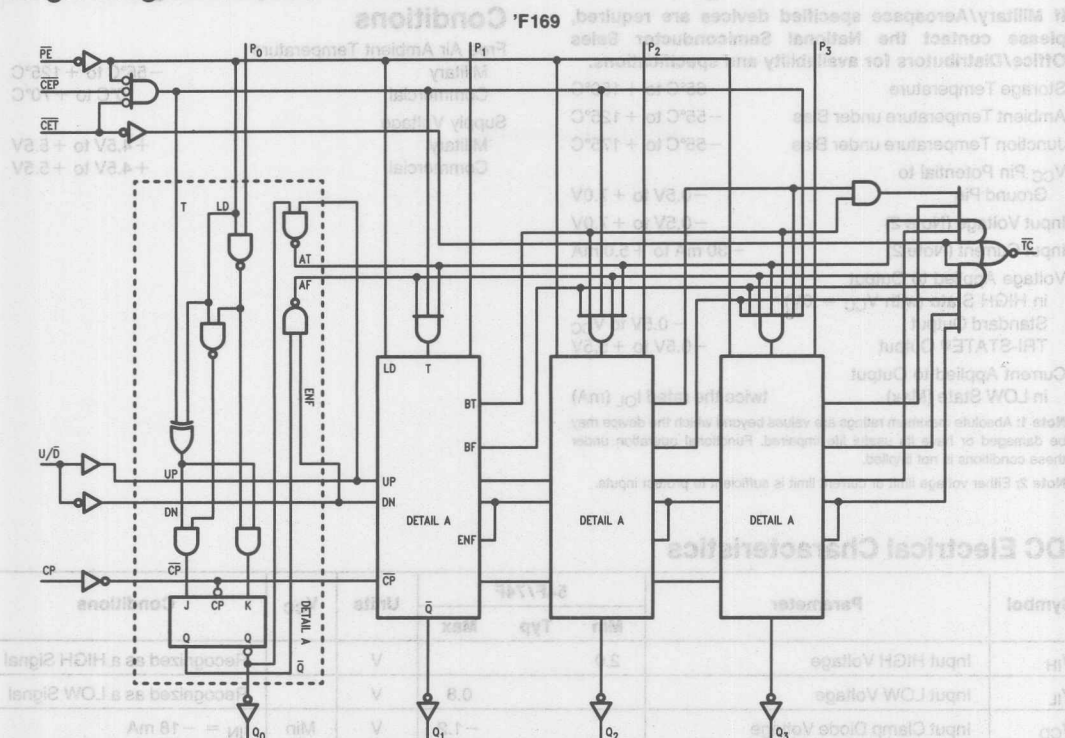
the 'F169) in the Count Up mode. The  $\overline{TC}$  output state is not a function of the Count Enable Parallel ( $\overline{CEP}$ ) input level. The  $\overline{TC}$  output of the 'F168 decade counter can also be LOW in the illegal states 11, 13, and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the 'F168 will return to the legitimate sequence within two counts. Since the  $\overline{TC}$  signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on  $\overline{TC}$ . For this reason the use of  $\overline{TC}$  as a clock signal is not recommended (see logic equations below).

- 1) Count Enable =  $\overline{CEP} \cdot \overline{CET} \cdot \overline{PE}$
- 2) Up: ('F168):  $\overline{TC} = Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3 \cdot (Up) \cdot \overline{CET}$   
( 'F169):  $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (Up) \cdot \overline{CET}$
- 3) Down:  $\overline{TC} = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (Down) \cdot \overline{CET}$

**Logic Diagram**

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Logic Diagram (Continued)



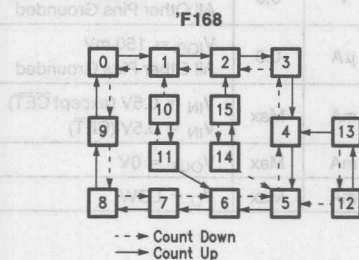
Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Mode Select Table

PE	CEP	CET	U/D	Action on Rising Clock Edge
L	X	X	X	Load ( $P_n \rightarrow Q_n$ )
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

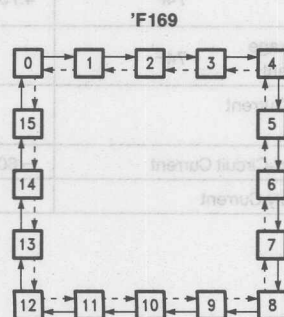
H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

## State Diagrams



--> Count Down  
-> Count Up

TL/F/9488-6



--> Count Down  
-> Count Up

TL/F/9488-7

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6 −1.2	mA	Max	V <sub>IN</sub> = 0.5V (except CET) V <sub>IN</sub> = 0.5V (CET)
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCL</sub>	Power Supply Current		35	52	mA	Max	V <sub>O</sub> = LOW

## 'F168

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Count Frequency	100	115		6.0		90		MHz	2-1
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $Q_n$ (PE HIGH or LOW)	3.0 4.0	6.5 9.0	8.5 11.5	3.0 4.0	12.0 16.0	3.0 4.0	9.5 13.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $\overline{TC}$	5.5 4.0	12.0 8.5	15.5 11.0	5.5 4.0	20.0 15.0	5.5 4.0	17.0 12.5	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay $\overline{CET}$ to $\overline{TC}$	2.5 2.5	4.5 6.0	6.0 8.0	2.5 2.5	9.0 12.0	2.5 2.5	7.0 9.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay $U/\overline{D}$ to $\overline{TC}$	3.5 4.0	8.5 12.5	11.0 16.0	3.5 4.0	16.0 14.0	3.5 4.0	12.5 18.0	ns	2-3

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $P_n$ to CP	4.0 4.0		4.5 4.5		4.5 4.5		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $P_n$ to CP	3.0 3.0		3.5 3.5		3.5 3.5			
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $\overline{\text{CEP}}$ or $\overline{\text{CET}}$ to CP	5.0 5.0		8.0 8.0		6.0 6.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $\overline{\text{CEP}}$ or $\overline{\text{CET}}$ to CP	0 0		0.0 1.0		0 0			
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $\overline{\text{PE}}$ to CP	8.0 8.0		10.0 10.0		9.0 9.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $\overline{\text{PE}}$ to CP	0 0		1.0 0		0 0			
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $U/\overline{D}$ to CP	11.0 16.5		14.0 12.0		12.5 18.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $U/\overline{D}$ to CP	0 0		0 0		0 0			
$t_w(\text{H})$ $t_w(\text{L})$	CP Pulse Width HIGH or LOW	5.0 5.0		6.0 9.0		5.5 5.5		ns	2-4

## 'F169

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Count Frequency	90			60		70		MHz	2-1
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $Q_n$ ( $\overline{\text{PE}}$ HIGH or LOW)	3.0 4.0	6.5 9.0	8.5 11.5	3.0 4.0	12.0 16.0	3.0 4.0	9.5 13.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $\overline{\text{TC}}$	5.5 4.0	12.0 8.5	15.5 12.5	5.5 4.0	20.0 15.0	5.5 4.0	17.5 13.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay $\overline{\text{CET}}$ to $\overline{\text{TC}}$	2.5 2.5	4.5 8.5	6.5 11.0	2.5 2.5	9.0 12.0	2.5 2.5	7.0 12.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay U/ $\overline{\text{D}}$ to $\overline{\text{TC}}$	3.5 4.0	8.5 8.0	11.5 12.0	3.5 4.0	16.0 14.0	3.5 4.0	12.5 13.0	ns	2-3

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	4.0		4.5		4.5		ns	2-6
$t_s(\text{L})$	$P_n$ to CP	4.0		4.5		4.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	3.0		3.5		3.5		ns	2-6
$t_h(\text{L})$	$P_n$ to CP	3.0		3.5		3.5			
$t_s(\text{H})$	Setup Time, HIGH or LOW	7.0		8.0		8.0		ns	2-6
$t_s(\text{L})$	$\overline{\text{CEP}}$ or $\overline{\text{CET}}$ to CP	5.0		8.0		6.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		0		0		ns	2-6
$t_h(\text{L})$	$\overline{\text{CEP}}$ or $\overline{\text{CET}}$ to CP	0.5		1.0		0.5			
$t_s(\text{H})$	Setup Time, HIGH or LOW	8.0		10.0		9.0		ns	2-6
$t_s(\text{L})$	$\overline{\text{PE}}$ to CP	8.0		10.0		9.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	1.0		1.0		1.0		ns	2-6
$t_h(\text{L})$	$\overline{\text{PE}}$ to CP	0		0		0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	11.0		14.0		12.5		ns	2-6
$t_s(\text{L})$	$\text{U}/\overline{\text{D}}$ to CP	7.0		12.0		8.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		0		0		ns	2-6
$t_h(\text{L})$	$\text{U}/\overline{\text{D}}$ to CP	0		0		0			
$t_w(\text{H})$	CP Pulse Width	4.0		6.0		4.5		ns	2-4
$t_w(\text{L})$	HIGH or LOW	7.0		9.0		8.0			



## 54F/74F174 Hex D Flip-Flop with Master Reset

### General Description

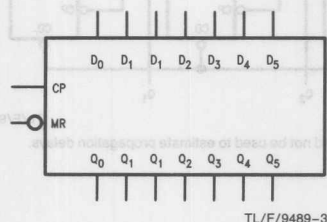
The 'F174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

### Features

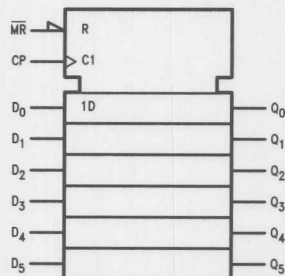
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Asynchronous common reset
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

### Logic Symbols

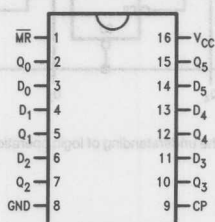


### IEEE/IEC

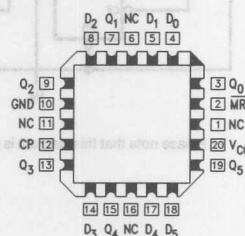


### Connection Diagrams

**Pin Assignment for  
DIP, SOIC and Flatpak**



**Pin Assignment  
for LCC**



**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
D <sub>0</sub> -D <sub>5</sub>	Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/ -0.6 mA
MR	Master Reset Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
Q <sub>0</sub> -Q <sub>5</sub>	Outputs	50/33.3	-1 mA/20 mA



# Functional Description

The 'F174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset (MR) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset (MR) will force all outputs LOW independent of Clock or Data inputs. The 'F174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

# Truth Table

Inputs			Outputs
MR	CP	D <sub>n</sub>	Q <sub>n</sub>
L	X	X	L
H	↗	H	H
H	↘	L	L

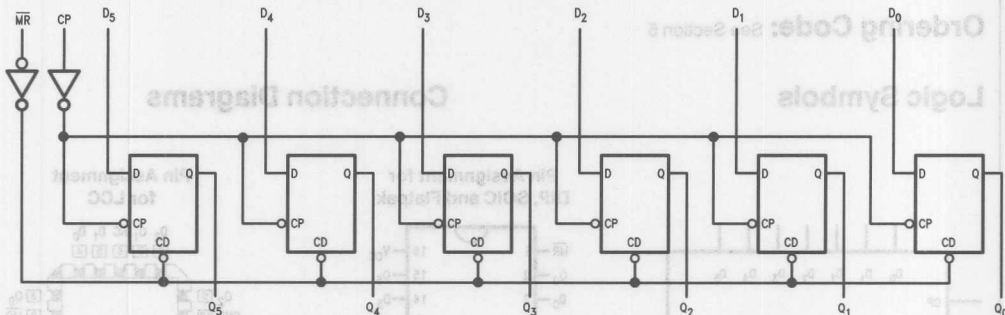
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH Clock Transition

# Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Pin Names	Description	U.L.	
		HIGH/LOW	Input/Output
D <sub>0</sub> -D <sub>5</sub>	Data inputs	1.0V/1.0	50 μA/-0.8 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0V/1.0	50 μA/-0.8 mA
MR	Master Reset Input (Active LOW)	1.0V/1.0	50 μA/-0.8 mA
Q <sub>0</sub> -Q <sub>5</sub>	Outputs	50/53.3	-1 mA/50 mA

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

ESD Last Passing Voltage (Min)	4000V
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**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	-55°C to +125°C
Military	0°C to +70°C
Commercial	
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage		0.8		V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage		-1.2		V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.5 2.7		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		30	45	mA	Max	CP =  D <sub>n</sub> = MR = HIGH
I <sub>CCL</sub>	Power Supply Current		30	45	mA	Max	V <sub>O</sub> = LOW

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	80			70		80		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	3.5	5.5	8.0	3.0	10.0	3.5	9.0		
$t_{\text{PHL}}$	CP to $Q_n$	4.0	7.0	10.0	4.0	12.0	4.0	11.0	ns	2-3
$t_{\text{PHL}}$	Propagation Delay									
	$\overline{\text{MR}}$ to $Q_n$	5.0	10.0	14.0	5.0	16.0	5.0	15.0	ns	2-3

## AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	4.0		5.0		4.0		ns	2-6
$t_s(\text{L})$	$D_n$ to CP	4.0		5.0		4.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		2.0		0		ns	2-4
$t_h(\text{L})$	$D_n$ to CP	0		2.0		0			
$t_w(\text{H})$	CP Pulse Width	4.0		5.0		4.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	6.0		7.5		6.0			
$t_w(\text{L})$	$\overline{\text{MR}}$ Pulse Width, LOW	5.0		6.5		5.0		ns	2-4
$t_{\text{rec}}$	Recovery Time, $\overline{\text{MR}}$ to CP	5.0		6.0		5.0			2-6

## 54F/74F175 Quad D Flip-Flop

### General Description

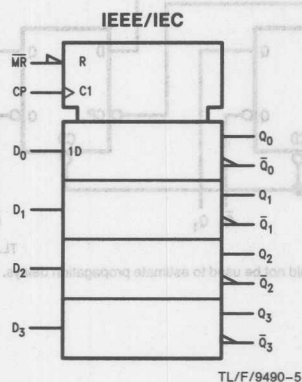
The 'F175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, LOW.

### Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Asynchronous common reset
- True and complement output

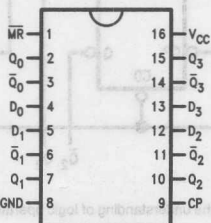
**Ordering Code:** See Section 5

### Logic Symbols

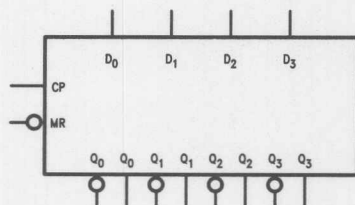
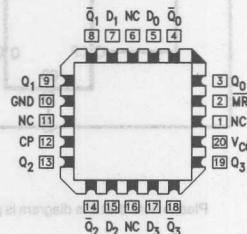


### Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak



Pin Assignment  
for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$D_0-D_3$	Data Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$Q_0-Q_3$	True Outputs	50/33.3	-1 mA / 20 mA
$\overline{Q_0}-\overline{Q_3}$	Complement Outputs	50/33.3	-1 mA / 20 mA

## Functional Description

The 'F175 consists of four edge-triggered D flip-flops with individual D inputs and Q and  $\bar{Q}$  outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and  $\bar{Q}$  outputs to follow. A LOW input on the Master Reset ( $\bar{MR}$ ) will force all Q outputs LOW and  $\bar{Q}$  outputs HIGH independent of Clock or Data inputs. The 'F175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

## Truth Table

Inputs			Outputs	
$\bar{MR}$	CP	D <sub>n</sub>	Q <sub>n</sub>	$\bar{Q}_n$
L	X	X	L	H
H	↗	H	L	L
H	↘	L	L	H

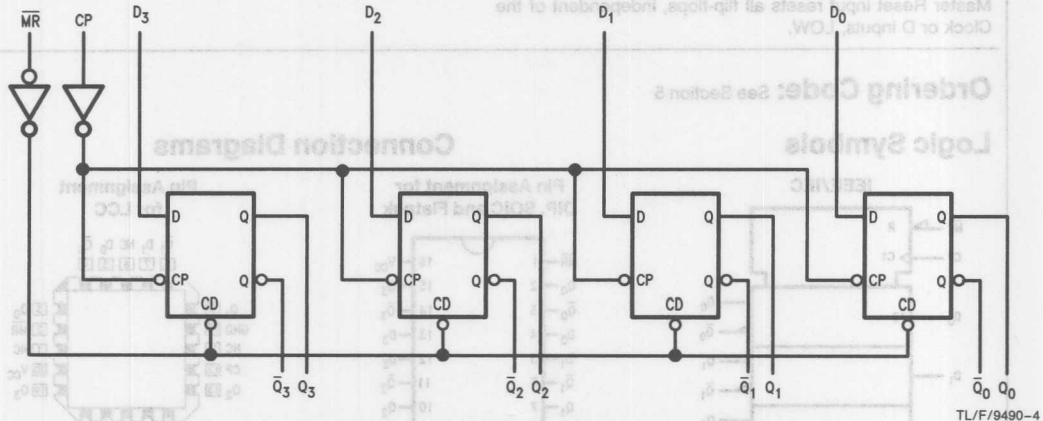
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH Clock Transition

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Pin Number	Description	U.L.	
		HIGH/LOW	Input/Output
D <sub>0</sub> -D <sub>3</sub>	Data Inputs	1.0/1.0	20 μA/-0.8 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/-0.8 mA
$\bar{MR}$	Master Reset Input (Active LOW)	1.0/1.0	20 μA/-0.8 mA
Q <sub>0</sub> -Q <sub>3</sub>	True Outputs	50/33.3	-1 mA/20 mA
$\bar{Q}_0$ - $\bar{Q}_3$	Complement Outputs	50/33.3	-1 mA/20 mA

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	−55°C to +125°C
Military	0°C to +70°C
Commercial	
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		22.5	34.0	mA	Max	CP =  D <sub>n</sub> = MR = HIGH



# **AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	100	140		80		100		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	4.0	5.0	6.5	3.5	8.5	4.0	7.5	ns	2-3
$t_{\text{PHL}}$	CP to $Q_n$ or $\bar{Q}_n$	4.0	6.5	8.5	4.0	10.5	4.0	9.5		
$t_{\text{PHL}}$	Propagation Delay $\overline{\text{MR}}$ to $Q_n$	4.5	9.0	11.5	4.5	15.0	4.5	13.0	ns	2-3
$t_{\text{PLH}}$	Propagation Delay $\overline{\text{MR}}$ to $\bar{Q}_n$	4.0	6.5	8.0	4.0	11.0	4.0	9.0	ns	2-3

## **AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	3.0		3.0		3.0		ns	2-6
$t_s(\text{L})$	$D_n$ to CP	3.0		4.0		3.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	1.0		1.0		1.0		ns	2-4
$t_h(\text{L})$	$D_n$ to CP	1.0		2.0		1.0			
$t_w(\text{H})$	CP Pulse Width	4.0		4.0		4.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	5.0		6.0		5.0			
$t_w(\text{L})$	$\overline{\text{MR}}$ Pulse Width, LOW	5.0		5.0		5.0		ns	2-4
$t_{\text{rec}}$	Recovery Time, $\overline{\text{MR}}$ to CP	5.0		6.0		5.0		ns	2-6

$V_{OL}$	Output LOW Voltage	Min	0.2	0.2	0.2	0.2	0.2		
$I_{IH}$	Input HIGH Current	Max	20.0	20.0	20.0	20.0	20.0		
$I_{IL}$	Input LOW Current	Max	100	100	100	100	100		
$I_{OZ}$	Output HIGH Leakage Current	Max	250	250	250	250	250		
$I_{OL}$	Output LOW Leakage Current	Max	50	50	50	50	50		
$I_{DD}$	Supply Current	Max	22.5	22.5	22.5	22.5	22.5		
$I_{OZ}$	Output HIGH Leakage Current	Max	250	250	250	250	250		
$I_{OL}$	Output LOW Leakage Current	Max	50	50	50	50	50		
$I_{DD}$	Supply Current	Max	22.5	22.5	22.5	22.5	22.5		

## 54F/74F181

### 4-Bit Arithmetic Logic Unit

#### General Description

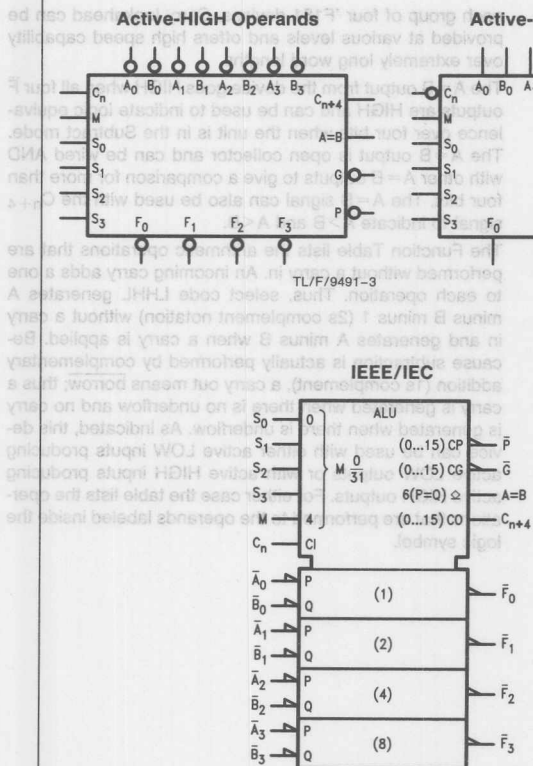
The 'F181 is a 4-bit Arithmetic logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations. It is 40% faster than the Schottky ALU and only consumes 30% as much power.

#### Features

- Full lookahead for high-speed arithmetic operation on long words
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

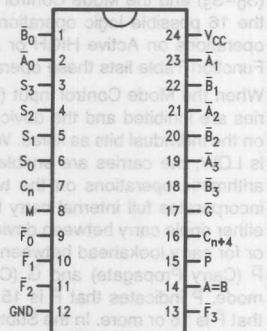
#### Logic Symbols



TL/F/9491-10

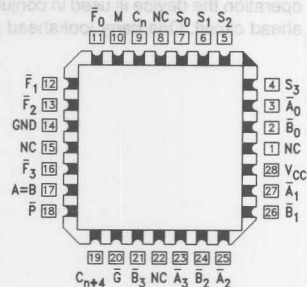
#### Connection Diagrams

##### Pin Assignment for DIP, SOIC and Flatpak



TL/F/9491-1

##### Pin Assignment for LCC



TL/F/9491-2

## Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\bar{A}_0-\bar{A}_3$	A Operand Inputs (Active LOW)	1.0/3.0	20 $\mu$ A/ -1.8 mA
$\bar{B}_0-\bar{B}_3$	B Operand Inputs (Active LOW)	1.0/3.0	20 $\mu$ A/ -1.8 mA
$S_0-S_3$	Function Select Inputs	1.0/4.0	20 $\mu$ A/ -2.4 mA
M	Mode Control Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
$C_n$	Carry Input	1.0/5.0	20 $\mu$ A/ -3.0 mA
$\bar{F}_0-\bar{F}_3$	Function Outputs (Active LOW)	50/33.3	-1 mA/20 mA
A = B	Comparator Output	OC*/33.3	* /20 mA
$\bar{G}$	Carry Generate Output (Active LOW)	50/33.3	-1 mA/20 mA
$\bar{P}$	Carry Propagate Output (Active LOW)	50/33.3	-1 mA/20 mA
$C_n + 4$	Carry Output	50/33.3	-1 mA/20 mA

\*OC-Open Collector

## Functional Description

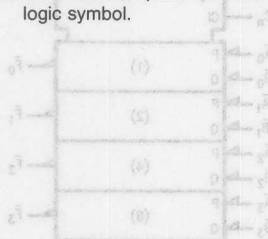
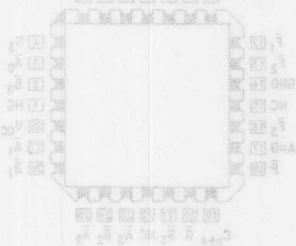
The 'F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs ( $S_0-S_3$ ) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on Active HIGH or Active LOW operands. The Function Table lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the  $C_n + 4$  output, or for carry lookahead between packages using the signals  $\bar{P}$  (Carry Propagate) and  $\bar{G}$  (Carry Generate). In the Add mode,  $\bar{P}$  indicates that  $\bar{F}$  is 15 or more, while  $\bar{G}$  indicates that  $\bar{F}$  is 16 or more. In the Subtract mode  $\bar{P}$  indicates that  $\bar{F}$  is zero or less, while  $\bar{G}$  indicates that  $\bar{F}$  is less than zero.  $\bar{P}$  and  $\bar{G}$  are not affected by carry in. When speed requirements are not stringent, the 'F181 can be used in a simple Ripple Carry mode by connecting the Carry output ( $C_n + 4$ ) signal to the Carry input ( $C_n$ ) of the next unit. For high speed operation the device is used in conjunction with a carry lookahead circuit. One carry lookahead package is required for

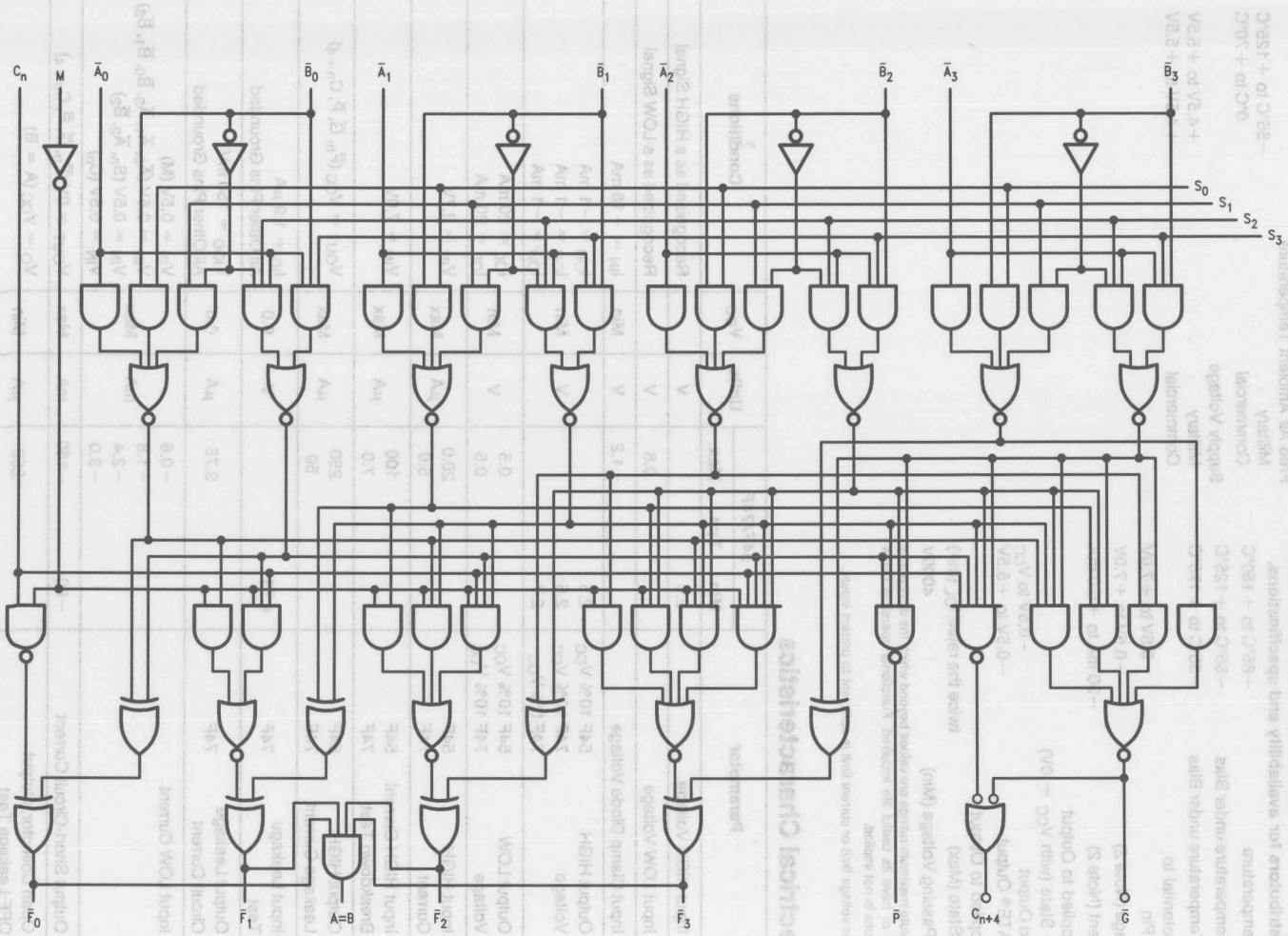
each group of four 'F181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four  $\bar{F}$  outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the Subtract mode. The A = B output is open collector and can be wired AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the  $C_n + 4$  signal to indicate  $A > B$  and  $A < B$ .

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.



## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub> ( $\bar{F}_n, \bar{G}, \bar{P}, C_n + 4$ )
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6 -1.8 -2.4 -3.0	mA	Max	V <sub>IN</sub> = 0.5V (M) V <sub>IN</sub> = 0.5V ( $\bar{A}_0, \bar{A}_1, \bar{A}_3, \bar{B}_0, \bar{B}_1, \bar{B}_3$ ) V <sub>IN</sub> = 0.5V (S <sub>n</sub> , $\bar{A}_2, \bar{B}_2$ ) V <sub>IN</sub> = 0.5V (C <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150			V <sub>OUT</sub> = 0V ( $\bar{F}_n, \bar{G}, \bar{P}, C_n + 4$ )
I <sub>OHC</sub>	Open Collector, Output OFF Leakage Test			250	μA	Min	V <sub>O</sub> = V <sub>CC</sub> (A = B)
I <sub>CCH</sub>	Power Supply Current		43	65.0	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		43	65.0			V <sub>O</sub> = LOW



Table 5-2 'F181 Operation Tables

	$S_0$	$S_1$	$S_2$	$S_3$	Logic ( $M=H$ )	Arithmetic ( $M=L, C_0=\text{Inactive}$ )	Arithmetic ( $M=L, C_0=\text{Active}$ )
<p>a. All Input Data Inverted</p>	L	L	L	L	$\bar{A}$	A minus 1	A
	H	L	L	L	$\bar{A} \cdot \bar{B}$	A • B minus 1	A • B
	L	H	L	L	$\bar{A} + \bar{B}$	A • B minus 1	A • B
	H	H	L	L	Logic "1"	minus 1 (2s comp.)	Zero
	L	L	H	L	$\bar{A} + \bar{B}$	A plus (A + B)	A plus (A + B) plus 1
	H	L	H	L	$\bar{B}$	A • B plus (A + B)	A • B plus (A + B) plus 1
	L	H	H	L	$\bar{A} \oplus \bar{B}$	A minus B minus 1	A minus B
	H	H	H	L	$\bar{A} + \bar{B}$	A + B	A + B plus 1
	L	L	L	H	$\bar{A} \cdot B$	A plus (A + B)	A plus (A + B) plus 1
	L	L	L	H	$A \oplus B$	A plus B	A plus B plus 1
<p>b. All Input Data True</p>	L	L	L	L	$\bar{A}$	A	A plus 1
	H	L	L	L	$\bar{A} + \bar{B}$	A + B	A + B plus 1
	L	H	L	L	$\bar{A} \cdot B$	A + B	A + B plus 1
	H	H	L	L	Logic "0"	minus 1 (2s comp.)	Zero
	L	L	H	L	$\bar{A} \cdot \bar{B}$	A plus (A • B)	A plus A • B plus 1
	L	L	H	L	$\bar{B}$	A • B plus (A + B)	A • B plus (A + B) plus 1
	L	H	H	L	$A \oplus B$	A minus B minus 1	A minus B
	H	H	H	L	$A \cdot \bar{B}$	A • B minus 1	A • B
	L	L	L	H	$\bar{A} + B$	A plus A • B	A plus A • B plus 1
	L	L	L	H	$\bar{A} \oplus B$	A plus B	A plus B plus 1
<p>c. A Input Data Inverted; B Input Data True</p>	L	L	L	L	$\bar{A}$	A minus 1	A
	H	L	L	L	$\bar{A} + B$	A • B minus 1	A • B
	L	H	L	L	$\bar{A} \cdot \bar{B}$	A • B minus 1	A • B
	H	H	L	L	Logic "1"	minus 1 (2s comp.)	Zero
	L	L	H	L	$\bar{A} \cdot B$	A plus (A + B)	A plus (A + B) plus 1
	L	L	H	L	$\bar{B}$	A • B plus (A + B)	A • B plus (A + B) plus 1
	L	H	H	L	$A \oplus B$	A plus B	A plus B plus 1
	H	H	H	L	$\bar{A} + B$	A + B	A + B plus 1
	L	L	L	H	$\bar{A} + \bar{B}$	A plus (A + B)	A plus (A + B) plus 1
	L	L	L	H	$\bar{A} \oplus \bar{B}$	A minus B minus 1	A minus B
<p>d. A Input Data True; B Input Data Inverted</p>	L	L	L	L	$\bar{A}$	A	A plus 1
	H	L	L	L	$\bar{A} \cdot \bar{B}$	A + B	A + B plus 1
	L	H	L	L	$\bar{A} + \bar{B}$	A + B	A + B plus 1
	H	H	L	L	Logic "0"	minus 1 (2s comp.)	Zero
	L	L	H	L	$\bar{A} + B$	A plus A • B	A plus A • B plus 1
	L	L	H	L	$\bar{B}$	A • B plus (A + B)	A • B plus (A + B) plus 1
	L	H	H	L	$\bar{A} \oplus \bar{B}$	A plus B	A plus B plus 1
	H	H	H	L	$\bar{A} \cdot B$	A • B minus 1	A • B
	L	L	L	H	$\bar{A} \cdot \bar{B}$	A plus A • B	A plus A • B plus 1
	L	L	L	H	$A \oplus B$	A minus B minus 1	A minus B



**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	Mode	74F			54F		74F		Units	Fig. No.
			$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{pF}$			
			Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay		3.0	6.4	8.5	3.0	10.0	3.0	9.5	ns	2-3
$t_{PHL}$	$C_n$ to $C_n + 4$		3.0	6.1	8.0	3.0	9.5	3.0	9.0		
$t_{PLH}$	Propagation Delay		5.0	10.0	13.0	5.0	15.5	5.0	14.0	ns	2-3
$t_{PHL}$	$\bar{A}$ or $\bar{B}$ to $C_n + 4$	Sum	4.0	9.4	12.0	3.5	16.5	4.0	13.0		
$t_{PLH}$	Propagation Delay		5.0	10.8	14.0	5.0	17.0	5.0	15.0	ns	2-3
$t_{PHL}$	$\bar{A}$ or $\bar{B}$ to $C_n + 4$	Dif	5.0	10.0	13.0	4.0	15.0	5.0	14.0		
$t_{PLH}$	Propagation Delay		3.0	6.7	8.5	2.5	16.0	3.0	9.5	ns	2-3
$t_{PHL}$	$C_n$ to $\bar{F}$	Any	3.0	6.5	8.5	2.5	12.0	3.0	9.5		
$t_{PLH}$	Propagation Delay		3.0	5.7	7.5	2.5	9.0	3.0	8.5	ns	2-3
$t_{PHL}$	$\bar{A}$ or $\bar{B}$ or $\bar{G}$	Sum	3.0	5.8	7.5	2.5	9.5	3.0	8.5		
$t_{PLH}$	Propagation Delay		3.0	6.5	8.5	2.5	11.5	3.0	9.5	ns	2-3
$t_{PHL}$	$\bar{A}$ or $\bar{B}$ to $\bar{G}$	Dif	3.0	7.3	9.5	2.5	11.0	3.0	10.5		
$t_{PLH}$	Propagation Delay		3.0	5.0	7.0	2.5	8.5	3.0	8.0	ns	2-3
$t_{PHL}$	$\bar{A}$ or $\bar{B}$ to $\bar{P}$	Sum	3.0	5.5	7.5	3.0	9.5	3.0	8.5		
$t_{PLH}$	Propagation Delay		3.0	5.8	7.5	2.5	11.0	3.0	8.5	ns	2-3
$t_{PHL}$	$\bar{A}$ or $\bar{B}$ to $\bar{P}$	Dif	4.0	6.5	8.5	3.0	11.0	4.0	9.5		
$t_{PLH}$	Propagation Delay		3.0	7.0	9.0	3.0	14.5	3.0	10.0	ns	2-3
$t_{PHL}$	$\bar{A}_i$ or $\bar{B}_i$ to $\bar{F}_i$	Sum	3.0	7.2	10.0	3.0	14.5	3.0	10.0		
$t_{PLH}$	Propagation Delay		3.0	8.2	11.0	3.0	17.5	3.0	12.0	ns	2-3
$t_{PHL}$	$\bar{A}_i$ or $\bar{B}_i$ to $\bar{F}_i$	Dif	3.0	5.0	11.0	3.0	14.5	3.0	12.0		
$t_{PLH}$	Propagation Delay		4.0	8.0	10.5	3.5	16.5	4.0	11.5	ns	2-3
$t_{PHL}$	Any $\bar{A}$ or $\bar{B}$ to Any $\bar{F}$	Sum	4.0	7.8	10.0	4.0	13.5	4.0	11.0		
$t_{PLH}$	Propagation Delay		4.5	9.4	12.0	3.5	17.5	4.5	13.0	ns	2-3
$t_{PHL}$	Any $\bar{A}$ or $\bar{B}$ to Any $\bar{F}$	Dif	3.5	9.4	12.0	3.0	14.0	3.5	13.0		
$t_{PLH}$	Propagation Delay		4.0	6.0	9.0	3.5	14.5	4.0	10.0	ns	2-3
$t_{PHL}$	$\bar{A}$ or $\bar{B}$ to $\bar{F}$	Logic	4.0	6.0	10.0	3.0	15.5	4.0	11.0		
$t_{PLH}$	Propagation Delay		11.0	18.5	27.0	8.0	35.0	11.0	29.0	ns	2-3
$t_{PHL}$	$\bar{A}$ or $\bar{B}$ to $A = B$	Dif	6.0	9.8	12.5	5.5	21.0	6.0	13.5		

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# 54F/74F182

## Carry Lookahead Generator

### General Description

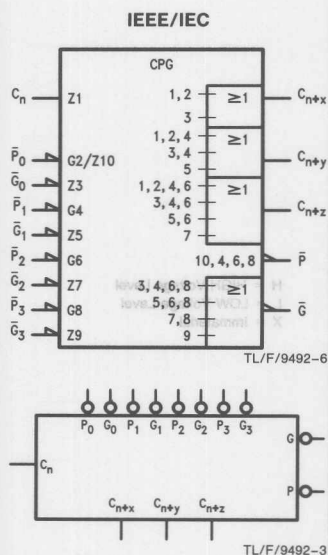
The 'F182 is a high-speed carry lookahead generator. It is generally used with the 'F181 or 'F381 4-bit arithmetic logic units to provide high-speed lookahead over word lengths of more than four bits.

### Features

- Provides lookahead carries across a group of four ALUs
- Multi-level lookahead high-speed arithmetic operation over long word lengths
- Guaranteed 4000V minimum ESD protection

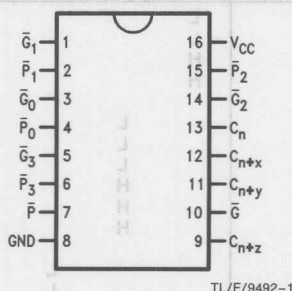
**Ordering Code:** See Section 5

### Logic Symbols

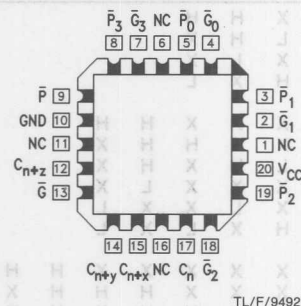


### Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



Pin Assignment for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$C_n$	Carry Input	1.0/2.0	20 $\mu$ A / -1.2 mA
$\bar{G}_0, \bar{G}_2$	Carry Generate Inputs (Active LOW)	1.0/14.0	20 $\mu$ A / -8.4 mA
$\bar{G}_1$	Carry Generate Input (Active LOW)	1.0/16.0	20 $\mu$ A / -9.6 mA
$\bar{G}_3$	Carry Generate Input (Active LOW)	1.0/8.0	20 $\mu$ A / -4.8 mA
$\bar{P}_0, \bar{P}_1$	Carry Propagate Inputs (Active LOW)	1.0/8.0	20 $\mu$ A / -4.8 mA
$\bar{P}_2$	Carry Propagate Input (Active LOW)	1.0/6.0	20 $\mu$ A / -3.6 mA
$\bar{P}_3$	Carry Propagate Input (Active LOW)	1.0/4.0	20 $\mu$ A / -2.4 mA
$C_{n+x} - C_{n+z}$	Carry Outputs	50/33.3	-1 mA / 20 mA
$\bar{G}$	Carry Generate Output (Active LOW)	50/33.3	-1 mA / 20 mA
$\bar{P}$	Carry Propagate Output (Active LOW)	50/33.3	-1 mA / 20 mA

## Functional Description

The 'F182 carry lookahead generator accepts up to four pairs of Active LOW Carry Propagate ( $\bar{P}_0$ – $\bar{P}_3$ ) and Carry Generate ( $\bar{G}_0$ – $\bar{G}_3$ ) signals and an Active HIGH Carry input ( $C_n$ ) and provides anticipated Active HIGH carries ( $C_{n+1}$ ,  $C_{n+2}$ ,  $C_{n+3}$ ) across four groups of binary adders. The 'F182 also has Active LOW Carry Propagate ( $\bar{P}$ ) and Carry Generate ( $\bar{G}$ ) outputs which may be used for further levels of lookahead. The logic equations provided at the outputs are:

$$C_{n+1} = G_0 + P_0 C_n$$

$$C_{n+2} = G_1 + P_1 G_0 + P_1 P_0 C_n$$

$$C_{n+3} = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n$$

$$\bar{G} = \bar{G}_3 + \bar{P}_3 \bar{G}_2 + \bar{P}_3 \bar{P}_2 \bar{G}_1 + \bar{P}_3 \bar{P}_2 \bar{P}_1 \bar{G}_0$$

$$\bar{P} = \bar{P}_2 \bar{P}_1 \bar{P}_0$$

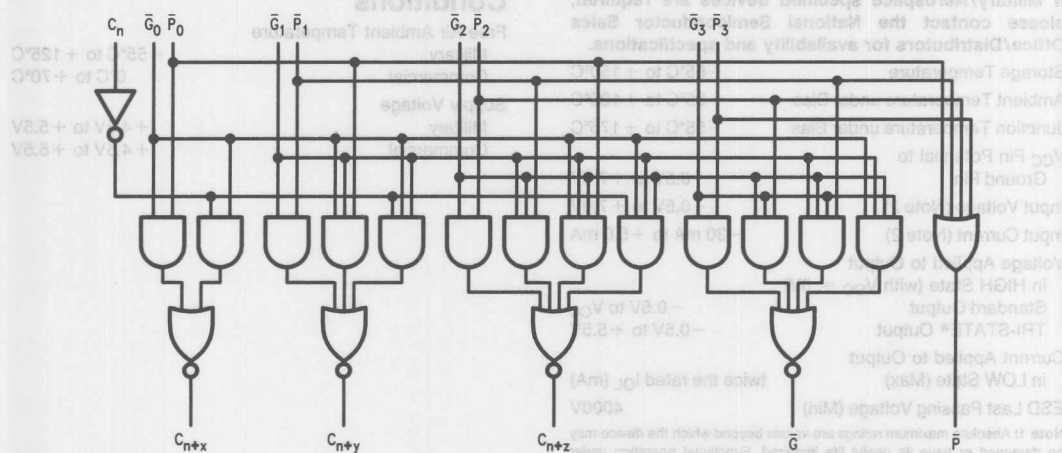
Also, the 'F182 can be used with binary ALUs in an active LOW or active HIGH input operand mode. The connections (Figure 1) to and from the ALU to the carry lookahead generator are identical in both cases. Carries are rippled between lookahead blocks. The critical speed path follows the circled numbers. There are several possible arrangements for the carry interconnects, but all achieve about the same speed. A 28-bit ALU is formed by dropping the last 'F181 or 'F381.

## Truth Table

Inputs									Outputs				
$C_n$	$\bar{G}_0$	$\bar{P}_0$	$\bar{G}_1$	$\bar{P}_1$	$\bar{G}_2$	$\bar{P}_2$	$\bar{G}_3$	$\bar{P}_3$	$C_{n+1}$	$C_{n+2}$	$C_{n+3}$	$\bar{G}$	$\bar{P}$
X	H	H							L				
L	H	X							L				
X	L	X							L				
H	X	L							H				
X	X	X	H	H					L				
X	H	H	H	X					L				
L	H	X	H	X					L				
X	X	X	L	X					L				
X	L	X	X	L					L				
H	X	L	X	L					H				
X	X	X	X	X	H	H			L				
X	X	X	H	H	H	X			L				
X	H	H	H	X	H	X			L				
L	H	X	H	X	H	X			L				
X	X	X	X	X	L	X			H				
X	X	X	L	X	X	L			H				
X	L	X	X	L	X	L			H				
H	X	L	X	L	X	L			H				
X			X	X	X	X	H	H	H				
X			X	X	H	H	H	X	H				
X			H	H	H	X	H	X	H				
X			X	X	X	X	L	X	L				
X			X	X	L	X	X	L	L				
X			X	X	X	L	X	L	L				
X			L	X	X	L	X	L	L				
L			X	L	X	L	X	L	L				
	H			X		X		X	H				
	X			H		X		X	H				
	X			X		X		H	H				
	X			X		X		L	H				
	L			L		L		L	L				

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

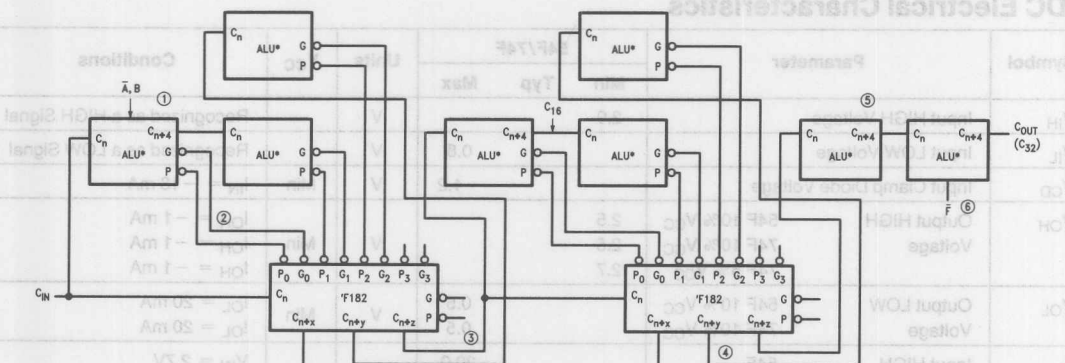


FIGURE 1. 32-Bit ALU with Ripped Carry between 16-Bit Lookahead ALUs

\*ALUs may be either 'F181 or 'F381

Symbol	Parameter	Typ	Max	Conditions
$I_{OH}$	Input HIGH Current	24	100	$V_{OH} = 2.7V$
$I_{OL}$	Input LOW Current	24	100	$V_{OL} = 0.4V$
$I_{OH}$	Output HIGH Current	24	280	$V_{OH} = 2.7V$
$I_{OL}$	Output LOW Current	24	280	$V_{OL} = 0.4V$
$I_{LH}$	Leakage Current	24	20	$V_{OH} = 2.7V$
$I_{LL}$	Leakage Current	24	20	$V_{OL} = 0.4V$
$I_{OH}$	Input HIGH Current	24	100	$V_{OH} = 2.7V$
$I_{OL}$	Input LOW Current	24	100	$V_{OL} = 0.4V$
$I_{OH}$	Output HIGH Current	24	280	$V_{OH} = 2.7V$
$I_{OL}$	Output LOW Current	24	280	$V_{OL} = 0.4V$
$I_{LH}$	Leakage Current	24	20	$V_{OH} = 2.7V$
$I_{LL}$	Leakage Current	24	20	$V_{OL} = 0.4V$
$I_{OH}$	Input HIGH Current	24	100	$V_{OH} = 2.7V$
$I_{OL}$	Input LOW Current	24	100	$V_{OL} = 0.4V$
$I_{OH}$	Output HIGH Current	24	280	$V_{OH} = 2.7V$
$I_{OL}$	Output LOW Current	24	280	$V_{OL} = 0.4V$
$I_{LH}$	Leakage Current	24	20	$V_{OH} = 2.7V$
$I_{LL}$	Leakage Current	24	20	$V_{OL} = 0.4V$
$I_{OH}$	Input HIGH Current	24	100	$V_{OH} = 2.7V$
$I_{OL}$	Input LOW Current	24	100	$V_{OL} = 0.4V$
$I_{OH}$	Output HIGH Current	24	280	$V_{OH} = 2.7V$
$I_{OL}$	Output LOW Current	24	280	$V_{OL} = 0.4V$
$I_{LH}$	Leakage Current	24	20	$V_{OH} = 2.7V$
$I_{LL}$	Leakage Current	24	20	$V_{OL} = 0.4V$

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

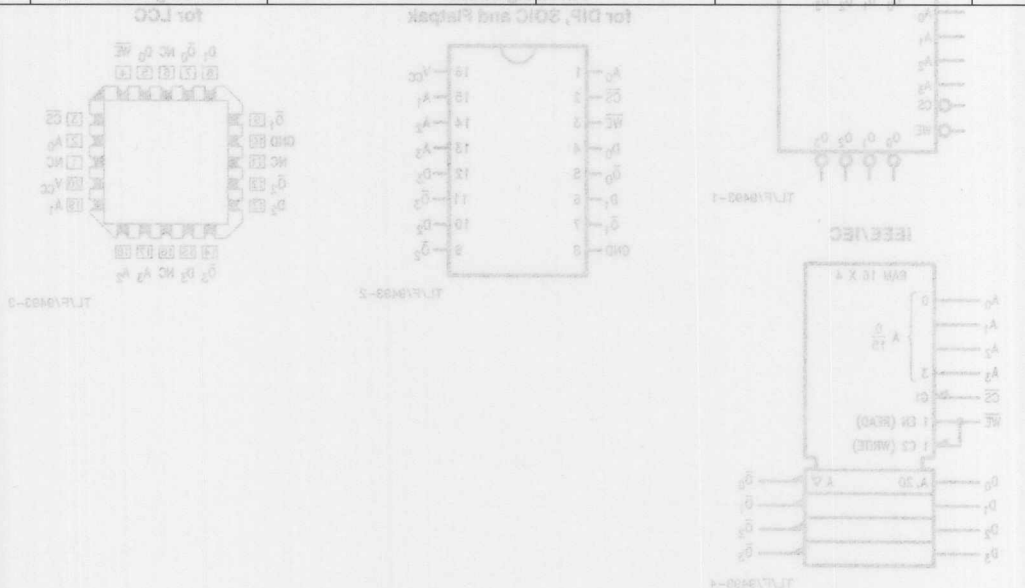
## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-1.2 -2.4 -3.6 -4.8 -8.4 -9.6	mA	Max	V <sub>IN</sub> = 0.5V (C <sub>N</sub> ) V <sub>IN</sub> = 0.5V (P <sub>3</sub> ) V <sub>IN</sub> = 0.5V (P <sub>2</sub> ) V <sub>IN</sub> = 0.5V (G <sub>3</sub> , P <sub>0</sub> , P <sub>1</sub> ) V <sub>IN</sub> = 0.5V (G <sub>0</sub> , G <sub>2</sub> ) V <sub>IN</sub> = 0.5V (G <sub>1</sub> )
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150			V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		18.4	28.0	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		23.5	36.0	mA	Max	V <sub>O</sub> = LOW

Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $C_n$ to $C_{n+x}$ , $C_{n+y}$ , $C_{n+z}$	3.0 3.0	6.6 6.8	8.5 9.0	3.0 3.0	12.0 11.0	3.0 3.0	9.5 10.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{P}_0$ , $\bar{P}_1$ , or $\bar{P}_2$ to $C_{n+x}$ , $C_{n+y}$ , or $C_{n+z}$	2.5 1.5	6.2 3.7	8.0 5.0	2.5 1.0	11.0 7.0	2.5 1.5	9.0 6.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{G}_0$ , $\bar{G}_1$ , or $\bar{G}_2$ to $C_{n+x}$ , $C_{n+y}$ , or $C_{n+z}$	2.5 1.5	6.5 3.9	8.5 5.2	2.5 1.0	11.0 7.0	2.5 1.5	9.5 6.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{P}_1$ , $\bar{P}_2$ , or $\bar{P}_3$ to $\bar{G}$	3.0 3.0	7.9 6.0	10.0 8.0	3.0 2.5	12.0 10.0	3.0 3.0	11.0 9.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{G}_n$ to $\bar{G}$	3.0 3.0	8.3 5.7	10.5 7.5	3.0 2.5	12.0 10.0	3.0 3.0	11.5 8.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{P}_n$ to $\bar{P}$	3.0 2.5	5.7 4.1	7.5 5.5	2.5 2.5	10.0 8.0	3.0 2.5	8.5 6.5	ns	2-3



Pin Names	Description	Slew Rate	
		U.L. HIGH/LOW	Input/Output Input/Output
$A_0-A_3$	Address Inputs	1.0/1.0	20 $\mu\text{A}$ - 0.8 mA
$\bar{CS}$	Chip Select Input (Active LOW)	1.0/1.0	20 $\mu\text{A}$ - 1.5 mA
$\bar{WE}$	Write Enable Input (Active LOW)	1.0/1.0	20 $\mu\text{A}$ - 0.8 mA
$D_0-D_3$	Data Inputs	1.0/1.0	20 $\mu\text{A}$ - 0.8 mA
$\bar{D}_0-\bar{D}_3$	Inverted Data Outputs	1.0/1.0 (3.3)	-3.0 mA/54 mA (20 mA)





## 54F/74F189 64-Bit Random Access Memory with TRI-STATE® Outputs

### General Description

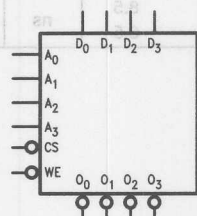
The 'F189 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are TRI-STATE and are in the high impedance state whenever the Chip Select ( $\overline{CS}$ ) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

### Features

- TRI-STATE outputs for data bus applications
- Buffered inputs minimize loading
- Address decoding on-chip
- Diode clamped inputs minimize ringing
- Available in SOIC, (300 mil only)

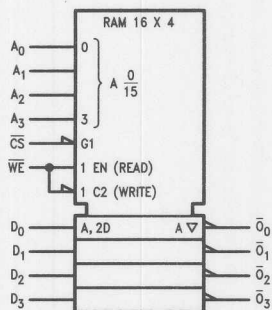
**Ordering Code:** See Section 5

### Logic Symbols



TL/F/9493-1

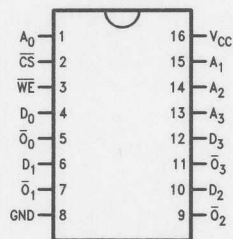
#### IEEE/IEC



TL/F/9493-4

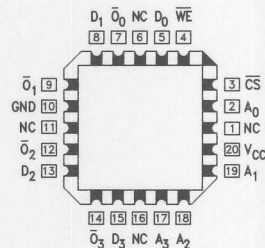
### Connection Diagrams

#### Pin Assignment for DIP, SOIC and Flatpak



TL/F/9493-2

#### Pin Assignment for LCC



TL/F/9493-3

**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_0-A_3$	Address Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/1.0	20 $\mu A$ / -1.2 mA
$\overline{WE}$	Write Enable Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$D_0-D_3$	Data Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{O}_0-\overline{O}_3$	Inverted Data Outputs	150/40 (33.3)	-3.0 mA/24 mA (20 mA)

Function Table

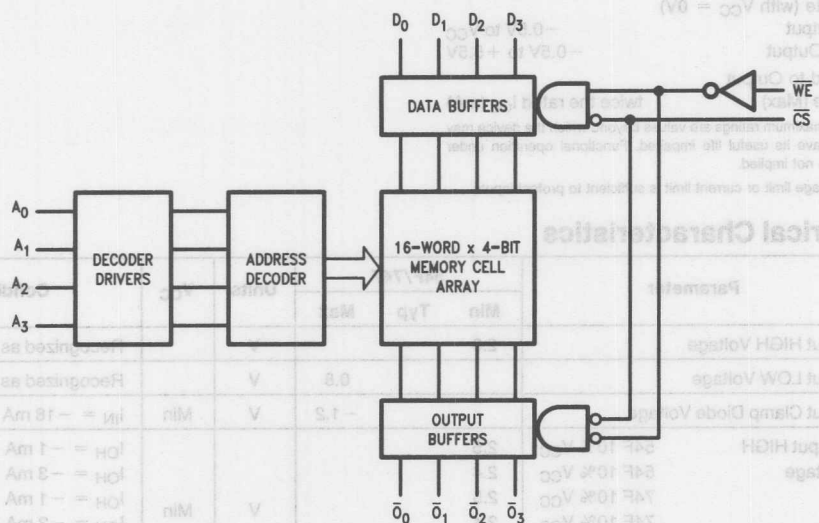
Inputs		Operation	Condition of Outputs
CS	WE		
L	L	Write	High Impedance
L	H	Read	Complement of Stored Data
H	X	Inhibit	High Impedance

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

## Block Diagram



TL/F/9493-5

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6 −1.2	mA	Max	V <sub>IN</sub> = 0.5V (except $\overline{CS}$ ) V <sub>IN</sub> = 0.5V ( $\overline{CS}$ )
I <sub>OZH</sub>	Output Leakage Current			50			V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500			V <sub>OUT</sub> = 5.25V
I <sub>CCZ</sub>	Power Supply Current		37	55	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$*T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{\text{PLH}}$	Access Time, HIGH or LOW	10.0	18.5	26.0	9.0	32.0	10.0	27.0	ns	2-3
$t_{\text{PHL}}$	$A_n$ to $\overline{O}_n$	8.0	13.5	19.0	8.0	23.0	8.0	20.0		
$t_{\text{pZH}}$	Access Time, HIGH or LOW	3.5	6.0	8.5	3.5	10.5	3.5	9.5	ns	2-5
$t_{\text{pZL}}$	$\overline{\text{CS}}$ to $\overline{O}_n$	5.0	9.0	13.0	5.0	15.0	5.0	14.0		
$t_{\text{pHZ}}$	Disable Time, HIGH or LOW	2.0	4.0	6.0	2.0	8.0	2.0	7.0	ns	2-5
$t_{\text{pLZ}}$	$\overline{\text{CS}}$ to $\overline{O}_n$	3.0	5.5	8.0	2.5	10.0	3.0	9.0		
$t_{\text{pZH}}$	Write Recovery Time,	6.5	15.0	28.0	6.5	37.5	6.5	29.0	ns	2-5
$t_{\text{pZL}}$	HIGH or LOW $\overline{\text{WE}}$ to $\overline{O}_n$	6.5	11.0	15.5	6.5	17.5	6.5	16.5		
$t_{\text{pHZ}}$	Disable Time, HIGH or LOW	4.0	7.0	10.0	3.5	12.0	4.0	11.0	ns	2-5
$t_{\text{pLZ}}$	$\overline{\text{WE}}$ to $\overline{O}_n$	5.0	9.0	13.0	5.0	15.0	5.0	14.0		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$*T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	0		0		0		ns	2-6
$t_s(\text{L})$	$A_n$ to $\overline{\text{WE}}$	0		0		0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0		2.0		2.0			
$t_h(\text{L})$	$A_n$ to $\overline{\text{WE}}$	2.0		2.0		2.0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	10.0		11.0		10.0		ns	2-6
$t_s(\text{L})$	$D_n$ to $\overline{\text{WE}}$	10.0		11.0		10.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		2.0		0			
$t_h(\text{L})$	$D_n$ to $\overline{\text{WE}}$	0		2.0		0			
$t_s(\text{L})$	Setup Time, LOW $\overline{\text{CS}}$ to $\overline{\text{WE}}$	0		0		0		ns	2-6
$t_h(\text{L})$	Hold Time, LOW $\overline{\text{CS}}$ to $\overline{\text{WE}}$	6.0		7.5		6.0			
$t_w(\text{L})$	$\overline{\text{WE}}$ Pulse Width, LOW	6.0		5.5		6.0			

\* $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ 

Pin Names	Description	U.L.	Input/Output
TC	Terminal Count Output (Active HIGH)	50/33.3	Output
RC	Ripple Clock Output (Active LOW)	50/33.3	Output
Q <sub>0</sub> -Q <sub>3</sub>	Flip-Flop Outputs	50/33.3	Output
U/D	Up/Down Count Control Input	1.0/1.0	Input
PC	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	Input
P <sub>0</sub> -P <sub>3</sub>	Parallel Data Inputs	1.0/1.0	Input
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	Input
CE	Count Enable Input (Active LOW)	1.0/3.0	Input



## 54F/74F190

### Up/Down Decade Counter with Preset and Ripple Clock

#### General Description

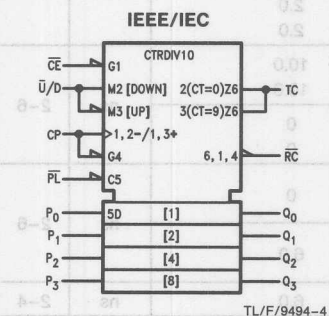
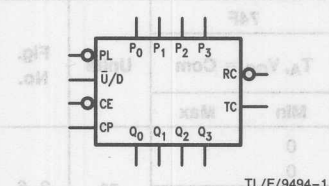
The 'F190 is a reversible BCD (8421) decade counter featuring synchronous counting and asynchronous presetting. The preset feature allows the 'F190 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

#### Features

- High-speed—125 MHz typical count frequency
- Synchronous counting
- Asynchronous parallel load
- Cascadable

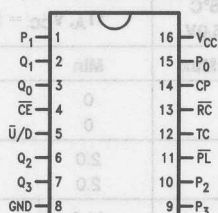
**Ordering Code:** See Section 5

#### Logic Symbols

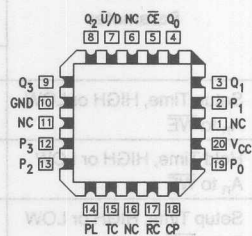


#### Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak



Pin Assignment  
for LCC





**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{CE}$	Count Enable Input (Active LOW)	1.0/3.0	20 $\mu$ A/ -1.8 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$P_0$ - $P_3$	Parallel Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{U/D}$	Up/Down Count Control Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
$Q_0$ - $Q_3$	Flip-Flop Outputs	50/33.3	-1 mA/20 mA
RC	Ripple Clock Output (Active LOW)	50/33.3	-1 mA/20 mA
TC	Terminal Count Output (Active HIGH)	50/33.3	-1 mA/20 mA

## Functional Description

The 'F190 is a synchronous up/down BCD decade counter containing four edge-triggered flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations. It has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ( $\overline{PL}$ ) input is LOW, information present on the Parallel Data inputs ( $P_0$ – $P_3$ ) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table. A HIGH signal on the  $\overline{CE}$  input inhibits counting. When  $\overline{CE}$  is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the  $\overline{U/D}$  input signal, as indicated in the Mode Select Table.  $\overline{CE}$  and  $\overline{U/D}$  can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

**$\overline{RC}$  Truth Table**

Inputs			Output
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H		
H	X	X	H
X	L	X	H


\*TC is generated internally

H = HIGH Voltage Level

L = LOW Voltage Level



X = Immaterial

 = LOW-to-HIGH Clock Transition

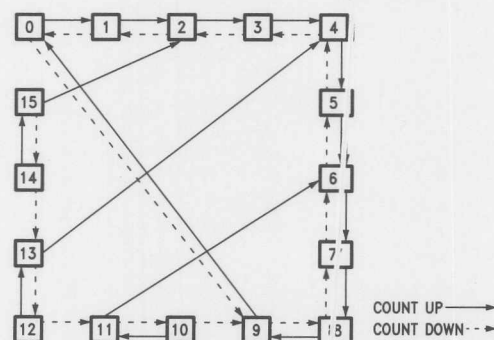
 = LOW Pulse

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches 9 in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until  $\overline{U/D}$  is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is also used internally to enable the Ripple Clock ( $\overline{RC}$ ) output. The  $\overline{RC}$  output is normally HIGH. When  $\overline{CE}$  is LOW and TC is HIGH, the  $\overline{RC}$  output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters. For a discussion and illustrations of the various methods of implementing multistage counters, please see the 'F191 data sheet.

**Mode Select Table**

Inputs				Mode
$\overline{PL}$	$\overline{CE}$	$\overline{U/D}$	CP	
H	L	L		Count Up
H	L	H		Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

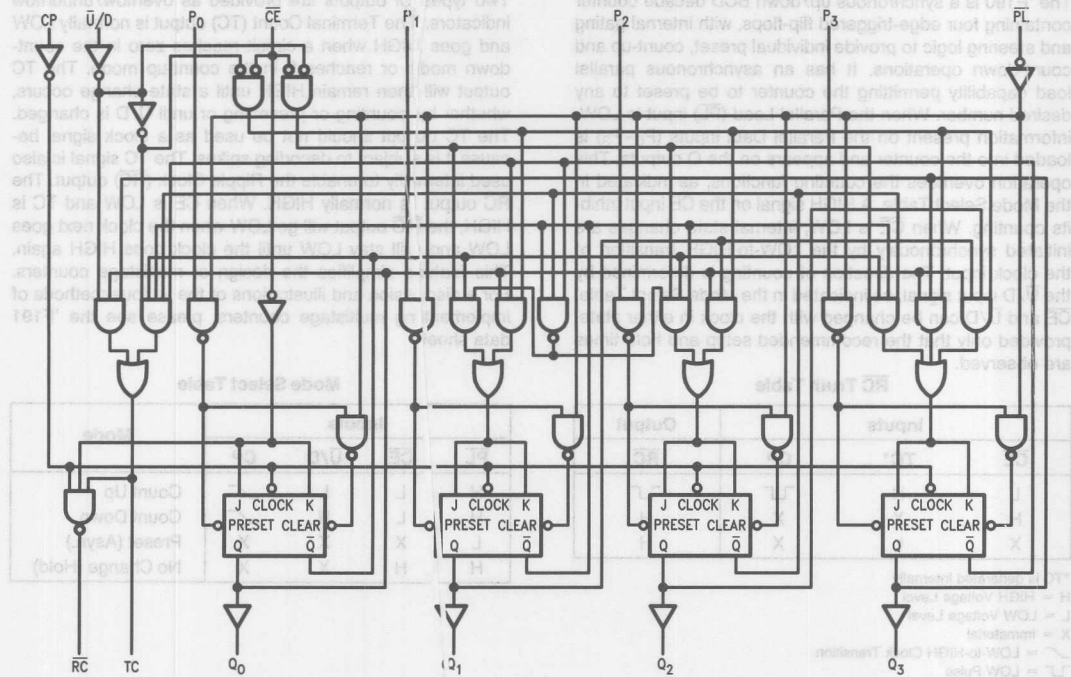
## State Diagram



TL/F/9494-5

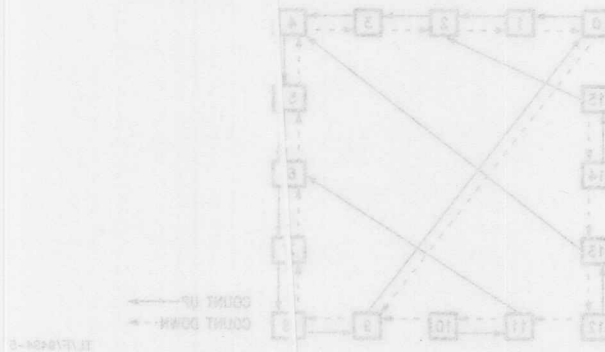


## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

TL/F/9494-6



**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	–0.5V to V <sub>CC</sub>
TRI-STATE® Output	–0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	–55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			–1.2	V	Min	I <sub>IN</sub> = –18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = –1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = –1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = –1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			–0.6 –1.8	mA	Max	V <sub>IN</sub> = 0.5V, except $\overline{CE}$ V <sub>IN</sub> = 0.5V, $\overline{CE}$
I <sub>OS</sub>	Output Short-Circuit Current		–60	–150			V <sub>OUT</sub> = 0V
I <sub>CCL</sub>	Power Supply Current		38	55	mA	Max	V <sub>O</sub> = LOW

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	100	125		75		90		MHz	2-1
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $Q_n$	3.0 5.0	5.5 8.5	7.5 11.0	3.0 5.0	9.5 13.5	3.0 5.0	8.5 12.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to TC	6.0 5.0	10.0 8.5	13.0 11.0	6.0 5.0	16.5 13.5	6.0 5.0	14.0 12.0		
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $\overline{\text{RC}}$	3.0 3.0	5.5 5.0	7.5 7.0	3.0 3.0	9.5 9.0	3.0 3.0	8.5 8.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay $\overline{\text{CE}}$ to $\overline{\text{RC}}$	3.0 3.0	5.0 5.5	7.0 7.0	3.0 3.0	9.0 9.0	3.0 3.0	8.0 8.0		
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay $\overline{\text{U/D}}$ to $\overline{\text{RC}}$	7.0 5.5	11.0 9.0	18.0 12.0	7.0 5.5	22.0 14.0	7.0 5.5	20.0 13.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay $\overline{\text{U/D}}$ to $\overline{\text{TC}}$	4.0 4.0	7.0 6.5	10.0 10.0	4.0 4.0	13.5 12.5	4.0 4.0	11.0 11.0		
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay $P_n$ to $Q_n$	3.0 6.0	4.5 10.0	7.0 13.0	3.0 6.0	9.0 16.0	3.0 6.0	8.0 14.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay $\overline{\text{PL}}$ to $Q_n$	5.0 5.5	8.5 9.0	11.0 12.0	5.0 5.5	13.0 14.5	5.0 5.5	12.0 13.0	ns	2-3

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $P_n$ to $\overline{\text{PL}}$	4.5 4.5		6.0 6.0		5.0 5.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $P_n$ to $\overline{\text{PL}}$	2.0 2.0		2.0 2.0		2.0 2.0			
$t_s(\text{L})$	Setup Time, LOW $\overline{\text{CE}}$ to CP	10.0		10.5		10.0		ns	2-6
$t_h(\text{L})$	Hold Time, LOW $\overline{\text{CE}}$ to CP	0		0		0			
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $\overline{\text{U/D}}$ to CP	12.0 12.0		12.0 12.0		12.0 12.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $\overline{\text{U/D}}$ to CP	0 0		0 0		0 0			
$t_w(\text{L})$	$\overline{\text{PL}}$ Pulse Width, LOW	6.0		8.5		6.0		ns	2-4
$t_w(\text{L})$	CP Pulse Width, LOW	5.0		7.0		5.0		ns	2-4
$t_{\text{rec}}$	Recovery Time $\overline{\text{PL}}$ to CP	6.0		7.5		6.0		ns	2-6

## 54F/74F191

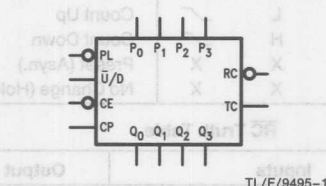
# Up/Down Binary Counter with Preset and Ripple Clock

## General Description

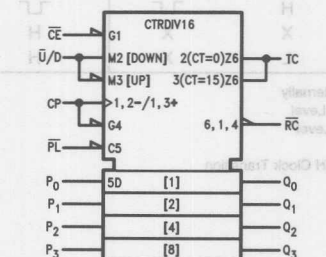
The 'F191 is a reversible modulo-16 binary counter featuring synchronous counting and asynchronous presetting. The preset feature allows the 'F191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

**Ordering Code:** See Section 5

## Logic Symbols



IEEE/IEC



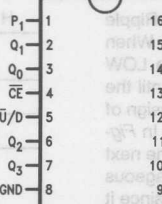
TL/F/9495-4

## Features

- High-Speed—125 MHz typical count frequency
- Synchronous counting
- Asynchronous parallel load
- Cascadable

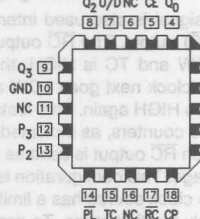
## Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak



TL/F/9495-2

Pin Assignment  
for LCC



TL/F/9495-3

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{CE}$	Count Enable Input (Active LOW)	1.0/3.0	20 $\mu$ A/ -1.8 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$P_0$ - $P_3$	Parallel Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
PL	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{U/D}$	Up/Down Count Control Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
$Q_0$ - $Q_3$	Flip-Flop Outputs	50/33.3	-1 mA/20 mA
RC	Ripple Clock Output (Active LOW)	50/33.3	-1 mA/20 mA
TC	Terminal Count Output (Active HIGH)	50/33.3	-1 mA/20 mA

## Functional Description

The 'F191 is a synchronous up/down 4-bit binary counter. It contains four edge-triggered flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load (PL) input is LOW, information present on the Parallel Data inputs (P<sub>0</sub>–P<sub>3</sub>) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the  $\overline{CE}$  input inhibits counting. When  $\overline{CE}$  is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the  $\overline{U/D}$  input signal, as indicated in the Mode Select Table.  $\overline{CE}$  and  $\overline{U/D}$  can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.



Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches 15 in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until  $\overline{U/D}$  is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ( $\overline{RC}$ ) output. The  $\overline{RC}$  output is normally HIGH. When  $\overline{CE}$  is LOW and TC is HIGH, the  $\overline{RC}$  output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figures 1 and 2. In Figure 1, each  $\overline{RC}$  output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on  $\overline{CE}$  inhibits the  $\overline{RC}$  output pulse, as indicated in the  $\overline{RC}$  Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.



A method of causing state changes to occur simultaneously in all stages is shown in Figure 2. All clock inputs are driven in parallel and the  $\overline{RC}$  outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the  $\overline{RC}$  output of any device goes HIGH shortly after its CP input goes HIGH.



The configuration shown in Figure 3 avoids ripple delays and their associated restrictions. The  $\overline{CE}$  input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures 1 and 2 doesn't apply, because the TC output of a given stage is not affected by its own  $\overline{CE}$ .

Mode Select Table

Inputs				Mode
PL	$\overline{CE}$	$\overline{U/D}$	CP	
H	L	L		Count Up
H	L	H		Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

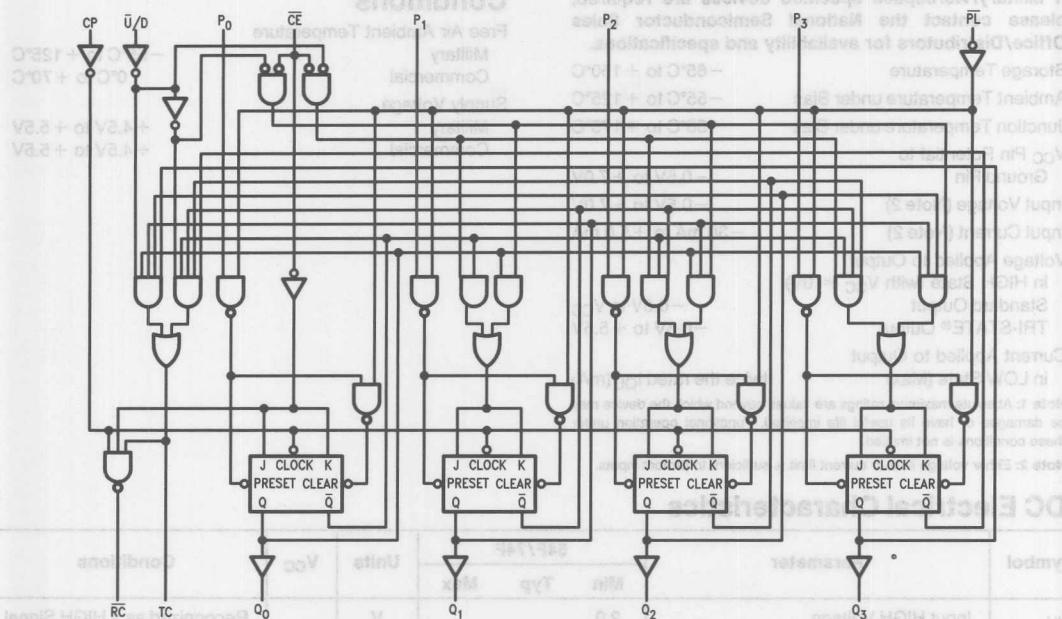
$\overline{RC}$  Truth Table

Inputs			Output
$\overline{CE}$	TC*	CP	
L	H		
H	X	X	H
X	L	X	H

\*TC is generated internally  
 H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 = LOW-to-HIGH Clock Transition  
 = LOW Pulse

Pin Name	Description	U.L.	Input/Output
TC	Terminal Count Output (Active HIGH)	50V/2.5A	Output
$\overline{RC}$	Ripple Clock Output (Active LOW)	50V/2.5A	Output
CP	Flip-Flop Outputs	50V/2.5A	Output
$\overline{U/D}$	Up/Down Count Control Input	50V/2.5A	Input
PL	Asynchronous Parallel Load Input (Active LOW)	50V/2.5A	Input
P <sub>0</sub> –P <sub>3</sub>	Parallel Data Inputs	50V/2.5A	Input
CP	Clock Pulse Input (Active Rising Edge)	50V/2.5A	Input
$\overline{CE}$	Count Enable Input (Active LOW)	50V/2.5A	Input

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

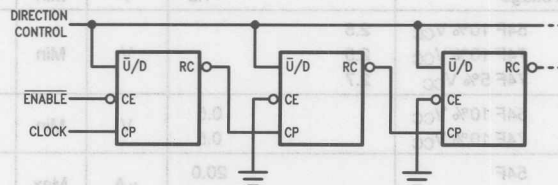


FIGURE 1. n-Stage Counter Using Ripple Clock

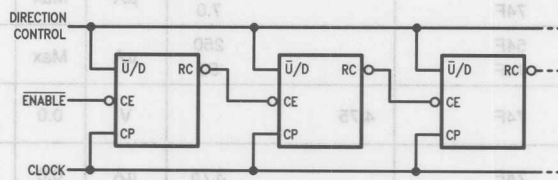


FIGURE 2. Synchronous n-Stage Counter Using Ripple Carry/Borrow

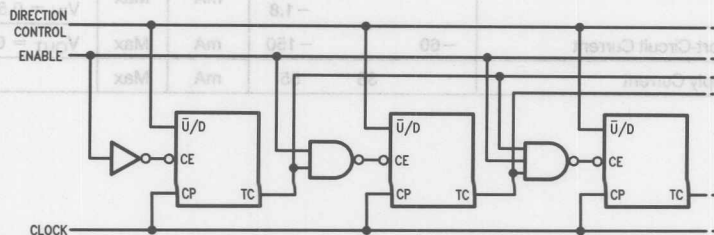


FIGURE 3. Synchronous n-Stage Counter with Gated Carry/Borrow



## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA, All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6 −1.8	mA	Max	V <sub>IN</sub> = 0.5V (except $\overline{CE}$ )
							V <sub>IN</sub> = 0.5V ( $\overline{CE}$ )
I <sub>OS</sub>	Output Short-Circuit Current	−60		−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		38	55			

## Recommended Operating Conditions

Free Air Ambient Temperature	−55°C to +125°C
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Count Frequency	100	125		75		90		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	3.0	5.5	7.5	3.0	9.5	3.0	8.5	ns	2-3
$t_{\text{PHL}}$	CP to $Q_n$	5.0	8.5	11.0	5.0	13.5	5.0	12.0		
$t_{\text{PLH}}$	Propagation Delay	6.0	10.0	13.0	6.0	16.5	6.0	14.0	ns	2-3
$t_{\text{PHL}}$	CP to TC	5.0	8.5	11.0	5.0	13.5	5.0	12.0		
$t_{\text{PLH}}$	Propagation Delay	3.0	5.5	7.5	3.0	9.5	3.0	8.5	ns	2-3
$t_{\text{PHL}}$	CP to $\overline{\text{RC}}$	3.0	5.0	7.0	3.0	9.0	3.0	8.0		
$t_{\text{PLH}}$	Propagation Delay	3.0	5.0	7.0	3.0	9.0	3.0	8.0	ns	2-3
$t_{\text{PHL}}$	$\overline{\text{CE}}$ to $\overline{\text{RC}}$	3.0	5.5	7.0	3.0	9.0	3.0	8.0		
$t_{\text{PLH}}$	Propagation Delay	7.0	11.0	18.0	7.0	22.0	7.0	20.0	ns	2-3
$t_{\text{PHL}}$	$\overline{\text{U/D}}$ to $\overline{\text{RC}}$	5.5	9.0	12.0	5.5	14.0	5.5	13.0		
$t_{\text{PLH}}$	Propagation Delay	4.0	7.0	10.0	4.0	13.5	4.0	11.0	ns	2-3
$t_{\text{PHL}}$	$\overline{\text{U/D}}$ to TC	4.0	6.5	10.0	4.0	12.5	4.0	11.0		
$t_{\text{PLH}}$	Propagation Delay	3.0	4.5	7.0	3.0	9.0	3.0	8.0	ns	2-3
$t_{\text{PHL}}$	$P_n$ to $Q_n$	6.0	10.0	13.0	6.0	16.0	6.0	14.0		
$t_{\text{PLH}}$	Propagation Delay	5.0	8.5	11.0	5.0	13.0	5.0	12.0	ns	2-3
$t_{\text{PHL}}$	$\overline{\text{PL}}$ to $Q_n$	5.5	9.0	12.0	5.5	14.5	5.5	13.0		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	4.5		6.0		5.0		ns	2-6
$t_s(\text{L})$	$P_n$ to $\overline{\text{PL}}$	4.5		6.0		5.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0		2.0		2.0		ns	2-6
$t_h(\text{L})$	$P_n$ to $\overline{\text{PL}}$	2.0		2.0		2.0			
$t_s(\text{L})$	Setup Time LOW $\overline{\text{CE}}$ to CP	10.0		10.5		10.0		ns	2-6
$t_h(\text{L})$	Hold Time LOW $\overline{\text{CE}}$ to CP	0		0		0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	12.0		12.0		12.0		ns	2-6
$t_s(\text{L})$	$\overline{\text{U/D}}$ to CP	12.0		12.0		12.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		0		0		ns	2-6
$t_h(\text{L})$	$\overline{\text{U/D}}$ to CP	0		0		0			
$t_w(\text{L})$	$\overline{\text{PL}}$ Pulse Width LOW	6.0		8.5		6.0		ns	2-4
$t_w(\text{L})$	CP Pulse Width LOW	5.0		7.0		5.0		ns	2-4
$t_{\text{rec}}$	Recovery Time $\overline{\text{PL}}$ to CP	6.0		7.5		6.0		ns	2-6



## 54F/74F192 Up/Down Decade Counter with Separate Up/Down Clocks

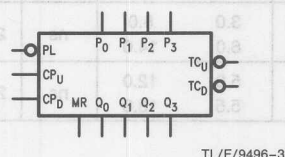
### General Description

The 'F192 is an up/down BCD decade (8421) counter. Separate Count Up and Count Down Clocks are used, and in either counting mode the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs.

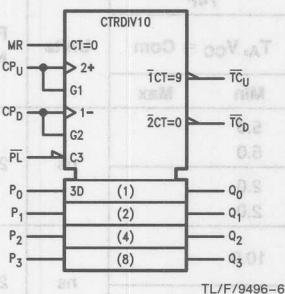
Separate Terminal Count Up and Terminal Count Down outputs are used as the clocks for a subsequent stage without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load (PL) and the Master Reset (MR) inputs asynchronously override the clocks.

**Ordering Code:** See Section 5

### Logic Symbols

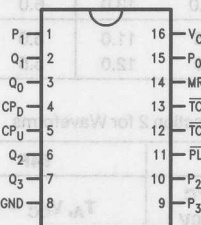


#### IEEE/IEC

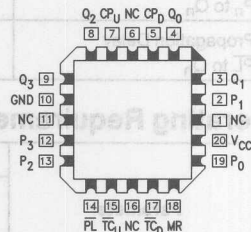


### Connection Diagrams

#### Pin Assignment for DIP, SOIC and Flatpak



#### Pin Assignment for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I <sub>IH</sub> /I <sub>IL</sub> Output I <sub>OH</sub> /I <sub>OL</sub>
CP <sub>U</sub>	Count Up Clock Input (Active Rising Edge)	1.0/3.0	20 $\mu$ A/ -1.8 mA
CP <sub>D</sub>	Count Down Clock Input (Active Rising Edge)	1.0/3.0	20 $\mu$ A/ -1.8 mA
MR	Asynchronous Master Reset Input (Active HIGH)	1.0/1.0	20 $\mu$ A/ -0.6 mA
PL	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
P <sub>0</sub> -P <sub>3</sub>	Parallel Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
Q <sub>0</sub> -Q <sub>3</sub>	Flip-Flop Outputs	50/33.3	-1 mA/20 mA
TC <sub>D</sub>	Terminal Count Down (Borrow) Output (Active LOW)	50/33.3	-1 mA/20 mA
TC <sub>U</sub>	Terminal Count Up (Carry) Output (Active LOW)	50/33.3	-1 mA/20 mA

## Functional Description

The 'F192 is an asynchronously presettable decade counter. It contains four edge-triggered flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

A LOW-to-HIGH transition on the CP input to each flip-flop causes the output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH, as indicated in the Function Table. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW.

The Terminal Count Up ( $\overline{TC}_U$ ) and Terminal Count Down ( $\overline{TC}_D$ ) outputs are normally HIGH. When the circuit has reached the maximum count state 9, the next HIGH-to-LOW transition of the Count Up Clock will cause  $\overline{TC}_U$  to go LOW.  $\overline{TC}_U$  will stay LOW until  $CP_U$  goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the  $\overline{TC}_D$  output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the TC outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.



$$\overline{TC}_U = Q_0 \cdot Q_3 \cdot \overline{CP}_U$$


$$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$$

The 'F192 has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ( $\overline{PL}$ ) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data input ( $P_0$ – $P_3$ ) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both clock inputs, and latch each Q output in the LOW state. If one of the clock inputs is LOW during and after a reset or

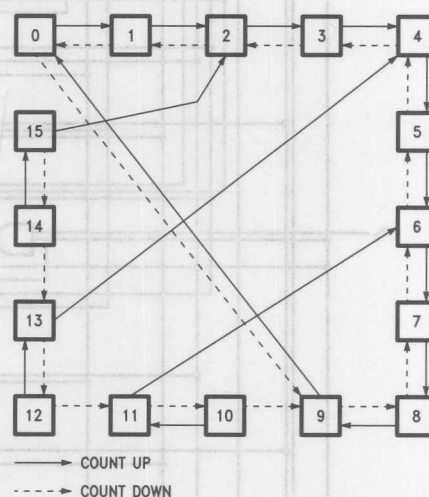
load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

Function Table

MR	$\overline{PL}$	$CP_U$	$CP_D$	Mode
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H		H	Count Up
L	H	H		Count Down

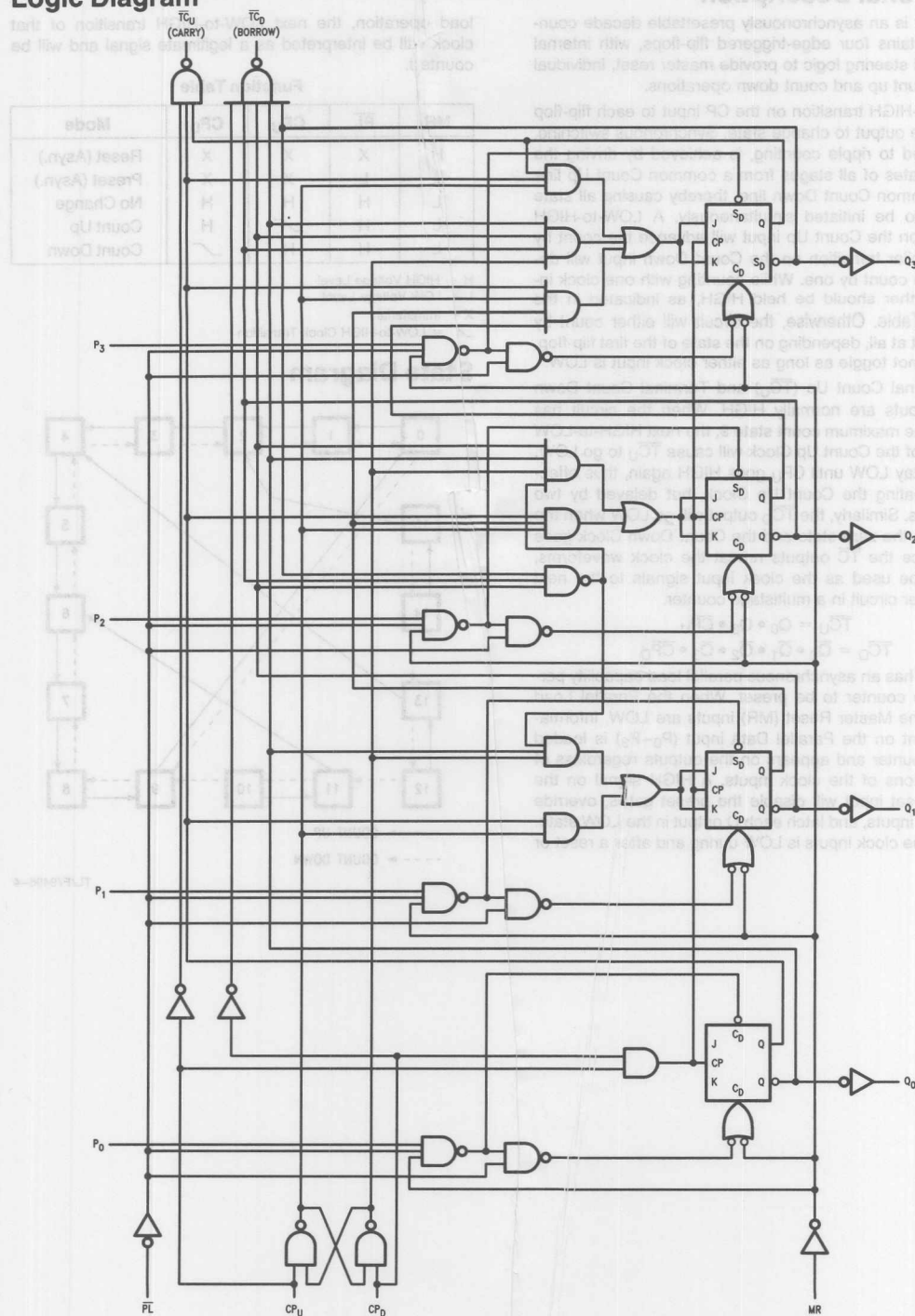
H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
 = LOW-to-HIGH Clock Transition

## State Diagram



TL/F/9496-4

# Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

TL/F/9496-5



**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	–0.5V to V <sub>CC</sub>
Standard Output	–0.5V to +5.5V
TRI-STATE® Output	–0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	–55°C to +125°C
Military	–55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			–1.2	V	Min	I <sub>IN</sub> = –18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = –1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = –1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = –1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			–0.6 –1.8	mA	Max	V <sub>IN</sub> = 0.5V, Except CP <sub>U</sub> , CP <sub>D</sub> V <sub>IN</sub> = 0.5V, CP <sub>U</sub> , CP <sub>D</sub>
I <sub>OS</sub>	Output Short-Circuit Current		–60	–150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCL</sub>	Power Supply Current		38	55	mA	Max	V <sub>O</sub> = LOW



**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	100	125		75		90		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay $CP_U$ or $CP_D$ to $\overline{TC}_U$ or $\overline{TC}_D$	4.0	7.0	9.0	4.0	10.5	4.0	10.0	ns	2-3
$t_{\text{PHL}}$		3.5	6.0	8.0	3.5	9.5	3.5	9.0		
$t_{\text{PLH}}$	Propagation Delay $CP_U$ or $CP_D$ to $Q_n$	4.0	6.5	8.5	4.0	10.0	4.0	9.5	ns	2-3
$t_{\text{PHL}}$		5.5	9.5	12.5	5.5	14.0	5.5	13.5		
$t_{\text{PLH}}$	Propagation Delay $P_n$ to $Q_n$	3.0	4.5	7.0	3.0	8.5	3.0	8.0	ns	2-3
$t_{\text{PHL}}$		6.0	11.0	14.5	6.0	16.5	6.0	15.5		
$t_{\text{PLH}}$	Propagation Delay $\overline{PL}$ to $Q_n$	5.0	8.5	11.0	5.0	13.5	5.0	12.0	ns	2-3
$t_{\text{PHL}}$		5.5	10.0	13.0	5.5	15.0	5.5	14.0		
$t_{\text{PHL}}$	Propagation Delay $MR$ to $Q_n$	6.5	11.0	14.5	6.5	16.0	6.5	15.5		
$t_{\text{PLH}}$	Propagation Delay $MR$ to $\overline{TC}_U$	6.0	10.5	13.5	6.0	15.0	6.0	14.5	ns	2-3
$t_{\text{PHL}}$	Propagation Delay $MR$ to $\overline{TC}_D$	7.0	11.5	14.5	7.0	16.0	7.0	15.5		
$t_{\text{PLH}}$	Propagation Delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	7.0	12.0	15.5	7.0	18.5	7.0	16.5	ns	2-3
$t_{\text{PHL}}$		7.0	11.5	14.5	7.0	17.5	7.0	15.5		
$t_{\text{PLH}}$	Propagation Delay $P_n$ to $\overline{TC}_U$ or $\overline{TC}_D$	7.0	11.5	14.5	7.0	16.5	7.0	15.5	ns	2-3
$t_{\text{PHL}}$		6.5	11.0	14.0	6.5	16.5	6.5	15.0		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $P_n$ to $\overline{\text{PL}}$	4.5 4.5		6.0 6.0		5.0 5.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $P_n$ to $\overline{\text{PL}}$	2.0 2.0		2.0 2.0		2.0 2.0			
$t_w(\text{L})$	$\overline{\text{PL}}$ Pulse Width, LOW	6.0		7.5		6.0		ns	2-4
$t_w(\text{L})$	$\text{CP}_U$ or $\text{CP}_D$ Pulse Width, LOW	5.0		7.0		5.0		ns	2-4
$t_w(\text{L})$	$\text{CP}_U$ or $\text{CP}_D$ Pulse Width, LOW (Change of Direction)	10.0		12.0		10.0		ns	2-4
$t_w(\text{H})$	$\overline{\text{MR}}$ Pulse Width, HIGH	6.0		6.0		6.0		ns	2-4
$t_{\text{rec}}$	Recovery Time $\overline{\text{PL}}$ to $\text{CP}_U$ or $\text{CP}_D$	6.0		8.0		6.0		ns	2-6
$t_{\text{rec}}$	Recovery Time $\text{MR}$ to $\text{CP}_U$ or $\text{CP}_D$	4.0		4.5		4.0		ns	2-6



## 54F/74F193 Up/Down Binary Counter with Separate Up/Down Clocks

### General Description

The 'F193 is an up/down modulo-16 binary counter. Separate Count Up and Count Down Clocks are used, and in either counting mode the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs. Separate Terminal Count Up and Terminal Count Down outputs are provided that are used as the clocks for subsequent stages without extra logic, thus simplifying multi-stage counter designs.

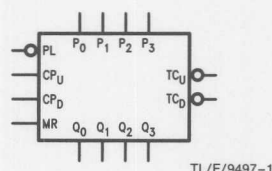
Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load (PL) and the Master Reset (MR) inputs asynchronously override the clocks.

### Features

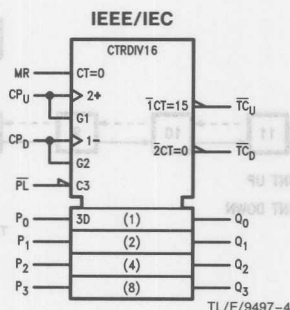
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

### Logic Symbols



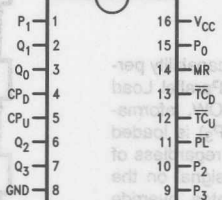
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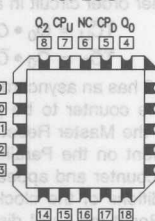
### Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9497-2

Pin Assignment for LCC



TL/F/9497-3

**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I <sub>IH</sub> /I <sub>IL</sub> Output I <sub>OH</sub> /I <sub>OL</sub>
CP <sub>U</sub>	Count Up Clock Input (Active Rising Edge)	1.0/3.0	20 $\mu$ A/ -1.8 mA
CP <sub>D</sub>	Count Down Clock Input (Active Rising Edge)	1.0/3.0	20 $\mu$ A/ -1.8 mA
MR	Asynchronous Master Reset Input (Active HIGH)	1.0/1.0	20 $\mu$ A/ -0.6 mA
PL	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
P <sub>0</sub> -P <sub>3</sub>	Parallel Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
Q <sub>0</sub> -Q <sub>3</sub>	Flip-Flop Outputs	50/33.3	-1 mA/20 mA
TC <sub>D</sub>	Terminal Count Down (Borrow) Output (Active LOW)	50/33.3	-1 mA/20 mA
TC <sub>U</sub>	Terminal Count Up (Carry) Output (Active LOW)	50/33.3	-1 mA/20 mA

## Functional Description

The 'F193 is a 4-bit binary synchronous up/down (reversible) counter. It contains four edge-triggered flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

A LOW-to-HIGH transition on the CP input to each flip-flop causes the output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH, as indicated in the Function Table.

The Terminal Count Up ( $\overline{TC}_U$ ) and Terminal Count Down ( $\overline{TC}_D$ ) outputs are normally HIGH. When the circuit has reached the maximum count state 15, the next HIGH-to-LOW transition of the Count Up Clock will cause  $\overline{TC}_U$  to go LOW.  $\overline{TC}_U$  will stay LOW until  $CP_U$  goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the  $\overline{TC}_D$  output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the  $\overline{TC}$  outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

$$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$$

$$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$$

The 'F193 has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load (PL) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data input ( $P_0$ – $P_3$ ) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both clock inputs, and latch each Q output in the LOW state.

If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

Function Table

MR	PL	CP <sub>U</sub>	CP <sub>D</sub>	Mode
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	↗	H	Count Up
L	H	H	↘	Count Down

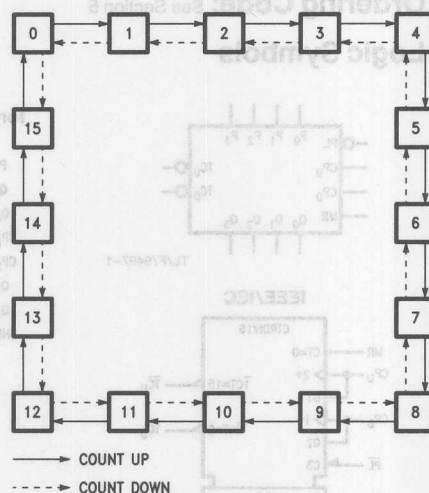
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH Clock Transition

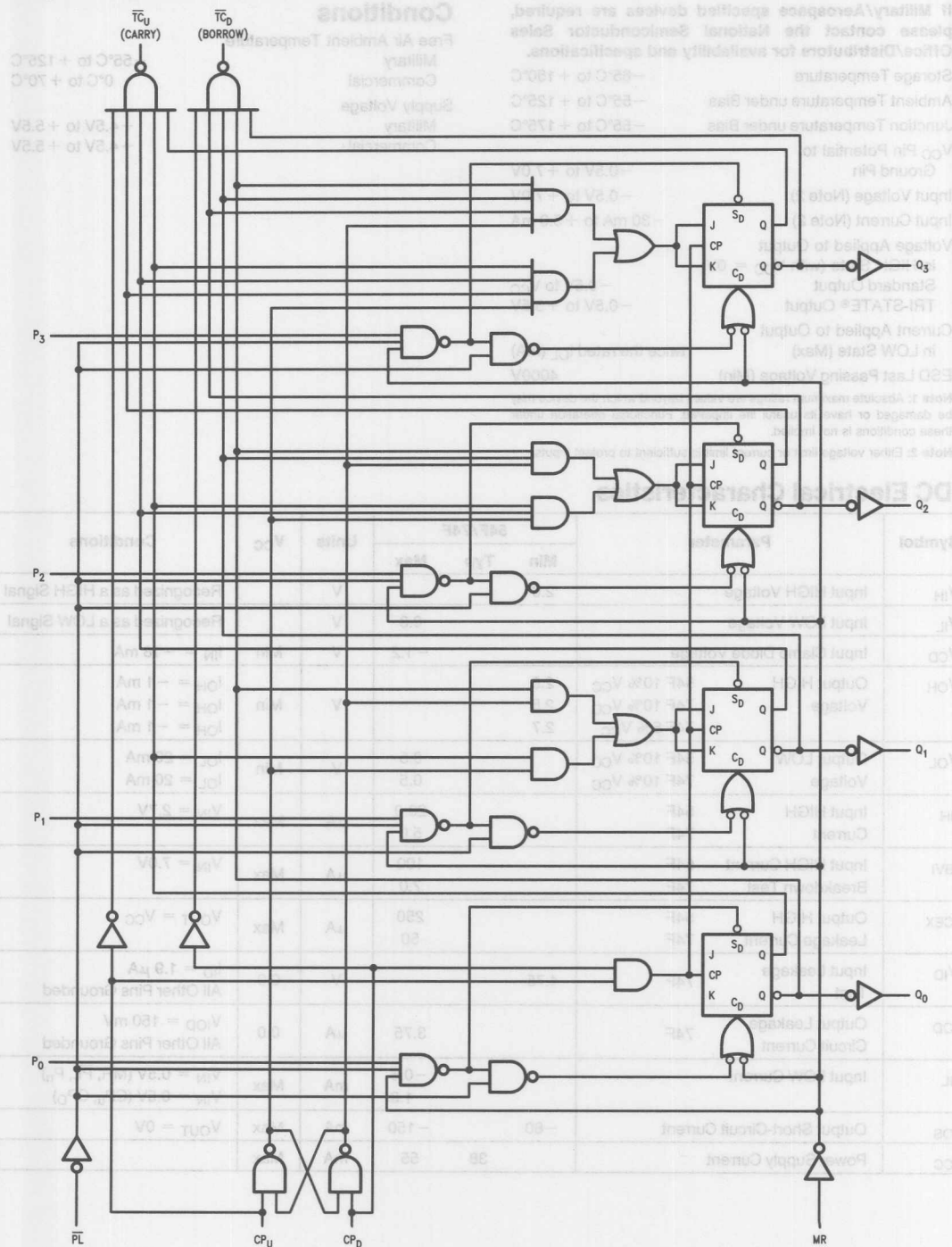
## State Diagram



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Pin Names	Description	U.L.	Input/Output
CP <sub>U</sub>	Count Up Clock Input (Active Rising Edge)	10V/3.0	Input
CP <sub>D</sub>	Count Down Clock Input (Active Rising Edge)	10V/3.0	Input
MR	Asynchronous Master Reset Input (Active HIGH)	10V/1.0	Input
PL	Asynchronous Parallel Load Input (Active LOW)	10V/1.0	Input
P <sub>0</sub> –P <sub>3</sub>	Parallel Data Inputs	10V/1.0	Input
Q <sub>0</sub> –Q <sub>3</sub>	Flip-Flop Outputs	50V/3.3	Output
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)	50V/3.3	Output
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)	50V/3.3	Output

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

ESD Last Passing Voltage (Min) 4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6 -1.8	mA	Max	V <sub>IN</sub> = 0.5V (MR, PL, P <sub>N</sub> ) V <sub>IN</sub> = 0.5V (CP <sub>U</sub> , CP <sub>D</sub> )
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		38	55	mA	Max	

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Count Frequency	100	125		75		90		MHz	2-1
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay $CP_U$ or $CP_D$ to $\overline{TC}_U$ or $\overline{TC}_D$	4.0 3.5	7.0 6.0	9.0 8.0	4.0 3.5	10.5 9.5	4.0 3.5	10.0 9.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay $CP_U$ or $CP_D$ to $Q_n$	4.0 5.5	6.5 9.5	8.5 12.5	3.5 5.5	10.0 14.0	4.0 5.5	9.5 13.5	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay $P_n$ to $Q_n$	3.0 6.0	4.5 11.0	7.0 14.5	3.0 6.0	8.5 16.5	3.0 6.0	8.0 15.5	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay $\overline{PL}$ to $Q_n$	5.0 5.5	8.5 10.0	11.0 13.0	5.0 5.5	13.5 15.0	5.0 5.5	12.0 14.0	ns	2-3
$t_{\text{PHL}}$	Propagation Delay MR to $Q_n$	5.5	11.0	14.5	5.0	16.0	5.5	15.5		
$t_{\text{PLH}}$	Propagation Delay MR to $\overline{TC}_U$	6.0	10.5	13.5	5.0	15.0	6.0	14.5	ns	2-3
$t_{\text{PHL}}$	Propagation Delay MR to $\overline{TC}_D$	6.0	11.5	14.5	6.0	16.0	6.0	15.5		
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	7.0 7.0	12.0 11.5	15.5 14.5	7.0 6.0	18.5 17.5	7.0 7.0	16.5 15.5	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay $P_n$ to $\overline{TC}_U$ or $\overline{TC}_D$	7.0 6.5	11.5 11.0	14.5 14.0	6.0 5.0	16.5 16.5	7.0 6.5	15.5 15.0	ns	2-3

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $P_n$ to $\overline{\text{PL}}$	4.5 4.5		6.0 6.0		5.0 5.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $P_n$ to $\overline{\text{PL}}$	2.0 2.0		2.0 2.0		2.0 2.0			
$t_w(\text{L})$	$\overline{\text{PL}}$ Pulse Width, LOW	6.0		7.5		6.0		ns	2-4
$t_w(\text{L})$	$\text{CP}_U$ or $\text{CP}_D$ Pulse Width, LOW	5.0		7.0		5.0		ns	2-4
$t_w(\text{L})$	$\text{CP}_U$ or $\text{CP}_D$ Pulse Width, LOW (Change of Direction)	10.0		12.0		10.0		ns	2-4
$t_w(\text{H})$	MR Pulse Width, HIGH	6.0		6.0		6.0		ns	2-4
$t_{\text{rec}}$	Recovery Time $\overline{\text{PL}}$ to $\text{CP}_U$ or $\text{CP}_D$	6.0		8.0		6.0		ns	2-6
$t_{\text{rec}}$	Recovery Time MR to $\text{CP}_U$ or $\text{CP}_D$	4.0		4.5		4.0		ns	2-6




**54F/74F194**

## 4-Bit Bidirectional Universal Shift Register

### General Description

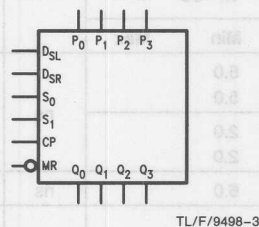
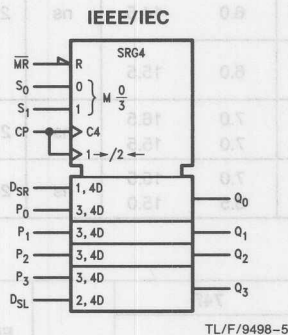
The 'F194 is a high-speed 4-bit bidirectional universal shift register. As a high-speed, multifunctional, sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The 'F194 is similar in operation to the 'F195 universal shift register, with added features of shift left without external connections and hold (do nothing) modes of operation.

### Features

- Typical shift frequency of 150 MHz
- Asynchronous master reset
- Hold (do nothing) mode
- Fully synchronous serial or parallel data transfers

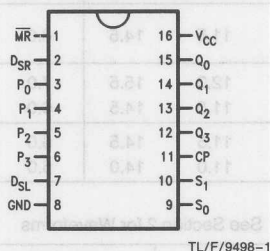
**Ordering Code:** See Section 5

### Logic Symbols

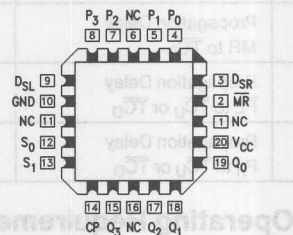


### Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak



Pin Assignment  
for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$S_0, S_1$	Mode Control Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
$P_0-P_3$	Parallel Data Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
DSR	Serial Data Input (Shift Right)	1.0/1.0	20 $\mu A$ / -0.6 mA
DSL	Serial Data Input (Shift Left)	1.0/1.0	20 $\mu A$ / -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu A$ / -0.6 mA
MR	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$Q_0-Q_3$	Parallel Outputs	50/33.3	-1 mA/20 mA

## Functional Description

The 'F194 contains four edge-triggered D flip-flops and the necessary interstage logic to synchronously perform shift right, shift left, parallel load and hold operations. Signals applied to the Select ( $S_0, S_1$ ) inputs determine the type of operation, as shown in the Mode Select Table. Signals on the Select, Parallel data ( $P_0$ – $P_3$ ) and Serial data ( $D_{SR}, D_{SL}$ )

inputs can change when the clock is in either state, provided only that the recommended setup and hold times, with respect to the clock rising edge, are observed. A LOW signal on Master Reset ( $\overline{MR}$ ) overrides all other inputs and forces the outputs LOW.

Mode Select Table

Operating Mode	Inputs						Outputs			
	$\overline{MR}$	$S_1$	$S_0$	$D_{SR}$	$D_{SL}$	$P_n$	$Q_0$	$Q_1$	$Q_2$	$Q_3$
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	$q_0$	$q_1$	$q_2$	$q_3$
Shift Left	H	h	l	X	l	X	$q_1$	$q_2$	$q_3$	L
	H	h	l	X	h	X	$q_1$	$q_2$	$q_3$	H
Shift Right	H	l	h	l	X	X	L	$q_0$	$q_1$	$q_2$
	H	l	h	h	X	X	H	$q_0$	$q_1$	$q_2$
Parallel Load	H	h	h	X	X	$P_n$	$P_0$	$P_1$	$P_2$	$P_3$

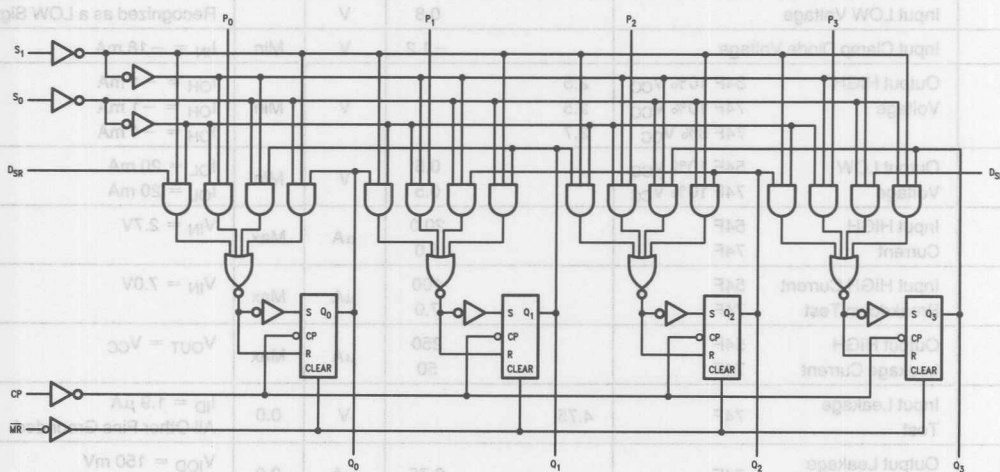
H (h) = High Voltage Level

L (l) = Low Voltage Level

$P_n$  ( $q_n$ ) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.

X = Immaterial

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

TL/F/9498-4

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
---	----------------

Input Voltage (Note 2)	−0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	−30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		33	46	mA	Max	

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Shift Frequency	105	150		90		90		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	3.5	5.2	7.0	3.0	8.5	3.5	8.0	ns	2-3
$t_{\text{PHL}}$	CP to $Q_n$	3.5	5.5	7.0	3.0	8.5	3.5	8.0		
$t_{\text{PHL}}$	Propagation Delay MR to $Q_n$	4.5	8.6	12.0	4.5	14.5	4.5	14.0	ns	2-3

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW $P_n$ or $D_{SR}$ or $D_{SL}$ to CP	4.0		6.0		4.0		ns	2-6
$t_s(\text{L})$		4.0		4.0		4.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW $P_n$ or $D_{SR}$ or $D_{SL}$ to CP	1.0		1.5		1.0			
$t_h(\text{L})$		0		1.0		1.0			
$t_s(\text{H})$	Setup Time, HIGH or LOW $S_n$ to CP	10.0		10.5		11.0		ns	2-6
$t_s(\text{L})$		8.0		8.0		8.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW $S_n$ to CP	0		0		0			
$t_h(\text{L})$		0		0		0			
$t_w(\text{H})$	CP Pulse Width, HIGH	5.0		5.5		5.5		ns	2-4
$t_w(\text{L})$	$\overline{\text{MR}}$ Pulse Width, LOW	5.0		5.0		5.0		ns	2-4
$t_{\text{rec}}$	Recovery Time $\overline{\text{MR}}$ to CP	9.0		9.0		11.0		ns	2-6

Pin Names	Description	U.L.	Input/Output
$A_0-A_2$	Address Inputs	1.0/1.0	Input
$\overline{\text{CS}}$	Chip Select Input (Active LOW)	1.0/2.0	Input
$\overline{\text{WE}}$	Write Enable Input (Active LOW)	1.0/1.0	Input
$D_0-D_7$	Data Inputs	1.0/1.0	Input
$D_0-D_7$	TRI-STATE Data Outputs	180/40 (23.8)	Output


**54F/74F219**

## 64-Bit Random Access Memory with TRI-STATE® Outputs

### General Description

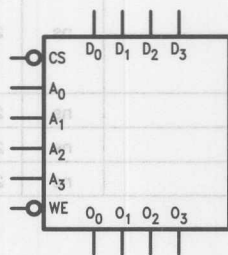
The 'F219 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are TRI-STATE and are in the high-impedance state whenever the Chip Select ( $\overline{CS}$ ) input is HIGH. The outputs are active only in the Read mode. This device is similar to the 'F189 but features non-inverting, rather than inverting, data outputs.

### Features

- TRI-STATE outputs for data bus applications
- Buffered inputs minimize loading
- Address decoding on-chip
- Diode clamped inputs minimize ringing
- Available in SOIC (300 mil only)

**Ordering Code:** See Section 5

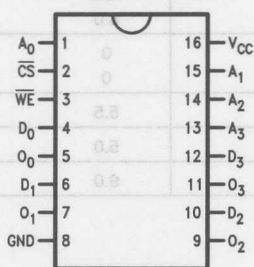
### Logic Symbol



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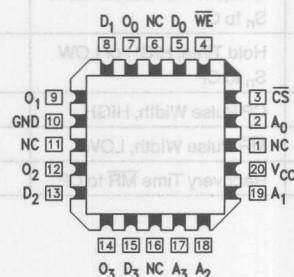
### Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak



TL/F/9500-2

Pin Assignment  
for LCC



TL/F/9500-3

**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_0-A_3$	Address Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/2.0	20 $\mu A$ / -1.2 mA
$\overline{WE}$	Write Enable Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$D_0-D_3$	Data Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
$O_0-O_3$	TRI-STATE Data Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

Function Table

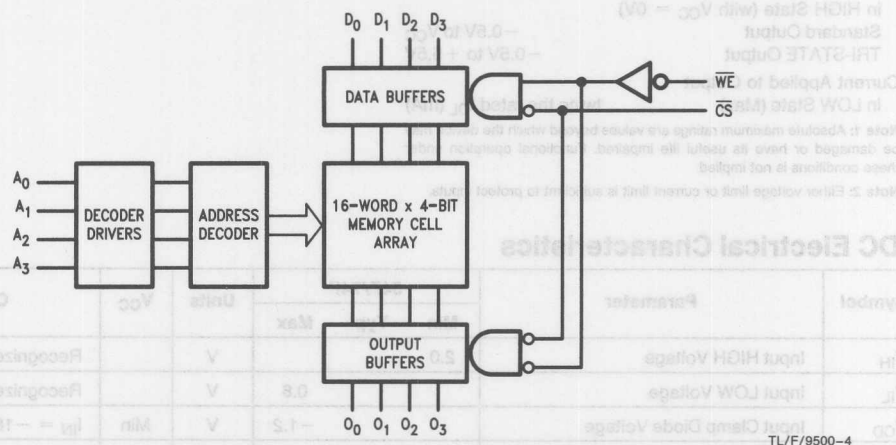
Inputs		Operation	Condition of Outputs
CS	WE		
L	L	Write	High Impedance
L	H	Read	True Stored Data
H	X	Inhibit	High Impedance

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

## Block Diagram



Symbol	Parameter	Units	Max	Min	Conditions
$V_{IH}$	Input HIGH Voltage	V			Recognized as a HIGH signal
$V_{IL}$	Input LOW Voltage	V	0.8		Recognized as a LOW signal
$V_{DD}$	Input Clamp Diode Voltage	V	-1.5		$I_{CL} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	V			$I_{OH} = -1 \text{ mA}$ $I_{OH} = -3 \text{ mA}$ $I_{OH} = -1 \text{ mA}$ $I_{OH} = -3 \text{ mA}$ $I_{OH} = -1 \text{ mA}$ $I_{OH} = -3 \text{ mA}$
$V_{OL}$	Output LOW Voltage	V			$I_{OL} = 20 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
$I_{IH}$	Input HIGH Current	$\mu\text{A}$	20.0		$V_{IH} = 2.7 \text{ V}$
$I_{IH}$	Input HIGH Current	$\mu\text{A}$	100		$V_{IH} = 7.0 \text{ V}$
$I_{OH}$	Output HIGH Current	$\mu\text{A}$	220		$V_{OH} = V_{DD}$
$I_{OL}$	Output LOW Current	$\mu\text{A}$	50		
$I_{IP}$	Input Leakage Current	$\mu\text{A}$			$I_{IP} = 1.8 \mu\text{A}$ All Other Pins Grounded
$I_{OP}$	Output Leakage Current	$\mu\text{A}$			$V_{DD} = 150 \text{ mV}$ All Other Pins Grounded
$I_{IL}$	Input LOW Current	$\text{mA}$	-0.8		$V_{IH} = 0.3 \text{ V}$ ( $A_0, WE, D_0$ ) $V_{IL} = 0.3 \text{ V}$ ( $D_3$ )
$I_{OH}$	Output Leakage Current	$\mu\text{A}$	50		$V_{OH} = 2.7 \text{ V}$
$I_{OL}$	Output Leakage Current	$\mu\text{A}$	-50		$V_{OH} = 0.3 \text{ V}$
$I_{OS}$	Output Short-Circuit Current	$\text{mA}$	-150		$V_{OH} = 0 \text{ V}$
$I_{DZ}$	Bus Drainage Test	$\mu\text{A}$	500		$V_{OH} = 2.5 \text{ V}$
$I_{CC}$	Power Supply Current	$\text{mA}$	55		



## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6 −1.2	mA	Max	V <sub>IN</sub> = 0.5V (A <sub>n</sub> , $\overline{WE}$ , D <sub>n</sub> ) V <sub>IN</sub> = 0.5V ( $\overline{CS}$ )
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CC</sub>	Power Supply Current		37	55	mA	Max	

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Access Time, HIGH or LOW	10.0	18.5	26.0	9.0	32.0	10.0	27.0	ns	2-3
$t_{PHL}$	$A_n$ to $O_n$	8.0	13.5	19.0	8.0	23.0	8.0	20.0		
$t_{PZH}$	Access Time, HIGH or LOW	3.5	6.0	8.5	3.5	10.5	3.5	9.5	ns	2-5
$t_{PZL}$	$\overline{CS}$ to $O_n$	5.0	9.0	13.0	5.0	15.0	5.0	14.0		
$t_{PHZ}$	Disable Time, HIGH or LOW	2.0	4.0	6.0	2.0	8.0	2.0	7.0	ns	2-5
$t_{PLZ}$	$\overline{CS}$ to $O_n$	3.0	5.5	8.0	2.5	10.0	3.0	9.0		
$t_{PZH}$	Write Recovery Time	6.5	20.0	28.0	6.5	37.5	6.5	29.0	ns	2-5
$t_{PZL}$	HIGH or LOW, $\overline{WE}$ to $O_n$	6.5	11.0	15.5	6.5	17.5	6.5	16.5		
$t_{PHZ}$	Disable Time, HIGH or LOW	4.0	7.0	10.0	3.5	12.0	4.0	11.0	ns	2-5
$t_{PLZ}$	$\overline{WE}$ to $O_n$	5.0	9.0	13.0	5.0	15.0	5.0	14.0		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	0		0		0		ns	2-6
$t_s(\text{L})$	$A_n$ to $\overline{\text{WE}}$	0		0		0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0		2.0		2.0		ns	2-6
$t_h(\text{L})$	$A_n$ to $\overline{\text{WE}}$	2.0		2.0		2.0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	10.0		11.0		10.0		ns	2-6
$t_s(\text{L})$	$D_n$ to $\overline{\text{WE}}$	10.0		11.0		10.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		2.0		0		ns	2-6
$t_h(\text{L})$	$D_n$ to $\overline{\text{WE}}$	0		2.0		0			
$t_s(\text{L})$	Setup Time, LOW $\overline{\text{CS}}$ to $\overline{\text{WE}}$	0		0		0		ns	2-6
$t_h(\text{L})$	Hold Time, LOW $\overline{\text{CS}}$ to $\overline{\text{WE}}$	6.0		7.5		6.0			
$t_w(\text{L})$	$\overline{\text{WE}}$ Pulse Width, LOW	6.0		7.5		6.0		ns	2-4



## 54F/74F240•54F/74F241•54F/74F244

### Octal Buffers/Line Drivers with TRI-STATE® Outputs

#### General Description

The 'F240, 'F241 and 'F244 are octal buffers and line drivers designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC and board density.

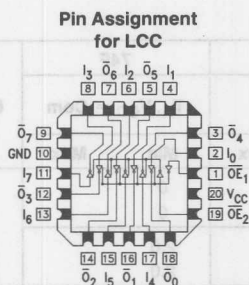
#### Features

- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs sink 64 mA (48 mA mil)
- 12 mA source current
- Input clamp diodes limit high-speed termination effects
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

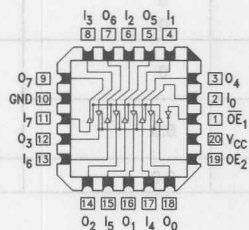
#### Connection Diagrams

'F240



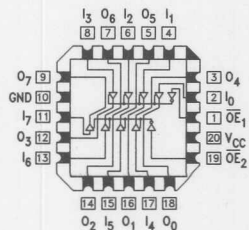
TL/F/9501-2

'F241



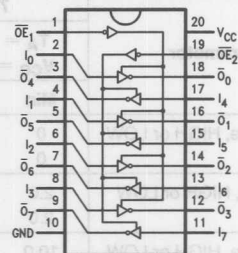
TL/F/9501-4

'F244

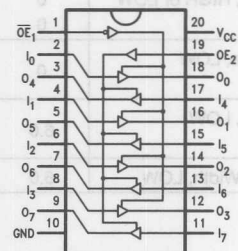


TL/F/9501-6

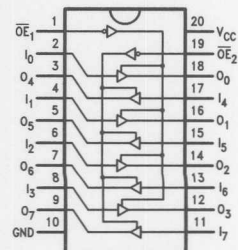
**Pin Assignment for DIP, SOIC and Flatpak**



TL/F/9501-1

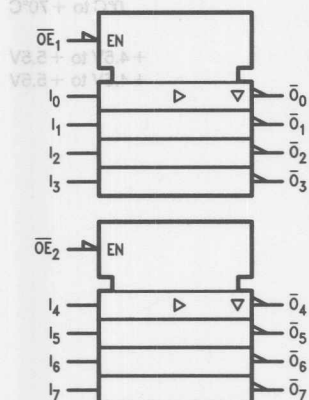


TL/F/9501-3

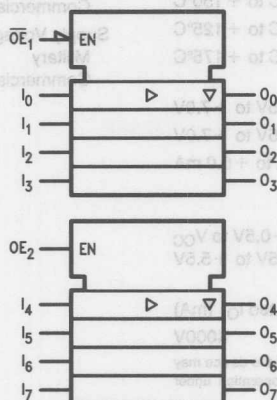


TL/F/9501-5

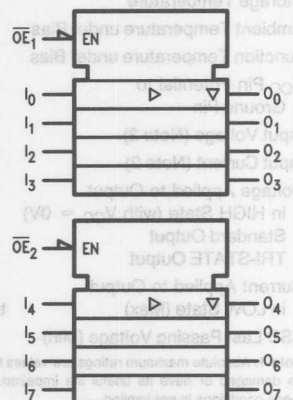
## Logic Symbols

IEEE/IEC  
'F240

TL/F/9501-7

IEEE/IEC  
'F241

TL/F/9501-8

IEEE/IEC  
'F244

TL/F/9501-9

## Unit Loading/Fan Out: See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{OE}_1, \overline{OE}_2$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.667	20 $\mu A$ / -1 mA
$OE_2$	TRI-STATE Output Enable Input (Active HIGH)	1.0/1.667	20 $\mu A$ / -1 mA
$I_0-I_7$	Inputs ('F240)	1.0/1.667*	20 $\mu A$ / -1 mA
$I_0-I_7$	Inputs ('F241, 'F244)	1.0/2.667*	20 $\mu A$ / -1.6 mA
$\overline{O}_0-\overline{O}_7, O_0-O_7$	Outputs	600/106.6 (80)	-12 mA/64 mA (48 mA)

\*Worst-case 'F240 enabled; 'F241, 'F244 disabled

## Truth Tables

'F240

$\overline{OE}_1$	$D_{1n}$	$O_{1n}$	$\overline{OE}_2$	$D_{2n}$	$O_{2n}$
H	X	Z	H	X	Z
L	H	L	L	H	H
L	L	H	L	L	H

'F241

$\overline{OE}_1$	$D_{1n}$	$O_{1n}$	$OE_2$	$D_{2n}$	$O_{2n}$
H	X	Z	L	X	Z
L	H	H	H	H	H
L	L	L	H	L	L

'F244

$\overline{OE}_1$	$D_{1n}$	$O_{1n}$	$\overline{OE}_2$	$D_{2n}$	$O_{2n}$
H	X	Z	H	X	Z
L	H	H	L	H	H
L	L	L	L	L	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.4		V	Min	I <sub>OH</sub> = −3 mA
		54F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = −12 mA
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = −15 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.55	V	Min	I <sub>OL</sub> = 48 mA
		74F 10% V <sub>CC</sub>		0.55			I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BV</sub>	Input HIGH Current Breakdown Test	54F		100	μA	μA	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−1.0 −1.6	mA	Max	V <sub>IN</sub> = 0.5V ( $\overline{OE}_1, \overline{OE}_2, OE_2, D_n$ ('F240')) V <sub>IN</sub> = 0.5V ( $D_n$ ('F241', 'F244'))
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−100	−225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V

**DC Electrical Characteristics** (Continued)

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
I <sub>CCH</sub>	Power Supply Current ('F240)		19	29	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current ('F240)		50	75	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current ('F240)		42	63	mA	Max	V <sub>O</sub> = HIGH Z
I <sub>CCH</sub>	Power Supply Current ('F241, 'F244)		40	60	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current ('F241, 'F244)		60	90	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current ('F241, 'F244)		60	90	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	3.0	5.1	7.0	3.0	9.0	3.0	8.0	ns	2-3
t <sub>PHL</sub>	Data to Output ('F240)	2.0	3.5	4.7	2.0	6.0	2.0	5.7		
t <sub>PZH</sub>	Output Enable Time ('F240)	2.0	3.5	4.7	2.0	6.5	2.0	5.7	ns	2-5
t <sub>PZL</sub>		4.0	6.9	9.0	4.0	10.5	4.0	10.0		
t <sub>PHZ</sub>	Output Disable Time ('F240)	2.0	4.0	5.3	2.0	6.5	2.0	6.3		
t <sub>PLZ</sub>		2.0	6.0	8.0	2.0	12.5	2.0	9.5	ns	2-3
t <sub>PLH</sub>	Propagation Delay	2.5	4.0	5.2	2.0	6.5	2.5	6.2		
t <sub>PHL</sub>	Data to Output ('F241, 'F244)	2.5	4.0	5.2	2.0	7.0	2.5	6.5		
t <sub>PZH</sub>	Output Enable Time ('F241, 'F244)	2.0	4.3	5.7	2.0	7.0	2.0	6.7	ns	2-5
t <sub>PZL</sub>		2.0	5.4	7.0	2.0	8.5	2.0	8.0		
t <sub>PHZ</sub>	Output Disable Time ('F241, 'F244)	2.0	4.5	6.0	2.0	7.0	2.0	7.0		
t <sub>PLZ</sub>		2.0	4.5	6.0	2.0	7.5	2.0	7.0		

Pin Names	Description	U.L.	Input/Output
E <sub>1</sub>	Enable Input (Active LOW)	1.0V/87	Input
E <sub>2</sub>	Enable Input (Active HIGH)	1.0V/87	Input
A <sub>0</sub>	Inputs	0.5V/87	Input
A <sub>1</sub>	Inputs	0.5V/87	Input
A <sub>2</sub>	Inputs	0.5V/87	Input
A <sub>3</sub>	Inputs	0.5V/87	Input
A <sub>4</sub>	Inputs	0.5V/87	Input
A <sub>5</sub>	Inputs	0.5V/87	Input
A <sub>6</sub>	Inputs	0.5V/87	Input
A <sub>7</sub>	Inputs	0.5V/87	Input
A <sub>8</sub>	Inputs	0.5V/87	Input
A <sub>9</sub>	Inputs	0.5V/87	Input
A <sub>10</sub>	Inputs	0.5V/87	Input
A <sub>11</sub>	Inputs	0.5V/87	Input
A <sub>12</sub>	Inputs	0.5V/87	Input
A <sub>13</sub>	Inputs	0.5V/87	Input
A <sub>14</sub>	Inputs	0.5V/87	Input
A <sub>15</sub>	Inputs	0.5V/87	Input
A <sub>16</sub>	Inputs	0.5V/87	Input
A <sub>17</sub>	Inputs	0.5V/87	Input
A <sub>18</sub>	Inputs	0.5V/87	Input
A <sub>19</sub>	Inputs	0.5V/87	Input
A <sub>20</sub>	Inputs	0.5V/87	Input
A <sub>21</sub>	Inputs	0.5V/87	Input
A <sub>22</sub>	Inputs	0.5V/87	Input
A <sub>23</sub>	Inputs	0.5V/87	Input
A <sub>24</sub>	Inputs	0.5V/87	Input
A <sub>25</sub>	Inputs	0.5V/87	Input
A <sub>26</sub>	Inputs	0.5V/87	Input
A <sub>27</sub>	Inputs	0.5V/87	Input
A <sub>28</sub>	Inputs	0.5V/87	Input
A <sub>29</sub>	Inputs	0.5V/87	Input
A <sub>30</sub>	Inputs	0.5V/87	Input
A <sub>31</sub>	Inputs	0.5V/87	Input
A <sub>32</sub>	Inputs	0.5V/87	Input
A <sub>33</sub>	Inputs	0.5V/87	Input
A <sub>34</sub>	Inputs	0.5V/87	Input
A <sub>35</sub>	Inputs	0.5V/87	Input
A <sub>36</sub>	Inputs	0.5V/87	Input
A <sub>37</sub>	Inputs	0.5V/87	Input
A <sub>38</sub>	Inputs	0.5V/87	Input
A <sub>39</sub>	Inputs	0.5V/87	Input
A <sub>40</sub>	Inputs	0.5V/87	Input
A <sub>41</sub>	Inputs	0.5V/87	Input
A <sub>42</sub>	Inputs	0.5V/87	Input
A <sub>43</sub>	Inputs	0.5V/87	Input
A <sub>44</sub>	Inputs	0.5V/87	Input
A <sub>45</sub>	Inputs	0.5V/87	Input
A <sub>46</sub>	Inputs	0.5V/87	Input
A <sub>47</sub>	Inputs	0.5V/87	Input
A <sub>48</sub>	Inputs	0.5V/87	Input
A <sub>49</sub>	Inputs	0.5V/87	Input
A <sub>50</sub>	Inputs	0.5V/87	Input
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A <sub>70</sub>	Inputs	0.5V/87	Input
A <sub>71</sub>	Inputs	0.5V/87	Input
A <sub>72</sub>	Inputs	0.5V/87	Input
A <sub>73</sub>	Inputs	0.5V/87	Input
A <sub>74</sub>	Inputs	0.5V/87	Input
A <sub>75</sub>	Inputs	0.5V/87	Input
A <sub>76</sub>	Inputs	0.5V/87	Input
A <sub>77</sub>	Inputs	0.5V/87	Input
A <sub>78</sub>	Inputs	0.5V/87	Input
A <sub>79</sub>	Inputs	0.5V/87	Input
A <sub>80</sub>	Inputs	0.5V/87	Input
A <sub>81</sub>	Inputs	0.5V/87	Input
A <sub>82</sub>	Inputs	0.5V/87	Input
A <sub>83</sub>	Inputs	0.5V/87	Input
A <sub>84</sub>	Inputs	0.5V/87	Input
A <sub>85</sub>	Inputs	0.5V/87	Input
A <sub>86</sub>	Inputs	0.5V/87	Input
A <sub>87</sub>	Inputs	0.5V/87	Input
A <sub>88</sub>	Inputs	0.5V/87	Input
A <sub>89</sub>	Inputs	0.5V/87	Input
A <sub>90</sub>	Inputs	0.5V/87	Input
A <sub>91</sub>	Inputs	0.5V/87	Input
A <sub>92</sub>	Inputs	0.5V/87	Input
A <sub>93</sub>	Inputs	0.5V/87	Input
A <sub>94</sub>	Inputs	0.5V/87	Input
A <sub>95</sub>	Inputs	0.5V/87	Input
A <sub>96</sub>	Inputs	0.5V/87	Input
A <sub>97</sub>	Inputs	0.5V/87	Input
A <sub>98</sub>	Inputs	0.5V/87	Input
A <sub>99</sub>	Inputs	0.5V/87	Input
A <sub>100</sub>	Inputs	0.5V/87	Input

H = HIGH Voltage Level  
L = LOW Voltage Level  
Z = High Impedance  
N/A = Not Allowed

Inputs	Outputs
E <sub>1</sub>	L
E <sub>2</sub>	L
A <sub>0</sub>	L
A <sub>1</sub>	L
A <sub>2</sub>	L
A <sub>3</sub>	L
A <sub>4</sub>	L
A <sub>5</sub>	L
A <sub>6</sub>	L
A <sub>7</sub>	L
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A <sub>73</sub>	L
A <sub>74</sub>	L
A <sub>75</sub>	L
A <sub>76</sub>	L
A <sub>77</sub>	L
A <sub>78</sub>	L
A <sub>79</sub>	L
A <sub>80</sub>	L
A <sub>81</sub>	L
A <sub>82</sub>	L
A <sub>83</sub>	L
A <sub>84</sub>	L
A <sub>85</sub>	L
A <sub>86</sub>	L
A <sub>87</sub>	L
A <sub>88</sub>	L
A <sub>89</sub>	L
A <sub>90</sub>	L
A <sub>91</sub>	L
A <sub>92</sub>	L
A <sub>93</sub>	L
A <sub>94</sub>	L
A <sub>95</sub>	L
A <sub>96</sub>	L
A <sub>97</sub>	L
A <sub>98</sub>	L
A <sub>99</sub>	L
A <sub>100</sub>	L





## 54F/74F243

### Quad Bus Transceiver with TRI-STATE® Outputs

#### General Description

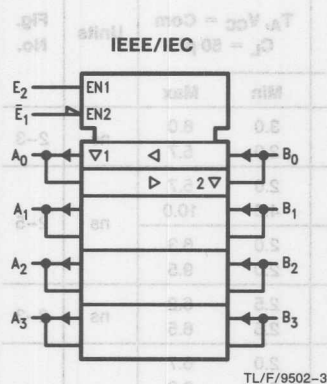
The 'F243 is a quad bus transmitter/receiver designed for 4-line asynchronous 2-way data communications between data busses.

#### Features

- 2-Way asynchronous data bus communication
- Input clamp diodes limit high-speed termination effects
- Guaranteed 4000V minimum ESD protection

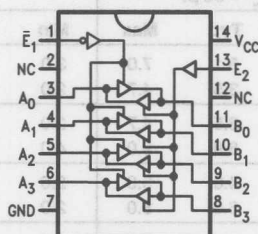
**Ordering Code:** See Section 5

#### Logic Symbol



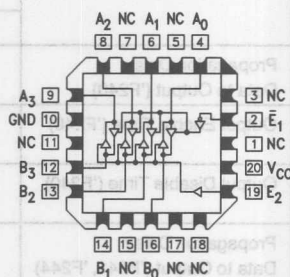
#### Connection Diagrams

Pin Assignment  
for DIP, SOIC and Flatpak



TL/F/9502-1

Pin Assignment  
for LCC



TL/F/9502-2

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\bar{E}_1$	Enable Input (Active LOW)	1.0/1.67	20 $\mu$ A / -1 mA
$E_2$	Enable Input (Active HIGH)	1.0/1.67	20 $\mu$ A / -1 mA
$A_n, B_n$	Inputs	3.5/2.67	70 $\mu$ A / -1.6 mA
	Outputs	600/106.6(80)	-12 mA/64 mA(48 mA)

#### Truth Table

Inputs		Inputs/Outputs	
$\bar{E}_1$	$E_2$	$A_n$	$B_n$
L	L	Input	B = A
L	H	N/A	N/A
H	L	Z	Z
H	H	A = B	Input

H = HIGH Voltage Level  
L = LOW Voltage Level  
Z = High Impedance  
N/A = Not Allowed

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

ESD Last Passing Voltage (Min) 4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.4 2.0 2.4 2.0 2.7		V	Min	I <sub>OH</sub> = −3 mA (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OH</sub> = −12 mA (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OH</sub> = −3 mA (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OH</sub> = −15 mA (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OH</sub> = −3 mA (A <sub>n</sub> , B <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.55 0.55	V	Min	I <sub>OL</sub> = 48 mA (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OL</sub> = 64 mA (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V (E <sub>1</sub> , E <sub>2</sub> )
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)	54F 74F		1.0 0.5	mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−1.0	mA	Max	V <sub>IN</sub> = 0.5V (E <sub>1</sub> , E <sub>2</sub> )
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			−1.6	mA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current		−100	−225	mA	Max	V <sub>OUT</sub> = 0V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CCH</sub>	Power Supply Current		64	80	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		64	90	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		71	90	mA	Max	V <sub>O</sub> = HIGH Z

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n$ to $B_n$ , $B_n$ to $A_n$	2.5 2.5	4.0 4.0	5.2 5.2	2.0 2.0	6.5 8.5	2.0 2.0	6.2 6.5	ns	2-3
$t_{pZH}$ $t_{pZL}$	Output Enable Time $\bar{E}_1$ to $B_n$ , $E_2$ to $A_n$	2.0 2.0	4.3 5.8	5.7 7.5	2.0 2.0	8.0 10.5	2.0 2.0	6.7 8.5	ns	2-5
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\bar{E}_1$ to $B_n$ , $E_2$ to $A_n$	2.0 2.0	4.5 4.5	6.0 6.0	1.5 2.0	7.5 8.5	1.5 2.0	7.0 7.0		

Notes: 1. Absolute maximum ratings and values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.  
2. Either voltage limit or current limit is sufficient to protect inputs.  
3. ESD Last Passing Voltage (Min) 4000V  
4. In LOW State (Max) twice the rated  $I_{OL}$  (mA)  
5. Current Applied to Output

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	$V_{CC}$	Conditions
		Min	Typ	Max			
$V_{IH}$	Input HIGH Voltage	2.0			V		Recognized as a HIGH signal
$V_{IL}$	Input LOW Voltage	0.8			V		Recognized as a LOW signal
$V_{OC}$	Input Clamp Diode Voltage	-1.2			V	Min	$I_{IN} = -18\text{mA}$
$V_{OH}$	Output HIGH Voltage	2.4 2.0 2.4 2.0 2.7			V	Min	$I_{OH} = -3\text{mA}$ ( $A_n$ , $B_n$ ) $I_{OH} = -12\text{mA}$ ( $A_n$ , $B_n$ ) $I_{OH} = -3\text{mA}$ ( $A_n$ , $B_n$ ) $I_{OH} = -12\text{mA}$ ( $A_n$ , $B_n$ ) $I_{OH} = -3\text{mA}$ ( $A_n$ , $B_n$ )
$V_{OL}$	Output LOW Voltage	0.25 0.25			V	Min	$I_{OL} = 48\text{mA}$ ( $A_n$ , $B_n$ ) $I_{OL} = 84\text{mA}$ ( $A_n$ , $B_n$ )
$I_{IH}$	Input HIGH Current	24F 24F			$\mu\text{A}$	Max	$V_{IN} = 2.7\text{V}$
$I_{HVT}$	Input HIGH Current Breakdown Test	24F 24F			$\mu\text{A}$	Max	$V_{IN} = 7.0\text{V}$ ( $E_1$ , $E_2$ )
$I_{LVT}$	Input LOW Current Breakdown Test	24F 24F			mA	Max	$V_{IN} = 0.5\text{V}$ ( $A_n$ , $B_n$ )
$I_{OZH}$	Output HIGH Leakage Current	24F 24F			$\mu\text{A}$	Max	$V_{OUT} = V_{CC}$
$V_{IO}$	Input Leakage Test	24F	4.75		V	0.0	$I_{IO} = 1.0\text{mA}$ All Other Pins Grounded
$I_{OD}$	Output Leakage Current	24F	3.75		$\mu\text{A}$	0.0	$V_{OD} = 150\text{mV}$ All Other Pins Grounded
$I_{IL}$	Input LOW Current	-1.0			mA	Max	$V_{IN} = 0.5\text{V}$ ( $E_1$ , $E_2$ )
$I_{IH} + I_{OZH}$	Output Leakage Current	70			$\mu\text{A}$	Max	$V_{OUT} = 2.7\text{V}$ ( $A_n$ , $B_n$ )
$I_{IL} + I_{OLZ}$	Output Leakage Current	-1.8			mA	Max	$V_{OUT} = 0.5\text{V}$ ( $A_n$ , $B_n$ )
$I_{OS}$	Output Short-Circuit Current	-255			mA	Max	$V_{OUT} = 0\text{V}$ ( $A_n$ , $B_n$ )
$I_{OCH}$	Power Supply Current	84	80		mA	Max	$V_{CC} = \text{HIGH}$
$I_{OCL}$	Power Supply Current	84	80		mA	Max	$V_{CC} = \text{LOW}$
$I_{OCS}$	Power Supply Current	71	80		mA	Max	$V_{CC} = \text{HIGH}$



## 54F/74F245

# Octal Bidirectional Transceiver with TRI-STATE® Outputs

### General Description

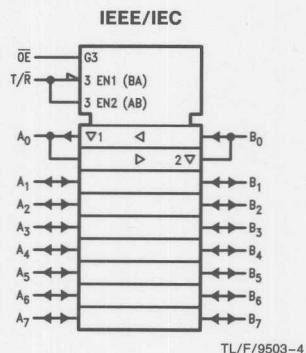
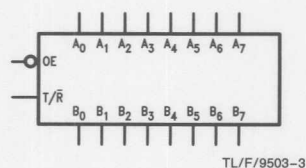
The 'F245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 24 mA (20 mA Mil) at the A ports and 64 mA (48 mA Mil) at the B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a High Z condition.

### Features

- Non-inverting buffers
- Bidirectional data path
- A outputs sink 24 mA (20 mA Mil)
- B outputs sink 64 mA (48 mA Mil)
- Guaranteed 4000V minimum ESD protection

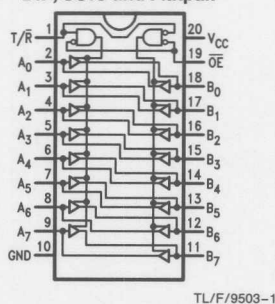
**Ordering Code:** See Section 5

### Logic Symbols

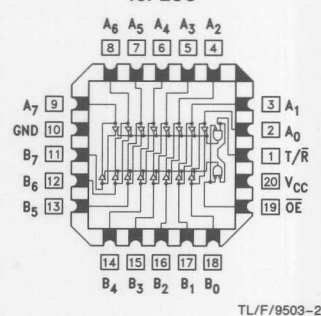


### Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak



Pin Assignment  
for LCC



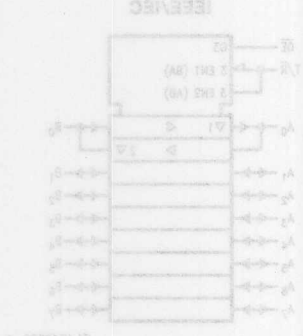
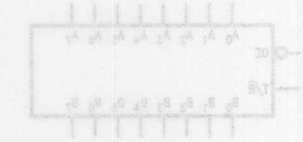
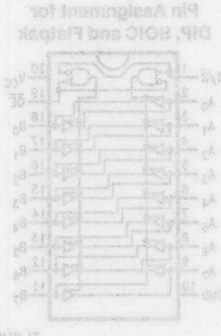
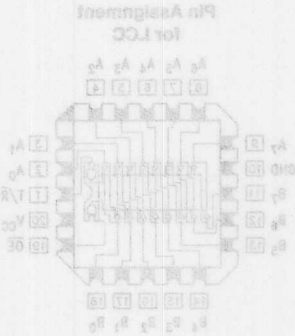
**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/2.0	20 $\mu$ A/ - 1.2 mA
$T/\overline{R}$	Transmit/Receive Input	1.0/2.0	20 $\mu$ A/ - 1.2 mA
$A_0-A_7$	Side A Inputs or TRI-STATE Outputs	3.5/1.083	70 $\mu$ A/ - 0.65 mA
$B_0-B_7$	Side B Inputs or TRI-STATE Outputs	150/40(38.3) 3.5/1.083 600/106.6(80)	- 3 mA/24 mA (20 mA) 70 $\mu$ A/ - 0.65 mA - 12 mA/64 mA (48 mA)

**Truth Table**

Inputs		Output
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial



**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	–0.5V to V <sub>CC</sub>
TRI-STATE Output	–0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

ESD Last Passing Voltage (Min) 4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	–55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage	0.8			V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage	–1.2			V	Min	I <sub>IN</sub> = –18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.4		V	Min	I <sub>OH</sub> = –3 mA (A <sub>n</sub> )
		54F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = –12 mA (B <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = –3 mA (A <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = –15 mA (B <sub>n</sub> )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = –3 mA (A <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA (A <sub>n</sub> )
		54F 10% V <sub>CC</sub>		0.55			I <sub>OL</sub> = 48 mA (B <sub>n</sub> )
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA (A <sub>n</sub> )
		74F 10% V <sub>CC</sub>		0.55			I <sub>OL</sub> = 64 mA (B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V (OE, T/Ē)
		74F		7.0			
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)	54F		1.0	mA	Max	V <sub>IN</sub> = 5.5 V (A <sub>n</sub> , B <sub>n</sub> )
		74F		0.5			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub> (A <sub>n</sub> , B <sub>n</sub> )
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			–1.2	mA	Max	V <sub>IN</sub> = 0.5V (T/Ē, OE)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			–650	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )



# DC Electrical Characteristics (Continued)

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
I <sub>OS</sub>	Output Short-Circuit Current	-60 -100		-150 -225	mA	Max	V <sub>OUT</sub> = 0V (A <sub>n</sub> ) V <sub>OUT</sub> = 0V (B <sub>n</sub> )
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V(A <sub>n</sub> , B <sub>n</sub> )
I <sub>CCH</sub>	Power Supply Current		70	90	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		95	120	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		85	110	mA	Max	V <sub>O</sub> = HIGH Z

## AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	2.5	4.2	6.0	2.0	7.5	2.0	7.0	ns	2-3
t <sub>PHL</sub>	A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	2.5	4.2	6.0	2.0	7.5	2.0	7.0		
t <sub>PZH</sub>	Output Enable Time	3.0	5.3	7.0	2.5	9.0	2.5	8.0	ns	2-5
t <sub>PZL</sub>		3.5	6.0	8.0	3.0	10.0	3.0	9.0		
t <sub>PHZ</sub>	Output Disable Time	2.0	5.0	6.5	2.0	9.0	2.0	7.5		
t <sub>PLZ</sub>		2.0	5.0	6.5	2.0	10.0	2.0	7.5		



54F/74F251A

## 8-Input Multiplexer with TRI-STATE® Outputs

### General Description

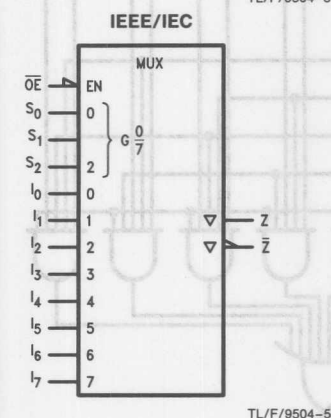
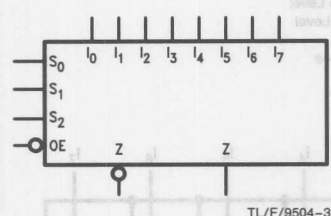
The 'F251A is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

### Features

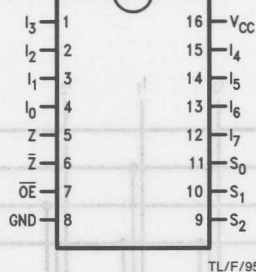
- Multifunctional capability
- On-chip select logic decoding
- Inverting and non-inverting TRI-STATE outputs

**Ordering Code:** See Section 5

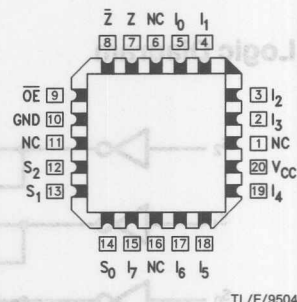
### Logic Symbols



Pin Assignment for  
DIP, SOIC and Flatpak



Pin Assignment  
for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$S_0-S_2$	Select Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$I_0-I_7$	Multiplexer Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
Z	TRI-STATE Multiplexer Output	150/40 (33.3)	-3 mA/24 mA (20 mA)
$\overline{Z}$	Complementary TRI-STATE Multiplexer Output	150/40 (33.3)	-3 mA/24 mA (20 mA)

## Functional Description

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs,  $S_0$ ,  $S_1$ ,  $S_2$ . Both assertion and negation outputs are provided. The Output Enable input ( $\overline{OE}$ ) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE} \cdot (I_0 \cdot \overline{S_0} \cdot \overline{S_1} \cdot \overline{S_2} + I_1 \cdot \overline{S_0} \cdot \overline{S_1} \cdot S_2 + I_2 \cdot \overline{S_0} \cdot S_1 \cdot \overline{S_2} + I_3 \cdot \overline{S_0} \cdot S_1 \cdot S_2 + I_4 \cdot S_0 \cdot \overline{S_1} \cdot \overline{S_2} + I_5 \cdot S_0 \cdot \overline{S_1} \cdot S_2 + I_6 \cdot S_0 \cdot S_1 \cdot \overline{S_2} + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

When the Output Enable is HIGH, both outputs are in the high impedance (High Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the

maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

## Truth Table

Inputs				Outputs	
$\overline{OE}$	$S_2$	$S_1$	$S_0$	$\overline{Z}$	$Z$
H	X	X	X	Z	Z
L	L	L	L	$\overline{I_0}$	$I_0$
L	L	L	H	$\overline{I_1}$	$I_1$
L	L	H	L	$\overline{I_2}$	$I_2$
L	L	H	H	$\overline{I_3}$	$I_3$
L	H	L	L	$\overline{I_4}$	$I_4$
L	H	L	H	$\overline{I_5}$	$I_5$
L	H	H	L	$\overline{I_6}$	$I_6$
L	H	H	H	$\overline{I_7}$	$I_7$

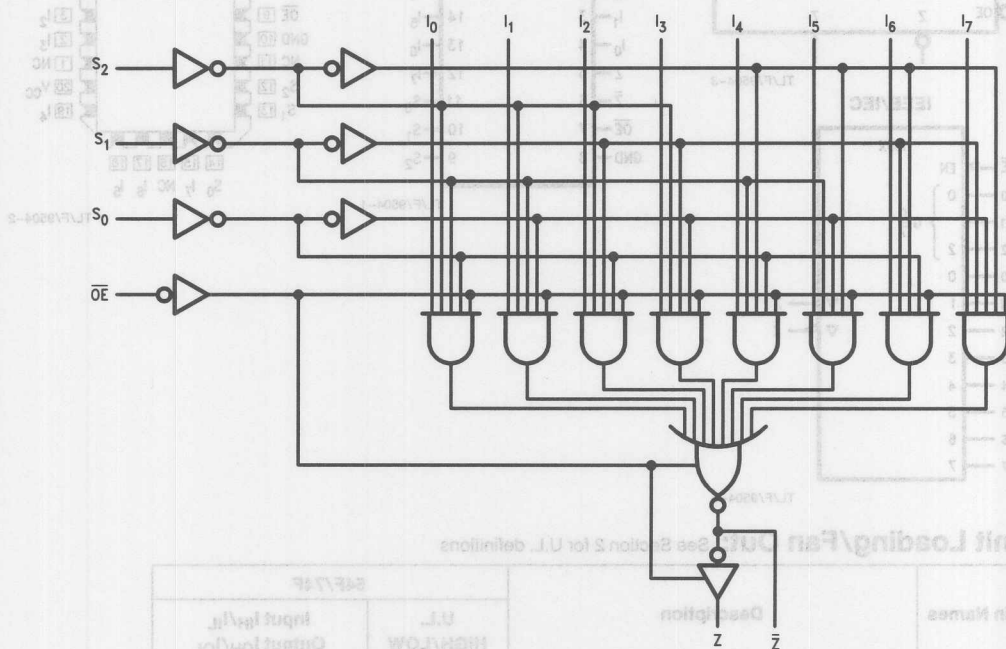
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

TL/F/9504-4

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military

−55°C to +125°C

Commercial

0°C to +70°C

Supply Voltage

Military

+4.5V to +5.5V

Commercial

+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CC1</sub>	Power Supply Current		15	22	mA	Max	V <sub>O</sub> = LOW
I <sub>CC2</sub>	Power Supply Current		16	24	mA	Max	V <sub>O</sub> = HIGH Z





## 54F/74F253

### Dual 4-Input Multiplexer with TRI-STATE® Outputs

#### General Description

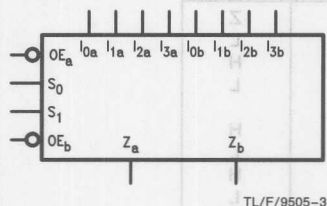
The 'F253 is a dual 4-input multiplexer with TRI-STATE® outputs. It can select two bits of data from four sources using common select inputs. The output may be individually switched to a high impedance state with a HIGH on the respective Output Enable (OE) inputs, allowing the outputs to interface directly with bus oriented systems.

#### Features

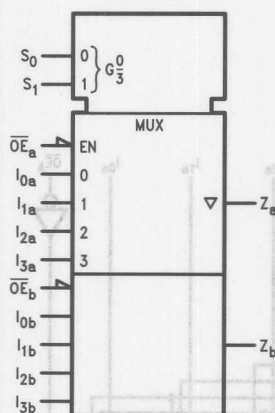
- Multifunction capability
- Non-inverting TRI-STATE outputs
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

#### Logic Symbols

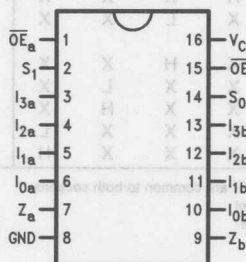


IEEE/IEC

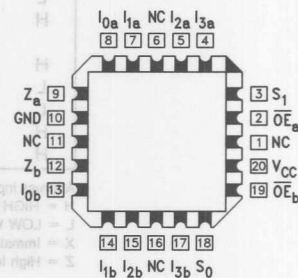


#### Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



Pin Assignment for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$I_{0a}-I_{3a}$	Side A Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$I_{0b}-I_{3b}$	Side B Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$S_0-S_1$	Common Select Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$OE_a$	Side A Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$OE_b$	Side B Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$Z_a, Z_b$	TRI-STATE Outputs	150/40(33.3)	-3 mA/24 mA (20 mA)



## Functional Description

This device contains two identical 4-input multiplexers with TRI-STATE outputs. They select two bits from four sources selected by common Select inputs ( $S_0, S_1$ ). The 4-input multiplexers have individual Output Enable ( $\overline{OE}_a, \overline{OE}_b$ ) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so that there is no overlap.

## Truth Table

Select Inputs		Data Inputs				Output Enable	Output
$S_0$	$S_1$	$I_0$	$I_1$	$I_2$	$I_3$	$\overline{OE}$	$Z$
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs  $S_0$  and  $S_1$  are common to both sections.

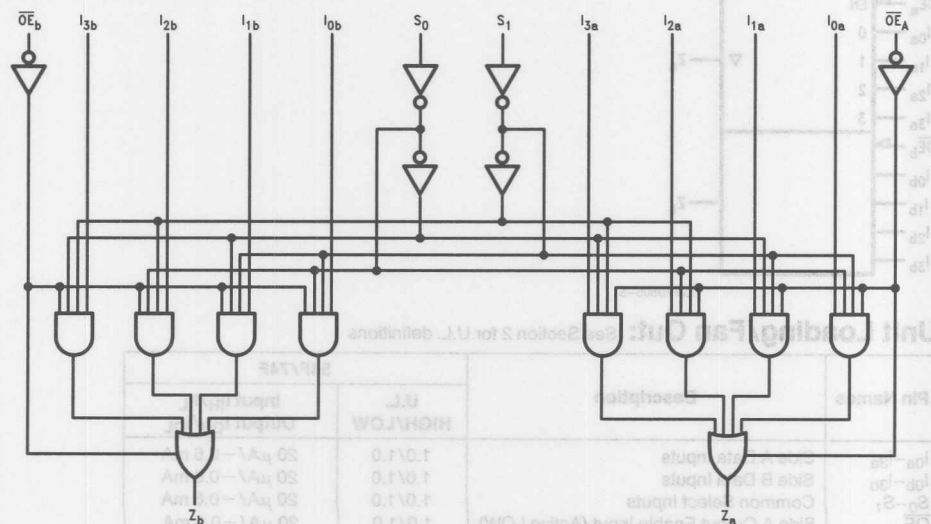
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

TL/F/9505-4

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	–0.5V to V <sub>CC</sub>
Standard Output	–0.5V to +5.5V
TRI-STATE Output	–0.5V to +5.5V

Current Applied to Output in LOW State (Max)

twice the rated I<sub>OL</sub> (mA)

ESD Last Passing Voltage (Min)

4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military

–55°C to +125°C

Commercial

0°C to +70°C

Supply Voltage

Military

+4.5V to +5.5V

Commercial

+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				–1.2	V	Min	I <sub>IN</sub> = –18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5			V	Min	I <sub>OH</sub> = –1 mA
		54F 10% V <sub>CC</sub>	2.4					I <sub>OH</sub> = –3 mA
		74F 10% V <sub>CC</sub>	2.5					I <sub>OH</sub> = –1 mA
		74F 10% V <sub>CC</sub>	2.4					I <sub>OH</sub> = –3 mA
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = –1 mA
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = –3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>			0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>			0.5			I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F			20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F			5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F			100	μA	Max	V <sub>IN</sub> = 7.0V
		74F			7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F			50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current				–0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current				50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current				–50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		–60		–150	mA	Max	V <sub>OUT</sub> = 0V
			–100		–225			V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test				500	μA	0.0V	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>CCH</sub>	Power Supply Current			11.5	16	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			16	23	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current			16	23	mA	Max	V <sub>O</sub> = HIGH Z

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$			54F $T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{pF}$		74F $T_A, V_{CC} = \text{Com}$ $C_L = 50\text{pF}$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_n$ to $Z_n$	4.5 3.0	8.5 6.5	11.5 9.0	3.5 2.5	15.0 11.0	4.5 3.0	13.0 10.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $I_n$ to $Z_n$	3.0 2.5	5.5 4.5	7.0 6.0	2.5 2.5	9.0 8.0	3.0 2.5	8.0 7.0	ns	2-3
$t_{PZH}$ $t_{PZL}$	Output Enable Time	3.0 3.0	6.0 6.0	8.0 8.0	2.5 2.5	10.0 10.0	3.0 3.0	9.0 9.0	ns	2-5
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time	2.0 2.0	3.7 4.4	5.0 6.0	2.0 2.0	6.5 8.0	2.0 2.0	6.0 7.0		

Symbol	Parameter	74F/54F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
$V_{IH}$	Input HIGH Voltage	2.0			V		Recognized as a HIGH signal
$V_{IL}$	Input LOW Voltage	0.8			V		Recognized as a LOW signal
$V_{OD}$	Input Clamp Diode Voltage	-1.2			V		$I_{IK} = -18\text{mA}$
$V_{OH}$	Output HIGH Voltage	2.7			V	Min	$I_{OH} = -3\text{mA}$
		2.4					$I_{OH} = -3\text{mA}$
		2.4					$I_{OH} = -1\text{mA}$
		2.4					$I_{OH} = -3\text{mA}$
		2.7					$I_{OH} = -1\text{mA}$
		2.7					$I_{OH} = -3\text{mA}$
$V_{OL}$	Output LOW Voltage	0.2			V	Min	$I_{OL} = 20\text{mA}$
		0.2					$I_{OL} = 24\text{mA}$
$I_{IH}$	Input HIGH Current	24			$\mu\text{A}$	Max	$V_{IH} = 2.7\text{V}$
		24					$V_{IH} = 2.0\text{V}$
$I_{IN}$	Input HIGH Current Breakdown Test	100			$\mu\text{A}$	Max	
		7.0					
$I_{OCH}$	Output HIGH Leakage Current	24			$\mu\text{A}$	Max	$V_{OUT} = V_{CC}$
		24					
$I_{IO}$	Input Leakage Test	4.75			V	0.0	$I_{IP} = 1.9\text{pA}$ All Other Pins Grounded
$I_{OO}$	Output Leakage Current	24			$\mu\text{A}$	0.0	$V_{IO} = 150\text{mV}$ All Other Pins Grounded
$I_{IL}$	Input LOW Current	-0.8			mA	Max	$V_{IH} = 0.8\text{V}$
$I_{OSH}$	Output Leakage Current	80			$\mu\text{A}$	Max	$V_{OUT} = 2.7\text{V}$
$I_{OCL}$	Output Leakage Current	-80			$\mu\text{A}$	Max	$V_{OUT} = 0.8\text{V}$
$I_{OE}$	Output Short-Circuit Current	-100			mA	Max	$V_{OUT} = 0\text{V}$
		-150					$V_{OUT} = 0\text{V}$
$I_{ZZ}$	Bus Drainage Test	200			$\mu\text{A}$	0.0V	$V_{OUT} = V_{CC}$
$I_{OCH}$	Power Supply Current	11.8			mA	Max	$V_{O} = \text{HIGH}$
$I_{OCL}$	Power Supply Current	18			mA	Max	$V_{O} = \text{LOW}$
$I_{OCC}$	Power Supply Current	18			mA	Max	$V_{O} = \text{HIGH } Z$



## 54F/74F257A

### Quad 2-Input Multiplexer with TRI-STATE® Outputs

#### General Description

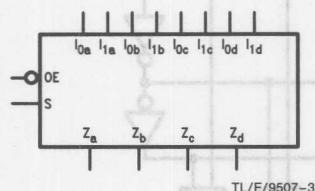
The 'F257A is a quad 2-input multiplexer with TRI-STATE outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ( $\overline{OE}$ ) input, allowing the outputs to interface directly with bus-oriented systems.

#### Features

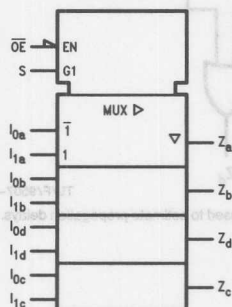
- Multiplexer expansion by tying outputs together
- Non-inverting TRI-STATE outputs
- Input clamp diodes limit high-speed termination effects
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

#### Logic Symbols

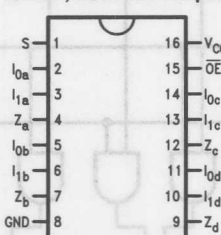


IEEE/IEC

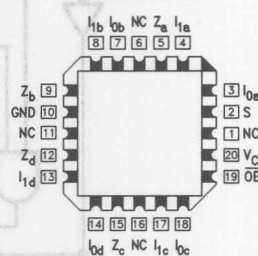


#### Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



Pin Assignment for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
S	Common Data Select Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$I_{0a}-I_{0d}$	Data Inputs from Source 0	1.0/1.0	20 $\mu$ A/ -0.6 mA
$I_{1a}-I_{1d}$	Data Inputs from Source 1	1.0/1.0	20 $\mu$ A/ -0.6 mA
$Z_a-Z_d$	TRI-STATE Multiplexer Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

## Functional Description

The 'F257A is a quad 2-input multiplexer with TRI-STATE outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the  $I_{0x}$  inputs are selected and when Select is HIGH, the  $I_{1x}$  inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equation for the outputs is shown below:

$$Z_n = \overline{OE} \cdot (I_n \cdot S + I_{on} \cdot \bar{S})$$

When the Output Enable input ( $\overline{OE}$ ) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so there is no overlap.

## Truth Table

Output Enable	Select Input	Data Inputs		Output
$\overline{OE}$	S	$I_0$	$I_1$	Z
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

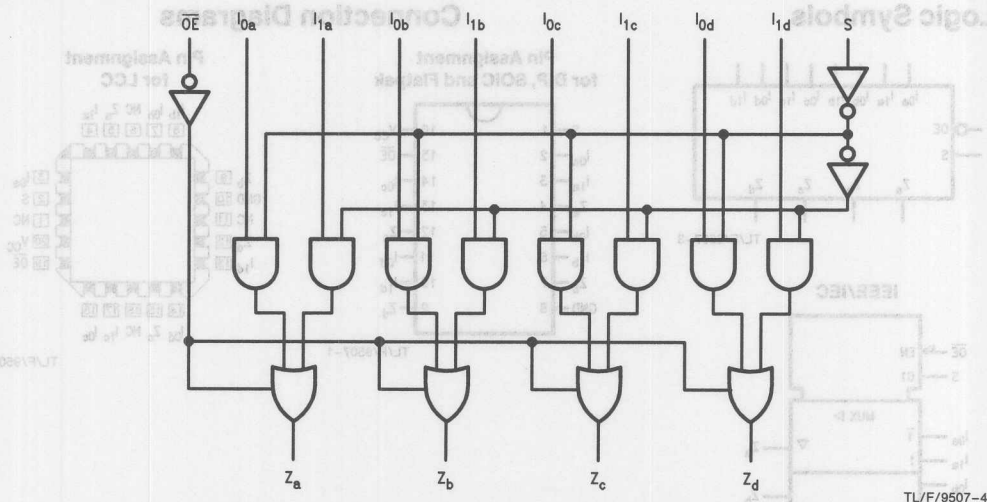
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Unit Loading/Fan Out: See Section 2 for U.I. definitions

Pin Number	Description	U.I.	Input/Output
2	Common Data Select Input	10/1.0	Input
OE	TRI-STATE Output Enable Input (Active LOW)	10/1.0	Input
10a-10d	Data Inputs from Source 0	10/1.0	Input
11a-11d	Data Inputs from Source 1	10/1.0	Input
20-23	TRI-STATE Multiplexer Outputs	10/1.0 (20-23)	Output

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
---	----------------

Input Voltage (Note 2)	−0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	−30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output	−0.5V to +5.5V
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

ESD Last Passing Voltage (Min)	4000V
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**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current		9.0	15	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		14.5	22	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		15	23	mA	Max	V <sub>O</sub> = HIGH Z



# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	2.5	4.5	5.5	2.0	7.0	2.0	6.0	ns	2-3
$t_{PHL}$	$I_n$ to $Z_n$	2.0	4.2	5.5	1.5	7.0	2.0	6.0		
$t_{PLH}$	Propagation Delay	4.0	5.0	9.5	3.5	11.5	3.5	10.5	ns	2-3
$t_{PHL}$	S to $Z_n$	2.5	6.5	7.0	2.5	9.0	2.5	8.0		
$t_{PZH}$	Output Enable Time	2.0	5.9	6.0	2.0	8.0	2.0	7.0	ns	2-5
$t_{PZL}$		2.5	5.5	7.0	2.5	9.0	2.5	8.0		
$t_{PHZ}$	Output Disable Time	2.0	4.3	6.0	2.0	7.0	2.0	7.0		
$t_{PLZ}$		2.0	4.5	6.0	2.0	8.5	2.0	7.0		

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect input.

ESD: Electrostatic Discharge (Min)

## DC Electrical Characteristics

Symbol	Parameter	74F			Units	$V_{CC}$	Conditions
		Min	Typ	Max			
$V_{IH}$	Input HIGH Voltage	2.0			V		Recognized as a HIGH signal
$V_{IL}$	Input LOW Voltage	0.8			V		Recognized as a LOW signal
$V_{CD}$	Input Clamp Diode Voltage	-1.2			V	Min	$I_{IN} = -18\text{mA}$
$V_{OH}$	Output HIGH Voltage	2.7	2.4	2.2	V	Min	$I_{OH} = -3\text{mA}$ $I_{OH} = -1\text{mA}$ $I_{OH} = -3\text{mA}$ $I_{OH} = -1\text{mA}$ $I_{OH} = -3\text{mA}$ $I_{OH} = -1\text{mA}$ $I_{OH} = -3\text{mA}$
$V_{OL}$	Output LOW Voltage	0.5	0.5	0.5	V	Min	$I_{OL} = 20\text{mA}$ $I_{OL} = 24\text{mA}$
$I_{IH}$	Input HIGH Current	24F	20.0	2.0	$\mu\text{A}$	Max	$V_{IN} = 2.7\text{V}$
$I_{BI}$	Input HIGH Current Breakdown Test	24F	100	7.0	$\mu\text{A}$	Max	$V_{IN} = 7.0\text{V}$
$I_{OX}$	Output HIGH Leakage Current	24F	280	20	$\mu\text{A}$	Max	$V_{OUT} = V_{CC}$
$V_{IO}$	Input Leakage Test	24F	4.75		V	0.0	$I_{IP} = 1.8\text{mA}$ All Other Pins Grounded
$I_{OP}$	Output Leakage Current	24F	3.75		$\mu\text{A}$	0.0	$V_{OP} = 180\text{mV}$ All Other Pins Grounded
$I_{IL}$	Input LOW Current		-0.8		mA	Max	$V_{IN} = 0.2\text{V}$
$I_{OZH}$	Output Leakage Current		20		$\mu\text{A}$	Max	$V_{OUT} = 2.7\text{V}$
$I_{OZL}$	Output Leakage Current		-20		$\mu\text{A}$	Max	$V_{OUT} = 0.2\text{V}$
$I_{OS}$	Output Short-Circuit Current	-60	-120		mA	Max	$V_{OUT} = 0\text{V}$
$I_{ZS}$	Bus Drainage Test		500		$\mu\text{A}$	0.0V	$V_{OUT} = 2.2\text{V}$
$I_{OCH}$	Power Supply Current	0.0	12		mA	Max	$V_O = \text{HIGH}$
$I_{OCL}$	Power Supply Current	14.5	22		mA	Max	$V_O = \text{LOW}$
$I_{OCS}$	Power Supply Current	12	23		mA	Max	$V_O = \text{HIGH } \Sigma$



**54F/74F258A**

## Quad 2-Input Multiplexer with TRI-STATE® Outputs

### General Description

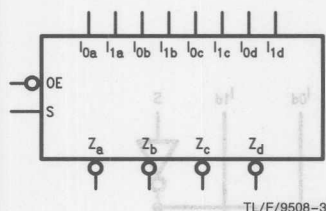
The 'F258A is a quad 2-input multiplexer with TRI-STATE outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ( $\overline{OE}$ ) input, allowing the outputs to interface directly with bus-oriented systems.

### Features

- Multiplexer expansion by tying outputs together
- Inverting TRI-STATE outputs
- Guaranteed 4000V minimum ESD protection

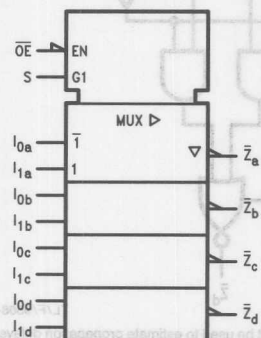
**Ordering Code:** See Section 5

### Logic Symbols



TL/F/9508-3

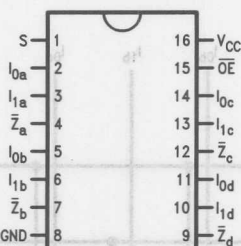
IEEE/IEC



TL/F/9508-5

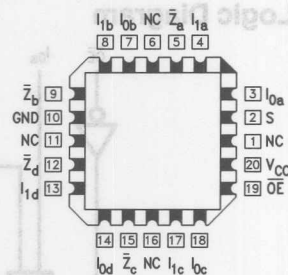
### Connection Diagrams

**Pin Assignment for DIP, SOIC and Flatpak**



TL/F/9508-1

**Pin Assignment for LCC**



TL/F/9508-2

**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
S	Common Data Select Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$I_{0a}-I_{0d}$	Data Inputs from Source 0	1.0/1.0	20 $\mu$ A/ -0.6 mA
$I_{1a}-I_{1d}$	Data Inputs from Source 1	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{Za}-\overline{Zd}$	TRI-STATE Inverting Data Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

## Functional Description

The 'F258A is a quad 2-input multiplexer with TRI-STATE outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the  $I_{0x}$  inputs are selected and when Select is HIGH, the  $I_{1x}$  inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The 'F258A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equation for the outputs is shown below:

$$\bar{Z}_n = \bar{OE} \cdot (I_{1n} \cdot S + I_{0n} \cdot \bar{S})$$

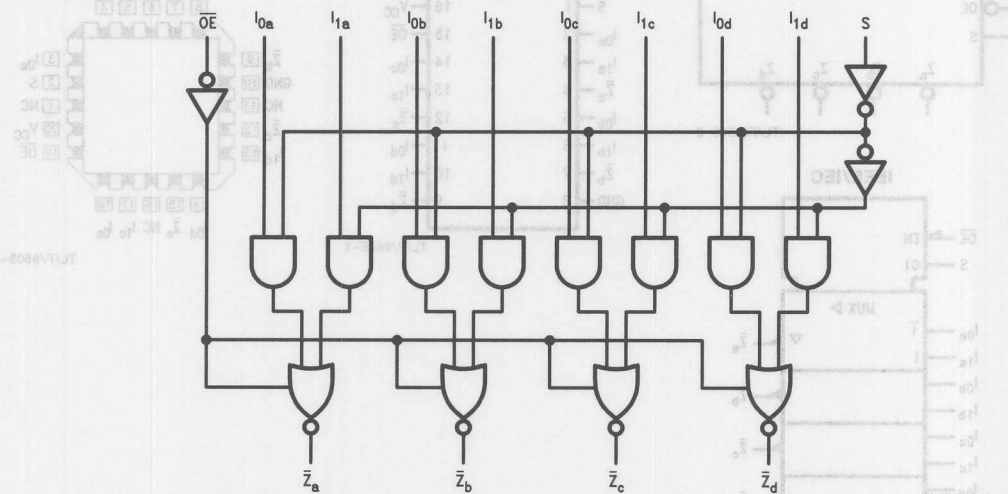
When the Output Enable input ( $\bar{OE}$ ) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs of the TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so there is no overlap.

## Truth Table

Output Enable	Select Input	Data Inputs		Output
$\bar{OE}$	S	$I_0$	$I_1$	$\bar{Z}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

## Logic Diagram



TL/F/9508-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Pin Name	Description	U.L.	
		HIGH/LOW	Input/Output
S	Common Data Select Input	1.0V/0	Input
$\bar{OE}$	TRI-STATE Output Enable Input (Active LOW)	1.0V/0	Input
$I_{0a}$	Data Input from Source 0	1.0V/0	Input
$I_{1a}$	Data Input from Source 1	1.0V/0	Input
$I_{0b}$	TRI-STATE Inverting Data Output	1.0V/0	Output
$I_{1b}$		1.0V/0	Output
$I_{0c}$		1.0V/0	Output
$I_{1c}$		1.0V/0	Output
$I_{0d}$		1.0V/0	Output
$I_{1d}$		1.0V/0	Output

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
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Input Voltage (Note 2)	–0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	–30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	–0.5V to V <sub>CC</sub>
Standard Output	–0.5V to +5.5V
TRI-STATE Output	–0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
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ESD Last Passing Voltage (Min)	4000V
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**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	–55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			–1.2	V	Min	I <sub>IN</sub> = –18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	I <sub>OH</sub> = –1 mA I <sub>OH</sub> = –3 mA I <sub>OH</sub> = –1 mA I <sub>OH</sub> = –3 mA I <sub>OH</sub> = –1 mA I <sub>OH</sub> = –3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			–0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			–50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		–60	–150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>CCH</sub>	Power Supply Current		6.2	9.5	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		15.1	23	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		11.3	17	mA	Max	V <sub>O</sub> = HIGH Z





## 54F/74F269 8-Bit Bidirectional Binary Counter

### General Description

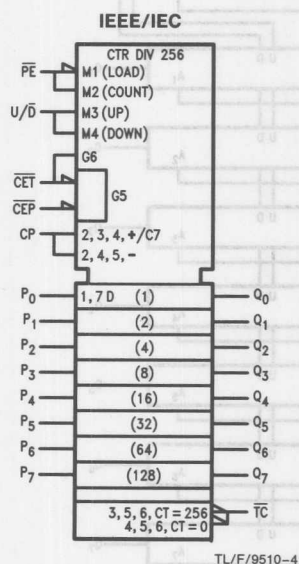
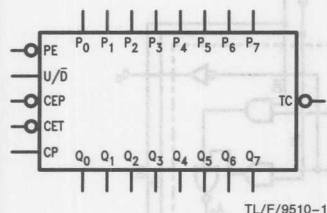
The 'F269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/D input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

### Features

- Synchronous counting and loading
- Built-in lookahead carry capability
- Count frequency 100 MHz
- Supply current 113 mA typ
- 300 mil slimline package

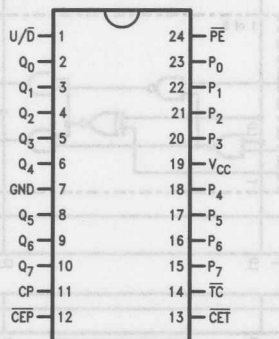
**Ordering Code:** See Section 5

### Logic Symbols

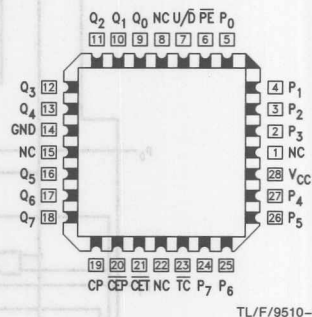


### Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak



Pin Assignment  
for LCC



Function Table

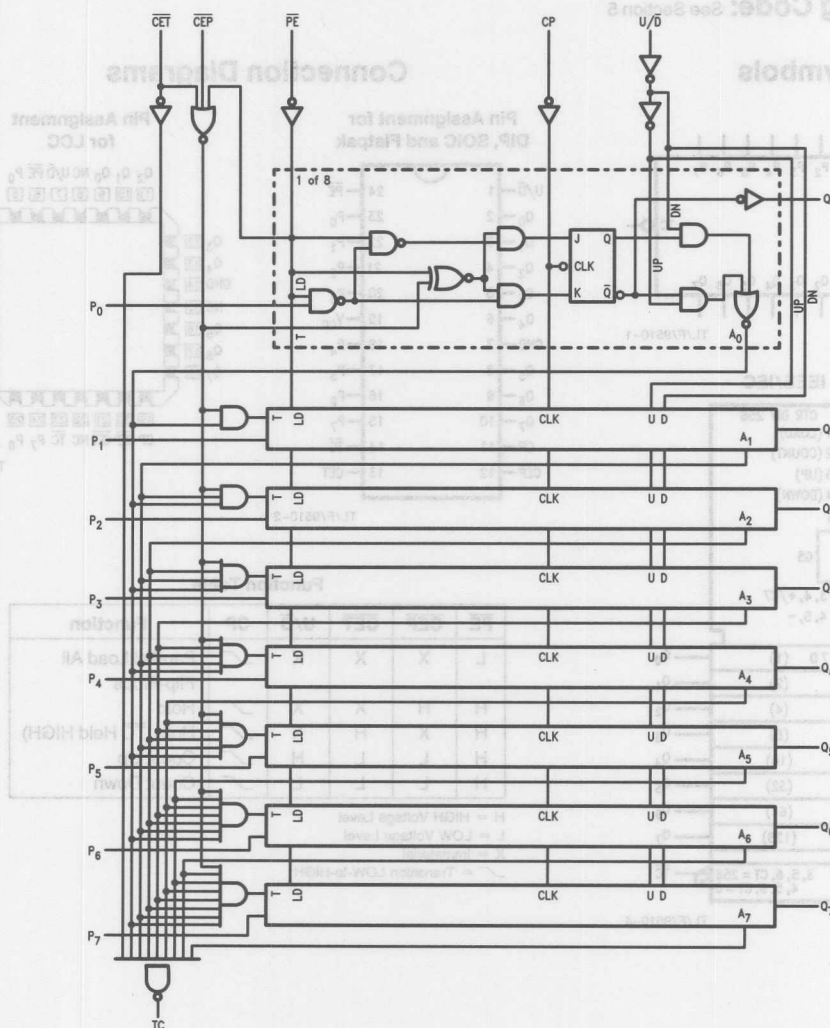
PE	CEP	CET	U/D	CP	Function
L	X	X	X	—	Parallel Load All Flip-Flops
H	H	X	X	—	Hold
H	X	H	X	—	Hold (TC Held HIGH)
H	L	L	H	—	Count Up
H	L	L	L	—	Count Down

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
— = Transition LOW-to-HIGH



**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$P_0-P_7$	Parallel Data Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$U/\overline{D}$	Up-Down Count Control Input	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
CP	Clock Input	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{TC}$	Terminal Count Output (Active LOW)	5.0/33.3	-1 mA / 20 mA
$Q_0-Q_7$	Flip-Flop Outputs	50/33.3	-1 mA / 20 mA

**Logic Diagram**


TL/F/9510-6

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	– 65°C to + 150°C
Ambient Temperature under Bias	– 55°C to + 125°C
Junction Temperature under Bias	– 55°C to + 175°C

V <sub>CC</sub> Pin Potential to Ground Pin	– 0.5V to + 7.0V
Input Voltage (Note 2)	– 0.5V to + 7.0V
Input Current (Note 2)	– 30 mA to + 5.0 mA

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	– 0.5V to V <sub>CC</sub>
TRI-STATE® Output	– 0.5V to + 5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	– 55°C to + 125°C
Commercial	0°C to + 70°C

Supply Voltage

Military	+ 4.5V to + 5.5V
Commercial	+ 4.5V to + 5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			– 1.2	V	Min	I <sub>IN</sub> = – 18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = – 1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = – 1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = – 1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA, All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			– 0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		– 60	– 150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		104	125	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		113	135	mA	Max	V <sub>O</sub> = LOW

# **AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	100					85		MHz	2-1
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $Q_n$ (Count-Up)	3.5 4.5		8.0 10.5			3.5 4.5	9.0 11.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay $U/\bar{D}$ to $\bar{TC}$	3.5 4.5		9.5 9.5			3.5 4.5	10.0 11.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay $\bar{CET}$ to $\bar{TC}$	3.5 3.0		9.0 10.5			3.5 3.0	10.5 11.5	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $\bar{TC}$	4.5 5.0		10.0 10.0			4.5 4.5	10.5 10.5	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $Q_n$ (Count-Down)	3.5 4.5		10.5 10.5			3.5 4.5	11.0 11.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $Q_n$ (Load)	3.5 4.0		9.0 9.0			3.5 4.0	10.0 9.0	ns	2-3

# **AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW Data to CP	3.5 3.0				4.0 3.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW Data to CP	1.0 1.0				2.0 1.0			
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $\overline{\text{PE}}$ to CP	5.5 5.5				6.5 6.5		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $\overline{\text{PE}}$ to CP	0 0				0 0			
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $\overline{\text{CET}}$ or $\overline{\text{CEP}}$ to CP	6.0 8.0				6.5 9.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $\overline{\text{CET}}$ or $\overline{\text{CEP}}$ to CP	0 0				0 0			
$t_w(\text{H})$ $t_w(\text{L})$	Clock Pulse Width, HIGH or LOW	3.5 3.5				3.5 4.0		ns	2-4
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $\text{U}/\overline{\text{D}}$ to CP	8.0 6.0				9.5 7.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $\text{U}/\overline{\text{D}}$ to CP	0.0 0.0				0.0 0.0		ns	2-6

## 54F/74F273 Octal D Flip-Flop

### General Description

The 'F273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ( $\overline{MR}$ ) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

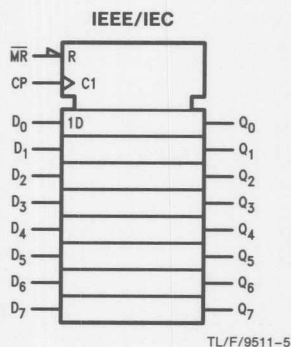
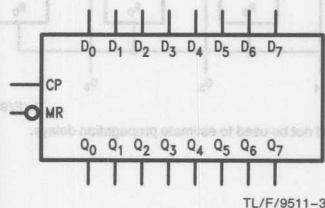
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the  $\overline{MR}$  input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

### Features

- Ideal buffer for MOS microprocessor or memory
- Eight edge-triggered D flip-flops
- Buffered common clock
- Buffered, asynchronous Master Reset
- See 'F377 for clock enable version
- See 'F373 for transparent latch version
- See 'F374 for TRI-STATE® version
- Guaranteed 4000V minimum ESD protection

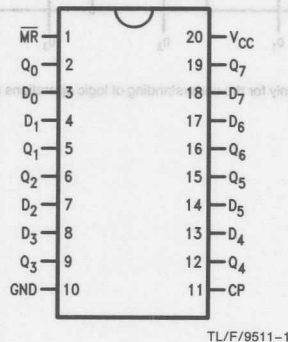
**Ordering Code:** See Section 5

### Logic Symbols

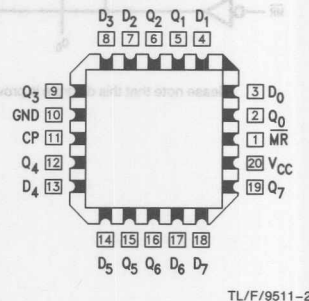


### Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak





Pin Assignment  
for LCC




# Unit Loading/Fan Out: See Section 2 for U.L. definitions

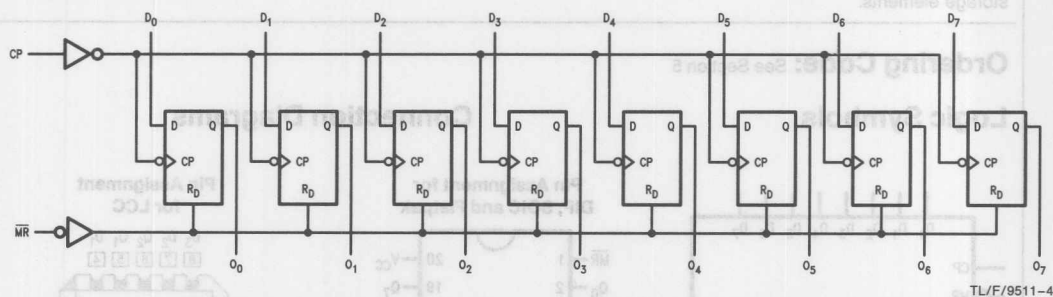
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$D_0-D_7$	Data Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{MR}$	Master Reset (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu A$ / -0.6 mA
$Q_0-Q_7$	Data Outputs	50/33.3	-1 mA/20 mA

Mode Select-Function Table


Operating Mode	Inputs			Output
	$\overline{MR}$	CP	$D_n$	$Q_n$
Reset (Clear)	L	X	X	L
Load '1'	H		h	H
Load '0'	H		l	L

H = HIGH Voltage Level steady state  
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition  
L = LOW Voltage Level steady state  
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition  
X = Immaterial  
 = LOW-to-HIGH clock transition

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Ambient Temperature under Bias		-55°C to +125°C		Commercial		0°C to +70°C			
Junction Temperature under Bias		-55°C to +175°C		Supply Voltage					
V <sub>CC</sub> Pin Potential to Ground Pin		-0.5V to +7.0V		Military		+4.5V to +5.5V			
Input Voltage (Note 2)		-0.5V to +7.0V		Commercial		+4.5V to +5.5V			
Input Current (Note 2)		-30 mA to +5.0 mA							
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)		-0.5V to V <sub>CC</sub>							
Standard Output TRI-STATE Output		-0.5V to +5.5V							
Current Applied to Output in LOW State (Max)		twice the rated I <sub>OL</sub> (mA)							
ESD Last Passing Voltage (min)		4000V							
<b>Note 1:</b> Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.									
<b>Note 2:</b> Either voltage limit or current limit is sufficient to protect inputs.									
<b>DC Electrical Characteristics</b>									
Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions	
			Min	Typ	Max				
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal	
V <sub>IL</sub>	Input LOW Voltage					0.8	V	Recognized as a LOW Signal	
V <sub>CD</sub>	Input Clamp Diode Voltage					-1.2	V	Min I <sub>IN</sub> = -18 mA	
V <sub>OH</sub>	Output HIGH Voltage	Mil	2.5			V	Min	I <sub>OH</sub> = -1 mA	
		10% V <sub>CC</sub>	2.5						
		5% V <sub>CC</sub>	2.7						
V <sub>OL</sub>	Output LOW Voltage	Mil				V	Min	I <sub>OL</sub> = 20 mA	
		10% V <sub>CC</sub>							
		5% V <sub>CC</sub>							
I <sub>IH</sub>	Input HIGH Current	54F	20.0			μA	Max	V <sub>IN</sub> = 2.7V	
		74F	5.0						
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F	100			μA	Max	V <sub>IN</sub> = 7.0V	
		74F	7.0						
I <sub>CEX</sub>	Output HIGH Leakage Current	54F	250			μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>	
		74F	50						
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All other pins grounded	
I <sub>OD</sub>	Output Leakage Circuit Current	74F	3.75			μA	0.0	V <sub>IOD</sub> = 150 mV All other pins grounded	
I <sub>IL</sub>	Input LOW Current		-0.6			mA	Max	V <sub>IN</sub> = 0.5V	
I <sub>OS</sub>	Output Short-Circuit Current		-60			-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		44			mA	Max	CP =  D <sub>n</sub> = MR = HIGH	
I <sub>CCL</sub>			56						



**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.	
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$				
		Min	Typ	Max	Min	Max	Min	Max			
$f_{\text{max}}$	Maximum Clock Frequency	160			9.5			130		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	3.0		7.0	2.5	9.5	2.5	7.5			
$t_{\text{PHL}}$	Clock to Output	4.0		9.00	3.0	11.0	3.5	9.0		ns	2-4
$t_{\text{PLH}}$	Propagation Delay	4.5		9.5	3.0	11.0	4.0	10.0		ns	
$t_{\text{PHL}}$	MR to Output										2-4

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	3.0		3.5		3.0		ns	2-6
$t_s(\text{L})$	Data to CP	3.5		4.0		3.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0.5		1.0		0.5			
$t_h(\text{L})$	Data to CP	1.0		1.0		1.0			
$t_w(\text{L})$	MR Pulse Width, LOW	6.0		4.0		6.0		ns	2-4
$t_w(\text{H})$	CP Pulse Width	6.0		5.0		6.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	6.0		5.0		6.0			
$t_{\text{rec}}$	Recovery Time, MR to CP	3.0		4.5		3.5		ns	2-4

# 54F/74F280 9-Bit Parity Generator/Checker

## General Description

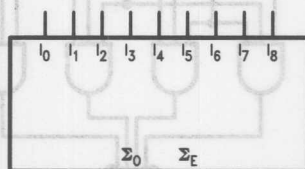
The 'F280 is a high-speed parity generator/checker that accepts nine bits of input data and detects whether an even or an odd number of these inputs is HIGH. If an even number of inputs is HIGH, the Sum Even output is HIGH. If an odd number is HIGH, the Sum Even output is LOW. The Sum Odd output is the complement of the Sum Even output.

## Features

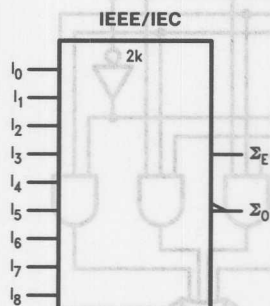
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

## Logic Symbols



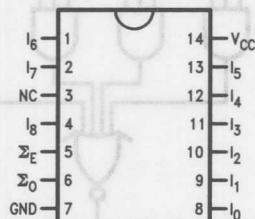
TL/F/9512-3



TL/F/9512-5

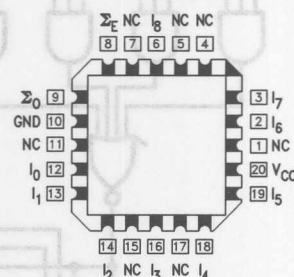
## Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9512-1

Pin Assignment for LCC



TL/F/9512-2

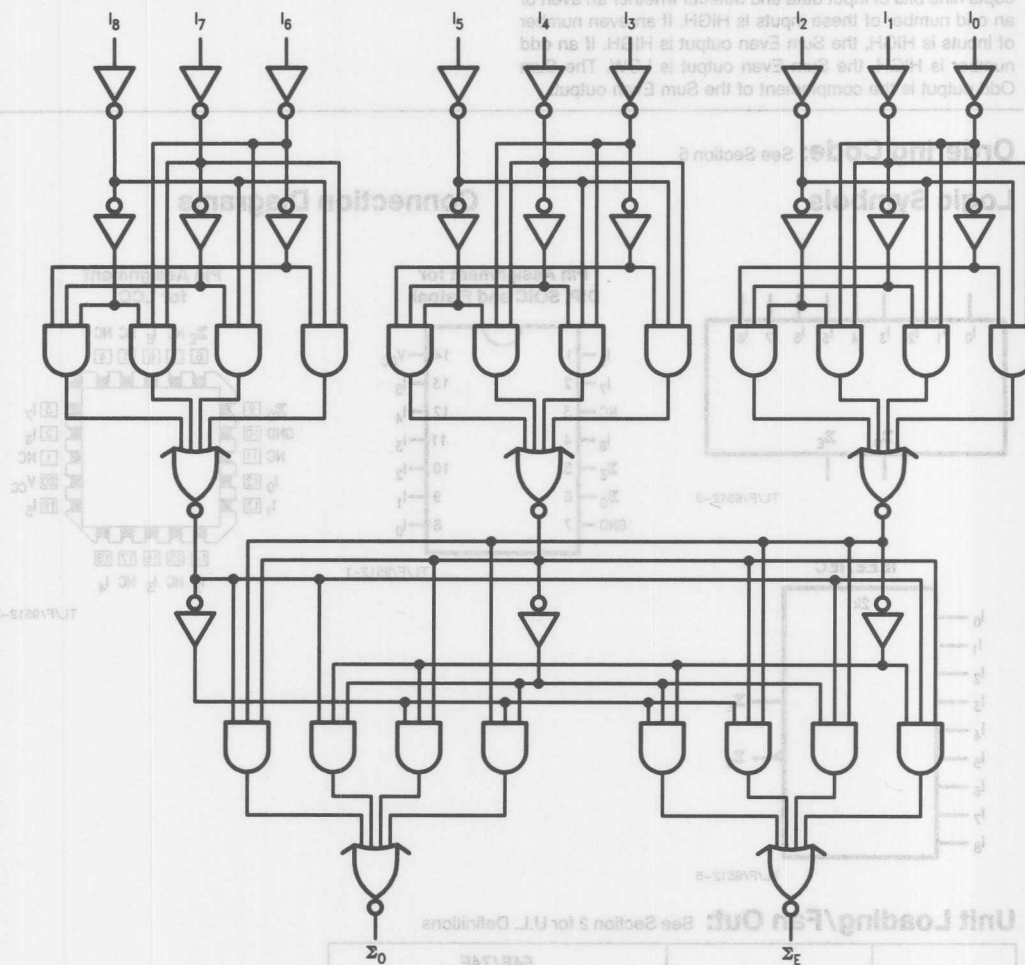
**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_H/I_L$ Output $O_H/O_L$
$I_0-I_8$	Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\Sigma_0$	Odd Parity Output	50/33.3	-1 mA/20 mA
$\Sigma_E$	Even Parity Output	50/33.3	-1 mA/20 mA

0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = HIGH Voltage Level  
L = LOW Voltage Level

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Symbol	Pin Name	Description	U.I.	SAF/74F
$\Sigma_0$	Even Parity Output	50V33.3	1.0/1.0	SAF/74F
$\Sigma_E$	Odd Parity Output	50V33.3	1.0/1.0	SAF/74F
$I_0$	Data Input	50V33.3	1.0/1.0	SAF/74F

TL/F/9512-4

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V

Input Current (Note 2)	−30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

ESD Last Passing Voltage (Min)	4000V
--------------------------------	-------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	−55°C to +125°C
Military	
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5			V	Min	I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.5					I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>			0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>			0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F			20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F			5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F			100	μA	Max	V <sub>IN</sub> = 7.0V
		74F			7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F			50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current				−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60		−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current			25	38	mA	Max	V <sub>O</sub> = HIGH

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	6.5	10.0	15.0	6.5	20.0	6.5	16.0	ns	2-3
$t_{PHL}$	$I_n$ to $\Sigma_E$	6.5	11.0	16.0	6.5	21.0	6.5	17.0		
$t_{PLH}$	Propagation Delay	6.0	10.0	15.0	6.0	20.0	6.0	16.0	ns	2-3
$t_{PHL}$	$I_n$ to $\Sigma_O$	6.5	11.0	16.0	6.5	21.0	6.5	17.0		

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Input voltage limit or current limit is sufficient to protect inputs.

Note 3: ESD Last Passing Voltage (Min) 4000V

Note 4: Current Applied to Output in LOW State (Max) twice the rated  $I_{OL}$  (mA)

Note 5: TRI-STATE<sup>®</sup> Output Standard Output -0.5V to  $V_{CC}$  in HIGH State (with  $V_{CC} = 0\text{V}$ )

## DC Electrical Characteristics

Symbol	Parameter	74F		Units	$V_{CC}$	Conditions
		Min	Typ			
$V_{IH}$	Input HIGH Voltage	2.0		V		Recognized as a HIGH Signal
$V_{IL}$	Input LOW Voltage	0.8		V		Recognized as a LOW Signal
$V_{OC}$	Input Clamp Diode Voltage	-1.5		V	Min	$I_{IN} = -18\text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.7	2.8	V	Min	$I_{OH} = -1\text{ mA}$ $I_{OH} = -1\text{ mA}$ $I_{OH} = -1\text{ mA}$
$V_{OL}$	Output LOW Voltage	0.2	0.2	V	Min	$I_{OL} = 20\text{ mA}$ $I_{OL} = 20\text{ mA}$
$I_{IH}$	Input HIGH Current	2.0	2.0	$\mu\text{A}$	Max	$V_{IN} = 2.7\text{V}$
$I_{IL}$	Input LOW Current	7.0	100	$\mu\text{A}$	Max	$V_{IN} = 7.0\text{V}$
$I_{CC}$	Output HIGH Leakage Current	20	250	$\mu\text{A}$	Max	$V_{OUT} = V_{CC}$
$I_{IO}$	Input Leakage Test	4.75		V	0.0	$I_D = 1.9\text{ mA}$ All Other Pins Grounded
$I_{OD}$	Output Leakage Current	3.75		$\mu\text{A}$	0.0	$V_{IO} = 150\text{ mV}$ All Other Pins Grounded
$I_{IL}$	Input LOW Current	-0.9		mA	Max	$V_{IN} = 0.5\text{V}$
$I_{OS}$	Output Short-Circuit Current	-60	-150	mA	Max	$V_{OUT} = 0\text{V}$
$I_{OCH}$	Power Supply Current	25	38	mA	Max	$V_O = \text{HIGH}$



## 54F/74F283

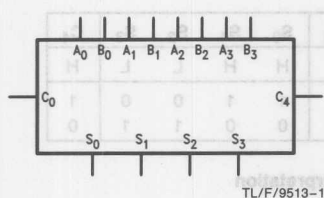
# 4-Bit Binary Full Adder with Fast Carry

## General Description

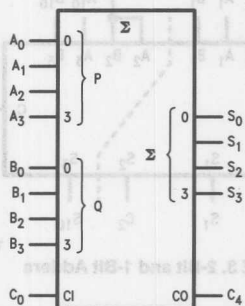
The 'F283 high-speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary words ( $A_0$ – $A_3$ ,  $B_0$ – $B_3$ ) and a Carry input ( $C_0$ ). It generates the binary Sum outputs ( $S_0$ – $S_3$ ) and the Carry output ( $C_4$ ) from the most significant bit. The 'F283 will operate with either active HIGH or active LOW operands (positive or negative logic).

**Ordering Code:** See Section 5

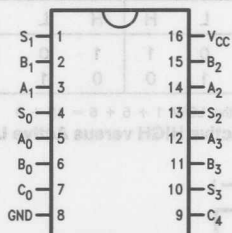
## Logic Symbols



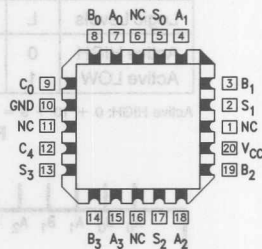
### IEEE/IEC



### Pin Assignment for DIP, SOIC and Flatpak



### Pin Assignment for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_0$ – $A_3$	A Operand Inputs	1.0/2.0	20 $\mu$ A/–1.2 mA
$B_0$ – $B_3$	B Operand Inputs	1.0/2.0	20 $\mu$ A/–1.2 mA
$C_0$	Carry Input	1.0/1.0	20 $\mu$ A/–0.6 mA
$S_0$ – $S_3$	Sum Outputs	50/33.3	–1 mA/20 mA
$C_4$	Carry Output	50/33.3	–1 mA/20 mA



## Functional Description

The 'F283 adds two 4-bit binary words (A plus B) plus the incoming Carry ( $C_0$ ). The binary sum appears on the Sum ( $S_0$ – $S_3$ ) and outgoing carry ( $C_4$ ) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$$2^0 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1) + 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3) = S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$

Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus  $C_0$ ,  $A_0$ ,  $B_0$  can be arbitrarily assigned to pins 5, 6 and 7 for DIPs, and 7, 8 and 9 for chip carrier packages. Due to the symmetry of the binary add function, the 'F283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). See Figure 1. Note that if  $C_0$  is not used it must be tied LOW for active HIGH logic or tied HIGH for active LOW logic.

Due to pin limitations, the intermediate carries of the 'F283 are not brought out for use as inputs or outputs. However,

other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. Figure 2 shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder ( $A_3$ ,  $B_3$ ) LOW makes  $S_3$  dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, Figure 3 shows a way of dividing the 'F283 into a 2-bit and a 1-bit adder. The third stage adder ( $A_2$ ,  $B_2$ ,  $S_2$ ) is used merely as a means of getting a carry ( $C_{10}$ ) signal into the fourth stage (via  $A_2$  and  $B_2$ ) and bringing out the carry from the second stage on  $S_2$ . Note that as long as  $A_2$  and  $B_2$  are the same, whether HIGH or LOW, they do not influence  $S_2$ . Similarly, when  $A_2$  and  $B_2$  are the same the carry into the third stage does not influence the carry out of the third stage. Figure 4 shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs  $S_0$ ,  $S_1$  and  $S_2$  present a binary number equal to the number of inputs  $I_1$ – $I_5$  that are true. Figure 5 shows one method of implementing a 5-input majority gate. When three or more of the inputs  $I_1$ – $I_5$  are true, the output  $M_5$  is true.

	$C_0$	$A_0$	$A_1$	$A_2$	$A_3$	$B_0$	$B_1$	$B_2$	$B_3$	$S_0$	$S_1$	$S_2$	$S_3$	$C_4$
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH:  $0 + 10 + 9 = 3 + 16$  Active LOW:  $1 + 5 + 6 = 12 + 0$

FIGURE 1. Active HIGH versus Active LOW Interpretation

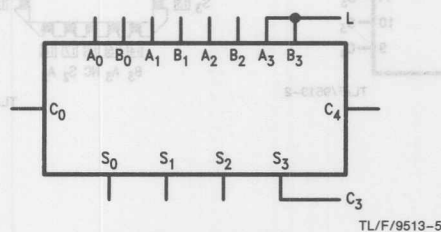


FIGURE 2. 3-Bit Adder

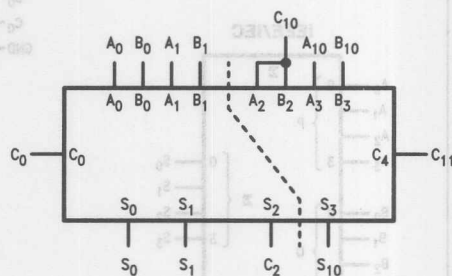


FIGURE 3. 2-Bit and 1-Bit Adders

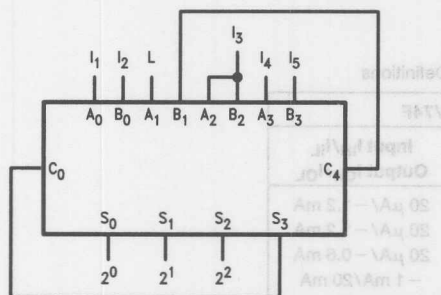


FIGURE 4. 5-Input Encoder

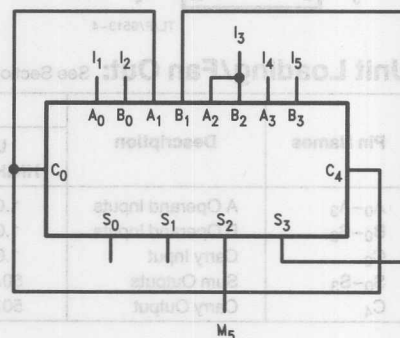


FIGURE 5. 5-Input Majority Gate

## Logic Diagram

Storage Temperature  
Office/Telephone  
please contact  
National Semiconductor Sales  
specified devices are required  
TLF/9513

These conditions is not implied. The output voltage limit is current limited, not at all. Either voltage limit or current limit is not implied. The output voltage limit is current limited, not at all. Either voltage limit or current limit is not implied.

DC Electrical Characteristics

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

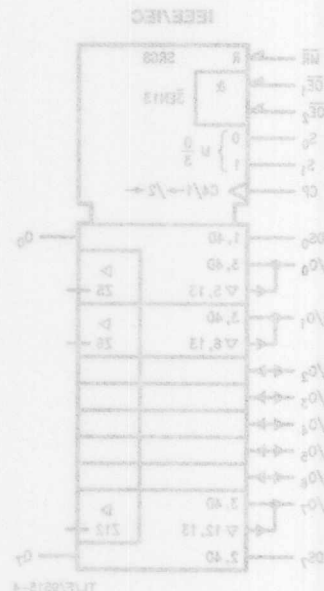
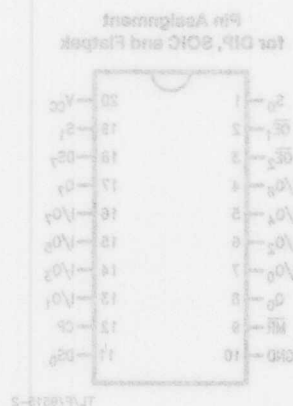
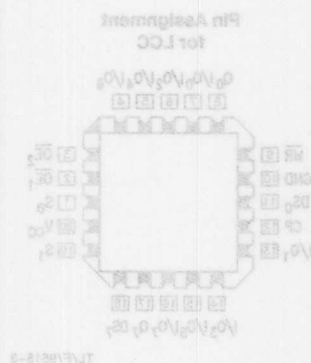
Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.5 2.7		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6 -1.2	mA	Max	V <sub>IN</sub> = 0.5V (C <sub>O</sub> ) V <sub>IN</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		36	55	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		36	55	mA	Max	V <sub>O</sub> = LOW

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay $C_0$ to $S_n$	3.5	7.0	9.5	3.5	14.0	3.5	11.0	ns	2-3
$t_{PHL}$		3.0	7.0	9.5	3.0	14.0	3.0	11.0		
$t_{PLH}$	Propagation Delay $A_n$ or $B_n$ to $S_n$	3.0	7.0	9.5	3.0	17.0	3.0	13.0	ns	2-3
$t_{PHL}$		3.0	7.0	9.5	3.0	14.0	3.0	11.5		
$t_{PLH}$	Propagation Delay $C_0$ to $C_4$	3.0	5.7	7.5	3.0	10.5	3.0	8.5	ns	2-3
$t_{PHL}$		3.0	5.4	7.0	2.5	10.0	3.0	8.0		
$t_{PLH}$	Propagation Delay $A_n$ or $B_n$ to $C_4$	3.0	5.7	7.5	3.0	10.5	3.0	8.5	ns	2-3
$t_{PHL}$		2.5	5.3	7.0	2.5	10.0	2.5	8.0		





## 54F/74F299 Octal Universal Shift/Storage Register with Common Parallel I/O Pins

### General Description

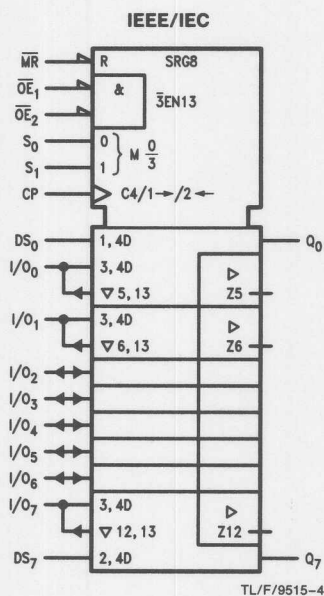
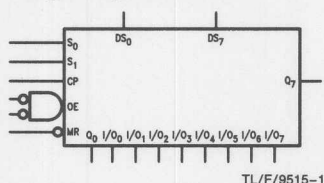
The 'F299 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs,  $Q_0$ – $Q_7$ , are provided to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

### Features

- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- TRI-STATE outputs for bus-oriented applications
- Guaranteed 4000V minimum ESD protection

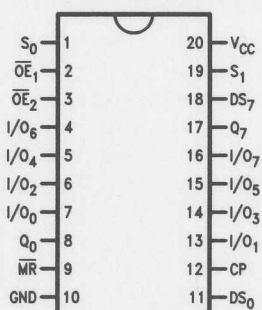
**Ordering Code:** See Section 5

### Logic Symbols

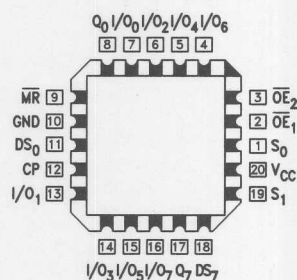


### Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



Pin Assignment for LCC



# Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/ -0.6 mA
DS <sub>0</sub>	Serial Data Input for Right Shift	1.0/1.0	20 $\mu$ A/ -0.6 mA
DS <sub>7</sub>	Serial Data Input for Left Shift	1.0/1.0	20 $\mu$ A/ -0.6 mA
S <sub>0</sub> , S <sub>1</sub>	Mode Select Inputs	1.0/2.0	20 $\mu$ A/ -1.2 mA
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{OE}_1, \overline{OE}_2$	TRI-STATE Output Enable Inputs (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
I/O <sub>0</sub> -I/O <sub>7</sub>	Parallel Data Inputs or TRI-STATE Parallel Outputs	3.5/1.083 150/40(33.3)	70 $\mu$ A/ -0.65 mA -3 mA/24 mA (20 mA)
Q <sub>0</sub> , Q <sub>7</sub>	Serial Outputs	50/33.3	-1 mA/20 mA

## Functional Description

The 'F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S<sub>0</sub> and S<sub>1</sub>, as shown in the Mode Select Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q<sub>0</sub> and Q<sub>7</sub> are also brought out on other pins for expansion in serial shifting of longer words.

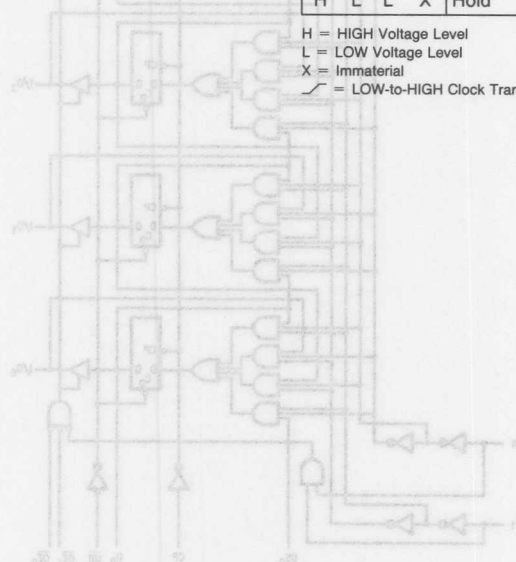
A LOW signal on  $\overline{MR}$  overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either  $\overline{OE}_1$  or  $\overline{OE}_2$  disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The TRI-STATE outputs are also disabled by HIGH signals on both S<sub>0</sub> and S<sub>1</sub> in preparation for a parallel load operation.

Mode Select Table

Inputs				Response
$\overline{MR}$	S <sub>1</sub>	S <sub>0</sub>	CP	
L	X	X	X	Asynchronous Reset; Q <sub>0</sub> -Q <sub>7</sub> = LOW
H	H	H	↗	Parallel Load; I/O <sub>n</sub> → Q <sub>n</sub>
H	L	H	↗	Shift Right; DS <sub>0</sub> → Q <sub>0</sub> , Q <sub>0</sub> → Q <sub>1</sub> , etc.
H	H	L	↗	Shift Left; DS <sub>7</sub> → Q <sub>7</sub> , Q <sub>7</sub> → Q <sub>6</sub> , etc.
H	L	L	X	Hold

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
↗ = LOW-to-HIGH Clock Transition



Please note that the diagram is provided only for the understanding of logic operations and should not be used to establish production design.





## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
---	----------------

Input Voltage (Note 2)	-0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	-30 mA to +5.0 mA
------------------------	-------------------

ESD Last Passing Voltage (Min)	4000V
--------------------------------	-------

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Voltage Applied to Output in HIGH State (with V<sub>CC</sub> = 0V)

Standard Output

-0.5V to V<sub>CC</sub>

TRI-STATE Output

-0.5V to +5.5V

Current Applied to Output in LOW State (Max)

twice the rated I<sub>OL</sub> (mA)

## Recommended Operating Conditions

Free Air Ambient Temperature

Military

-55°C to +125°C

Commercial

0°C to +70°C

Supply Voltage

Military

+4.5V to +5.5V

Commercial

+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA (Q <sub>0</sub> , Q <sub>7</sub> , I/O <sub>n</sub> )
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = -3 mA (I/O <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.5			V	I <sub>OH</sub> = -1 mA (Q <sub>0</sub> , Q <sub>7</sub> , I/O <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = -3 mA (I/O <sub>n</sub> )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA (Q <sub>0</sub> , Q <sub>7</sub> , I/O <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	54 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
		74 10% V <sub>CC</sub>		0.5		V	I <sub>OL</sub> = 20 mA (Q <sub>0</sub> , Q <sub>7</sub> )
		74 10% V <sub>CC</sub>		0.5		Min	I <sub>OL</sub> = 24 mA (I/O <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V (CP, DS <sub>0</sub> , DS <sub>7</sub> , S <sub>0</sub> , S <sub>1</sub> , MR, OE <sub>1</sub> , OE <sub>2</sub> )
		74F		5.0	μA		
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V (CP, DS <sub>0</sub> , DS <sub>7</sub> , S <sub>0</sub> , S <sub>1</sub> , MR, OE <sub>1</sub> , OE <sub>2</sub> )
		74F		7.0	μA		
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)	54F		1.0	mA	Max	V <sub>IN</sub> = 5.5V (I/O <sub>n</sub> )
		74F		0.5	mA		
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50	μA		
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6 -1.2	mA	Max	V <sub>IN</sub> = 0.5V (CP, DS <sub>0</sub> , DS <sub>7</sub> , MR, OE <sub>1</sub> , OE <sub>2</sub> ) V <sub>IN</sub> = 0.5V (S <sub>0</sub> , S <sub>1</sub> )
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>I/O</sub> = 2.7V (I/O <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			-650	μA	Max	V <sub>I/O</sub> = 0.5V (I/O <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CGH</sub>	Power Supply Current		68	95	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		68	95	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		68	95	mA	Max	V <sub>O</sub> = HIGH Z

# **AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Input Frequency	70	100				70		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay CP to $Q_0$ or $Q_7$	4.0	7.0	8.0			4.0	8.5	ns	2-3
$t_{\text{PHL}}$	Propagation Delay CP to $I/O_n$	4.5	6.5	8.0			4.5	8.5		
$t_{\text{PLH}}$	Propagation Delay CP to $I/O_n$	3.5	7.0	9.0			3.5	10.0	ns	2-3
$t_{\text{PHL}}$	Propagation Delay CP to $I/O_n$	4.0	8.5	9.0			4.0	10.0		
$t_{\text{PHL}}$	Propagation Delay $\overline{\text{MR}}$ to $Q_0$ or $Q_7$	5.5	7.5	9.5			5.5	10.5		
$t_{\text{PHL}}$	Propagation Delay $\overline{\text{MR}}$ to $I/O_n$	5.5	11.0	10.0			5.5	10.5		
$t_{\text{PZH}}$	Output Enable Time	3.5	6.0	8.0			3.5	9.0	ns	2-5
$t_{\text{PZL}}$	$\overline{\text{OE}}$ to $I/O_n$	4.0	7.0	10.0			4.0	11.0		
$t_{\text{PHZ}}$	Output Disable Time	2.0	4.5	6.0			2.0	7.0	ns	2-5
$t_{\text{PLZ}}$	$\overline{\text{OE}}$ to $I/O_n$	1.0	4.0	5.5			1.0	6.5		
$t_{\text{PZH}}$	Output Enable Time	3.5		9.0			3.5	10.0	ns	2-5
$t_{\text{PZL}}$	$S_n$ to $I/O_n$	4.0		10.0			4.0	11.0		
$t_{\text{PHZ}}$	Output Disable Time	2.5		6.0			2.5	7.0	ns	2-5
$t_{\text{PLZ}}$	$S_n$ to $I/O_n$	1.5		5.5			1.5	6.5		

## **AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	8.5				8.5		ns	2-6
$t_s(\text{L})$	$S_0$ or $S_1$ to CP	8.5				8.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0				0			
$t_h(\text{L})$	$S_0$ or $S_1$ to CP	0				0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	5.0				5.0		ns	2-6
$t_s(\text{L})$	$I/O_n$ , $DS_0$ or $DS_7$ to CP	5.0				5.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0				2.0			
$t_h(\text{L})$	$I/O_n$ , $DS_0$ or $DS_7$ to CP	2.0				2.0			
$t_w(\text{H})$	CP Pulse Width	5.0				5.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	5.0				5.0			
$t_w(\text{L})$	$\overline{\text{MR}}$ Pulse Width, LOW	5.0				5.0			
$t_{\text{rec}}$	Recovery Time, $\overline{\text{MR}}$ to CP	7.0				7.0		ns	2-6

## 54F/74F322

# Octal Serial/Parallel Register with Sign Extend

## General Description

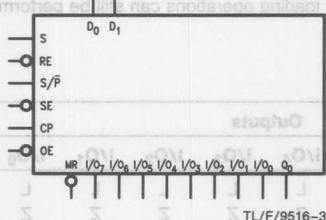
The 'F322 is an 8-bit shift register with provision for either serial or parallel loading and with TRI-STATE® parallel outputs plus a bi-state serial output. Parallel data inputs and parallel outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store), shift right with serial entry, shift right with sign extend and parallel load. An asynchronous Master Reset (MR) input overrides clocked operation and clears the register.

## Features

- Multiplexed parallel I/O ports
- Separate serial input and output
- Sign extend function
- TRI-STATE outputs for bus applications

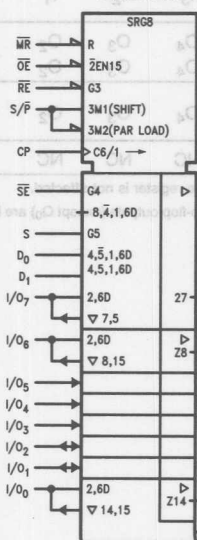
**Ordering Code:** See Section 5

## Logic Symbols



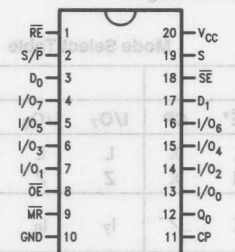
TL/F/9516-3

## IEEE/IEC



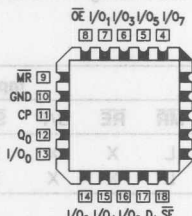
TL/F/9516-5

## Pin Assignment for DIP, SOIC and Flatpak



TL/F/9516-1

## Pin Assignment for LCC



TL/F/9516-2

# Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{RE}$	Register Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
S/P	Serial (HIGH) or Parallel (LOW) Mode Control Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{SE}$	Sign Extend Input (Active LOW)	1.0/3.0	20 $\mu$ A/ -1.8 mA
S	Serial Data Select Input	1.0/2.0	20 $\mu$ A/ -1.2 mA
$D_0, D_1$	Serial Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$Q_0$	Bi-State Serial Output	50/33.3	-1 mA/ -20 mA
$I/O_0-I/O_7$	Multiplexed Parallel Data Inputs or TRI-STATE Parallel Data Outputs	3.5/1.083	70 $\mu$ A/ -0.65 mA
		150/40 (33.3)	-3 mA/24 mA (20 mA)

## Functional Description

The 'F322 contains eight D-type edge triggered flip-flops and the interstage gating required to perform right shift and the intrastage gating necessary for hold and synchronous parallel load operations. A LOW signal on  $\overline{RE}$  enables shifting or parallel loading, while a HIGH signal enables the hold mode. A HIGH signal on S/P enables shift right, while a LOW signal disables the TRI-STATE output buffers and enables parallel loading. In the shift right mode a HIGH signal

on  $\overline{SE}$  enables serial entry from either  $D_0$  or  $D_1$ , as determined by the S input. A LOW signal on  $\overline{SE}$  enables shift right but  $Q_7$  reloads its contents, thus performing the sign extend function required for the 'F384 Twos Complement Multiplier. A HIGH signal on  $\overline{OE}$  disables the TRI-STATE output buffers, regardless of the other control inputs. In this condition the shifting and loading operations can still be performed.

Mode Select Table

Mode	Inputs							Outputs							Q <sub>0</sub>	
	MR	RE	S/P	SE	S	OE*	CP	I/O <sub>7</sub>	I/O <sub>6</sub>	I/O <sub>5</sub>	I/O <sub>4</sub>	I/O <sub>3</sub>	I/O <sub>2</sub>	I/O <sub>1</sub>		I/O <sub>0</sub>
Clear	L	X	X	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	X	X	X	X	H	X	Z	Z	Z	Z	Z	Z	Z	Z	L
Parallel Load	H	L	L	X	X	X		I <sub>7</sub>	I <sub>6</sub>	I <sub>5</sub>	I <sub>4</sub>	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	I <sub>0</sub>
Shift Right	H	L	H	H	L	L		D <sub>0</sub>	O <sub>7</sub>	O <sub>6</sub>	O <sub>5</sub>	O <sub>4</sub>	O <sub>3</sub>	O <sub>2</sub>	O <sub>1</sub>	O <sub>1</sub>
	H	L	H	H	H	L		D <sub>1</sub>	O <sub>7</sub>	O <sub>6</sub>	O <sub>5</sub>	O <sub>4</sub>	O <sub>3</sub>	O <sub>2</sub>	O <sub>1</sub>	O <sub>1</sub>
Sign Extend	H	L	H	L	X	L		O <sub>7</sub>	O <sub>7</sub>	O <sub>6</sub>	O <sub>5</sub>	O <sub>4</sub>	O <sub>3</sub>	O <sub>2</sub>	O <sub>1</sub>	O <sub>1</sub>
Hold	H	H	X	X	X	L		NC	NC	NC	NC	NC	NC	NC	NC	NC

\*When the  $\overline{OE}$  input is HIGH all  $I/O_n$  terminals are at the high impedance state; sequential operation or clearing of the register is not affected.

**Note 1:**  $I_7-I_0$  = The level of the steady-state input at the respective  $I/O$  terminal is loaded into the flip-flop while the flip-flop outputs (except  $Q_0$ ) are isolated from the  $I/O$  terminal.

**Note 2:**  $D_0, D_1$  = The level of the steady-state inputs to the serial multiplexer input.

**Note 3:**  $O_7-O_0$  = The level of the respective  $Q_n$  flip-flop prior to the last Clock LOW-to-HIGH transition.

H = HIGH Voltage Level

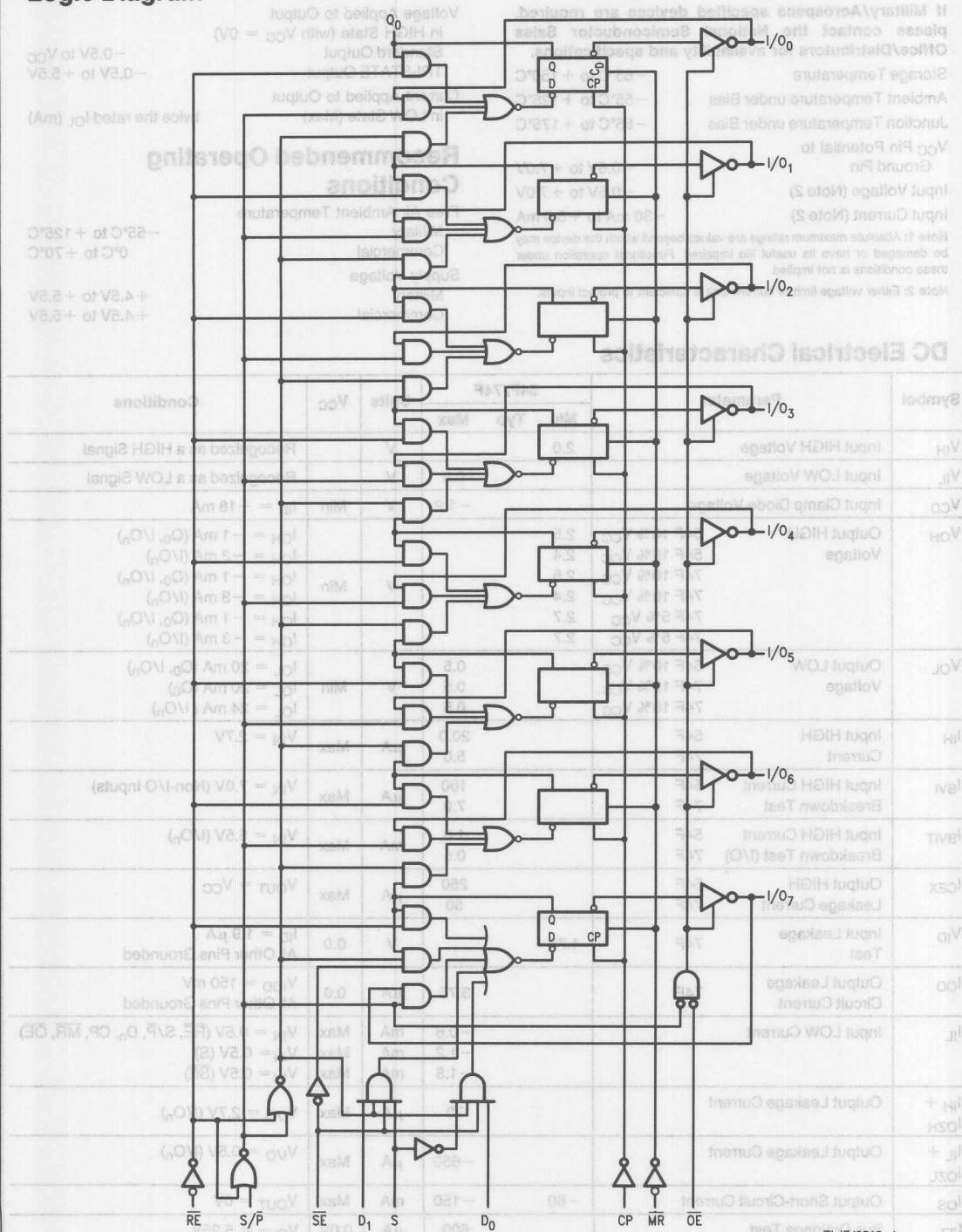
L = LOW Voltage Level

Z = High Impedance Output State

↗ = LOW-to-HIGH Transition

NC = No Change

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

Voltage Applied to Output in HIGH State (with V<sub>CC</sub> = 0V)

Standard Output −0.5V to V<sub>CC</sub>

TRI-STATE Output −0.5V to +5.5V

Current Applied to Output in LOW State (Max)

twice the rated I<sub>OL</sub> (mA)

## Recommended Operating Conditions

Free Air Ambient Temperature

Military −55°C to +125°C

Commercial 0°C to +70°C

Supply Voltage

Military +4.5V to +5.5V

Commercial +4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA (Q <sub>0</sub> , I/O <sub>n</sub> )
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA (I/O <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA (Q <sub>0</sub> , I/O <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA (I/O <sub>n</sub> )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA (Q <sub>0</sub> , I/O <sub>n</sub> )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −3 mA (I/O <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA (Q <sub>0</sub> , I/O <sub>n</sub> )
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA (Q <sub>0</sub> )
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA (I/O <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V (Non-I/O Inputs)
		74F		7.0			
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)	54F		1.0	mA	Max	V <sub>IN</sub> = 5.5V (I/O <sub>n</sub> )
		74F		0.5			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V (RE, S/P, D <sub>n</sub> , CP, MR, OE)
				−1.2	mA	Max	V <sub>IN</sub> = 0.5V (S)
				−1.8	mA	Max	V <sub>IN</sub> = 0.5V (SE)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>I/O</sub> = 2.7V (I/O <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			−650	μA	Max	V <sub>I/O</sub> = 0.5V (I/O <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CC</sub>	Power Supply Current		60	90	mA	Max	

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	70	90		50		70		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay CP to I/O <sub>n</sub>	3.5	7.0	7.5	3.5	9.5	3.5	8.5	ns	2-3
$t_{\text{PHL}}$	CP to I/O <sub>n</sub>	5.0	8.5	11.0	3.5	10.0	5.0	12.0		
$t_{\text{PLH}}$	Propagation Delay CP to Q <sub>0</sub>	3.5	7.0	9.0	3.5	11.0	3.5	10.0	ns	2-3
$t_{\text{PHL}}$	CP to Q <sub>0</sub>	3.5	7.0	8.0	3.5	10.0	3.5	9.0		
$t_{\text{PHL}}$	Propagation Delay MR to I/O <sub>n</sub>	6.0	10.0	13.0	6.0	15.0	6.0	14.0	ns	2-3
$t_{\text{PHL}}$	Propagation Delay MR to Q <sub>0</sub>	5.5	7.5	12.0	5.5	14.0	5.5	13.0	ns	2-3
$t_{\text{pZH}}$	Output Enable Time OE to I/O <sub>n</sub>	3.0	6.5	9.0	3.0	12.5	3.0	10.0	ns	2-5
$t_{\text{pZL}}$	OE to I/O <sub>n</sub>	4.0	8.5	11.0	4.0	14.5	4.0	12.0		
$t_{\text{PHZ}}$	Output Disable Time OE to I/O <sub>n</sub>	2.0	4.5	6.0	2.0	8.0	2.0	7.0	ns	2-5
$t_{\text{PLZ}}$	OE to I/O <sub>n</sub>	2.0	5.0	7.0	2.0	10.0	2.0	8.0		
$t_{\text{pZH}}$	Output Enable Time S/P to I/O <sub>n</sub>	4.5	8.0	10.5	4.5	13.5	4.5	11.5	ns	2-5
$t_{\text{pZL}}$	S/P to I/O <sub>n</sub>	5.5	10.0	14.0	5.5	17.0	5.5	15.0		
$t_{\text{PHZ}}$	Output Disable Time S/P to I/O <sub>n</sub>	5.0	9.0	11.5	5.0	16.5	5.0	12.5	ns	2-5
$t_{\text{PLZ}}$	S/P to I/O <sub>n</sub>	6.0	12.0	15.5	6.0	19.5	6.0	16.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $\overline{\text{RE}}$ to CP	6.0 14.0		14.0 18.0		7.0 16.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $\overline{\text{RE}}$ to CP	0 0		0 0		0 0		ns	2-6
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $D_0, D_1$ or $I/O_n$ to CP	6.5 6.5		8.5 8.5		7.5 7.5		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $D_0, D_1$ or $I/O_n$ to CP	2.0 2.0		3.0 3.0		3.0 3.0		ns	2-6
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW SE to CP	7.0 2.5		9.0 11.0		8.0 3.5		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $\overline{\text{SE}}$ to CP	2.0 0.0		2.0 1.0		2.0 0.0		ns	2-6
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $S/\overline{P}$ to CP	11.0 13.5		13.0 21.0		12.0 15.5		ns	2-6
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW S to CP	6.5 9.0		8.5 11.0		7.5 10.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW S or $S/\overline{P}$ to CP	0 0		1.0 0		0 0		ns	2-6
$t_w(\text{H})$ $t_w(\text{L})$	CP Pulse Width, HIGH or LOW	7.0		8.0		7.0		ns	2-4
$t_w(\text{L})$	$\overline{\text{MR}}$ Pulse Width, LOW	5.5		7.5		6.5			2-4
$t_{\text{rec}}$	Recovery Time $\overline{\text{MR}}$ to CP	8.0		12.0		8.0		ns	2-6



## 54F/74F323 Octal Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins

### General Description

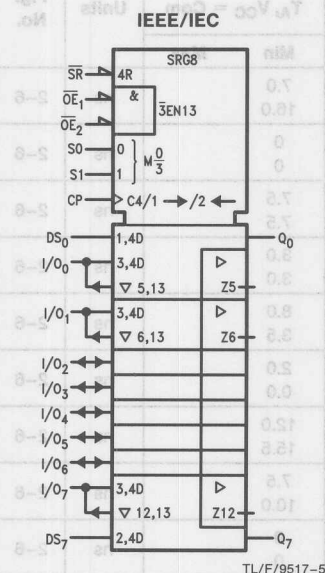
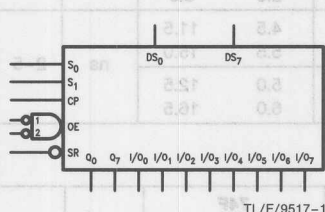
The 'F323 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Its function is similar to the 'F299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for  $Q_0$  and  $Q_7$  to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

### Features

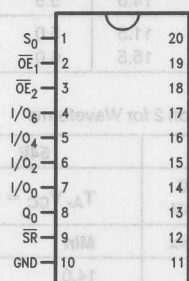
- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- TRI-STATE outputs for bus-oriented applications
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

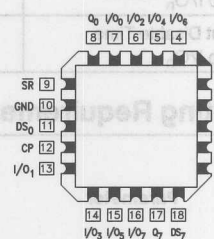
### Logic Symbols



Pin Assignment for DIP, SOIC and Flatpak



Pin Assignment for LCC



		HIGH/LOW	Output $I_{OH}/I_{OL}$
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/ -0.6 mA
DS <sub>0</sub>	Serial Data Input for Right Shift	1.0/1.0	20 $\mu$ A/ -0.6 mA
DS <sub>7</sub>	Serial Data Input for Left Shift	1.0/1.0	20 $\mu$ A/ -0.6 mA
S <sub>0</sub> , S <sub>1</sub>	Mode Select Inputs	1.0/2.0	20 $\mu$ A/ -1.2 mA
$\overline{SR}$	Synchronous Reset Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{OE}_1, \overline{OE}_2$	TRI-STATE Output Enable Inputs (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
I/O <sub>0</sub> -I/O <sub>7</sub>	Multiplexed Parallel Data Inputs	3.5/1.083	70 $\mu$ A/ -0.65 mA
	TRI-STATE Parallel Data Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)
Q <sub>0</sub> , Q <sub>7</sub>	Serial Outputs	50/33.3	-1 mA/20 mA

## Functional Description

The 'F323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S<sub>0</sub> and S<sub>1</sub> as shown in the Mode Select Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q<sub>0</sub> and Q<sub>7</sub> are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on  $\overline{SR}$  overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All

other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either  $\overline{OE}_1$  or  $\overline{OE}_2$  disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S<sub>0</sub> and S<sub>1</sub> in preparation for a parallel load operation.

Mode Select Table

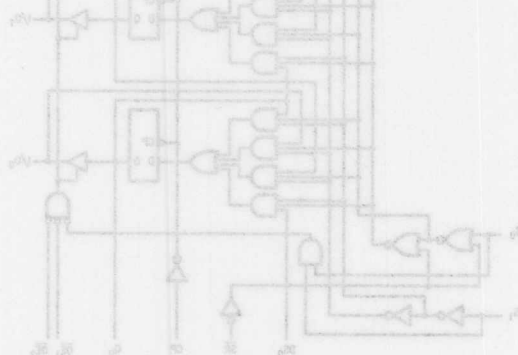
Inputs				Response
$\overline{SR}$	S <sub>1</sub>	S <sub>0</sub>	CP	
L	X	X	↗	Synchronous Reset; Q <sub>0</sub> -Q <sub>7</sub> = LOW
H	H	H	↗	Parallel Load; I/O <sub>n</sub> → Q <sub>n</sub>
H	L	H	↗	Shift Right; DS <sub>0</sub> → Q <sub>0</sub> , Q <sub>0</sub> → Q <sub>1</sub> , etc.
H	H	L	↗	Shift Left; DS <sub>7</sub> → Q <sub>7</sub> , Q <sub>7</sub> → Q <sub>6</sub> , etc.
H	L	L	X	Hold

H = HIGH Voltage Level

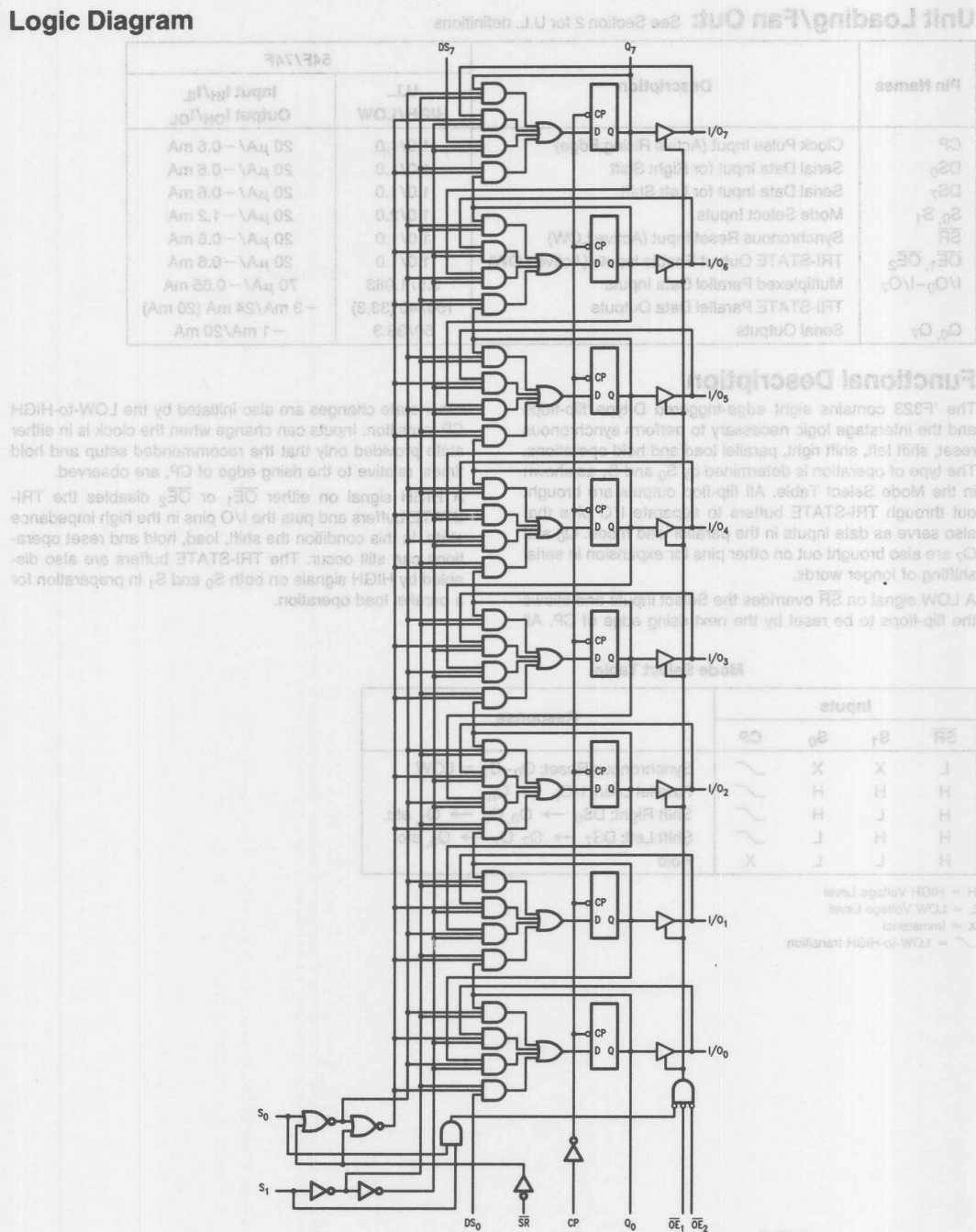
L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH transition



## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

ESD Last Passing Voltage (Min) 4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	−55°C to +125°C
Military	0°C to +70°C
Commercial	
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA (Q <sub>0</sub> , Q <sub>7</sub> )
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA (I/O <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA (Q <sub>0</sub> , Q <sub>7</sub> )
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA (I/O <sub>n</sub> )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA (Q <sub>0</sub> , Q <sub>7</sub> )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −3 mA (I/O <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA (I/O <sub>n</sub> , Q <sub>0</sub> , Q <sub>7</sub> )
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA (Q <sub>0</sub> , Q <sub>7</sub> )
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA (I/O <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V (Non I/O Inputs)
		74F		7.0			
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)	54F		1.0	mA	Max	V <sub>IN</sub> = 5.5V (I/O Inputs)
		74F		0.5			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V (CP, DS <sub>0</sub> , DS <sub>7</sub> , SR, OE <sub>1</sub> , OE <sub>2</sub> )
				−1.2		Max	V <sub>IN</sub> = 0.5V (S <sub>0</sub> , S <sub>1</sub> )
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current		68	95	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		68	95	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		68	95	mA	Max	V <sub>O</sub> = HIGH Z



# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Input Frequency	70	100				70		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	4.0	7.0	8.0			4.0	8.5		
$t_{\text{PHL}}$	CP to $Q_0$ or $Q_7$	4.5	6.5	8.0			4.5	8.5	ns	2-3
$t_{\text{PLH}}$	Propagation Delay	3.5	7.0	9.0			3.5	10.0		
$t_{\text{PHL}}$	CP to $I/O_n$	4.0	8.5	9.0			4.0	10.0		
$t_{\text{PZH}}$	Output Enable Time	3.5	6.0	8.0			3.5	9.0		
$t_{\text{PZL}}$		4.0	7.0	10.0			4.0	11.0	ns	2-5
$t_{\text{PHZ}}$	Output Disable Time	2.0	4.5	6.0			2.0	7.0		
$t_{\text{PLZ}}$		1.0	4.0	5.5			1.0	6.5		
$t_{\text{PZH}}$	Output Enable Time	3.5		9.0			3.5	10.0	ns	2-5
$t_{\text{PZL}}$	$S_n$ to $I/O_n$	4.0		10.0			4.0	11.0		
$t_{\text{PHZ}}$	Output Disable Time	2.5		6.0			2.5	7.0	ns	2-5
$t_{\text{PLZ}}$	$S_n$ to $I/O_n$	1.0		5.5			1.5	6.5		

## AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	8.5				8.5		ns	2-6
$t_s(\text{L})$	$S_0$ or $S_1$ to CP	8.5				8.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0				0			
$t_h(\text{L})$	$S_0$ or $S_1$ to CP	0				0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	5.0				5.0		ns	2-6
$t_s(\text{L})$	$I/O_n$ , $DS_0$ , $DS_7$ to CP	5.0				5.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0				2.0			
$t_h(\text{L})$	$I/O_n$ , $DS_0$ , $DS_7$ to CP	2.0				2.0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	10.0				10.0		ns	2-6
$t_s(\text{L})$	$\overline{SR}$ to CP	10.0				10.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0				0			
$t_h(\text{L})$	$\overline{SR}$ to CP	0				0			
$t_w(\text{H})$	CP Pulse Width	5.0				5.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	5.0				5.0			



## 54F/74F350 4-Bit Shifter with TRI-STATE® Outputs

### General Description

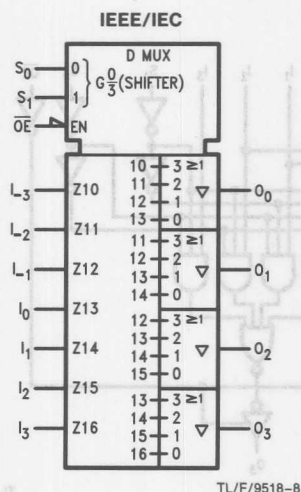
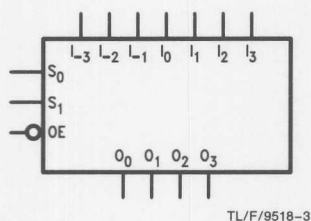
The 'F350 is a specialized multiplexer that accepts a 4-bit word and shifts it 0, 1, 2 or 3 places, as determined by two Select ( $S_0, S_1$ ) inputs. For expansion to longer words, three linking inputs are provided for lower-order bits; thus two packages can shift an 8-bit word, four packages a 16-bit word, etc. Shifting by more than three places is accomplished by paralleling the TRI-STATE outputs of different packages and using the Output Enable ( $\overline{OE}$ ) inputs as a third Select level. With appropriate interconnections, the 'F350 can perform zero-backfill, sign-extend or end-around (barrel) shift functions.

### Features

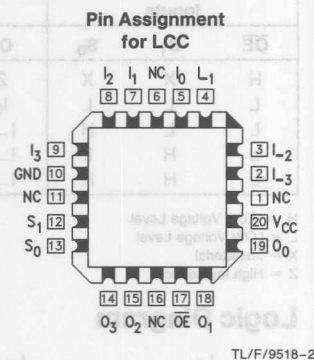
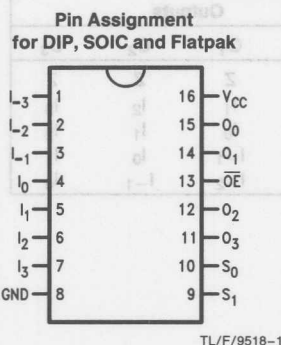
- Linking inputs for word expansion
- TRI-STATE outputs for extending shift range

**Ordering Code:** See Section 5

### Logic Symbols



### Connection Diagrams



# Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_H/I_L$ Output $O_H/O_L$
$S_0, S_1$	Select Inputs	1.0/2.0	20 $\mu$ A / -1.2 mA
$I_3-I_0$	Data Inputs	1.0/2.0	20 $\mu$ A / -1.2 mA
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/2.0	20 $\mu$ A / -1.2 mA
$O_3-O_0$	TRI-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

## Functional Description

The 'F350 is operationally equivalent to a 4-input multiplexer with the inputs connected so that the select code causes successive one-bit shifts of the data word. This internal connection makes it possible to perform shifts of 0, 1, 2 or 3 places on words of any length.

A 4-bit data word is introduced at the  $I_n$  inputs and is shifted according to the code applied to the select inputs  $S_0, S_1$ . Outputs  $O_0-O_3$  are TRI-STATE, controlled by an active LOW output enable ( $\overline{OE}$ ). When  $\overline{OE}$  is LOW, data outputs will follow selected data inputs; when HIGH, the data outputs will be forced to the high impedance state. This feature allows shifters to be cascaded on the same output lines or

to a common bus. The shift function can be logical, with zeros pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop.

## Logic Equations

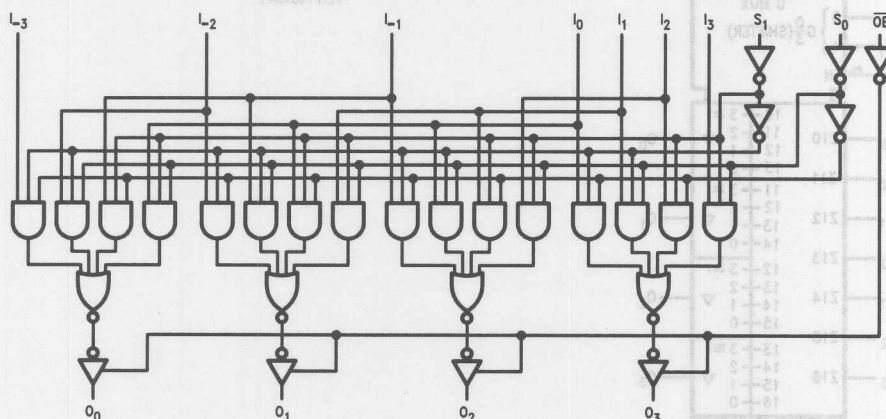
$$\begin{aligned} O_0 &= \overline{S_0}S_1I_0 + S_0\overline{S_1}I_{-1} + \overline{S_0}S_1I_{-2} + S_0\overline{S_1}I_{-3} \\ O_1 &= \overline{S_0}S_1I_1 + S_0\overline{S_1}I_0 + \overline{S_0}S_1I_{-1} + S_0\overline{S_1}I_{-2} \\ O_2 &= \overline{S_0}S_1I_2 + S_0\overline{S_1}I_1 + \overline{S_0}S_1I_0 + S_0\overline{S_1}I_{-1} \\ O_3 &= \overline{S_0}S_1I_3 + S_0\overline{S_1}I_2 + \overline{S_0}S_1I_1 + S_0\overline{S_1}I_0 \end{aligned}$$

## Truth Table

Inputs			Outputs			
$\overline{OE}$	$S_1$	$S_0$	$O_0$	$O_1$	$O_2$	$O_3$
H	X	X	Z	Z	Z	Z
L	L	L	$I_0$	$I_1$	$I_2$	$I_3$
L	L	H	$I_{-1}$	$I_0$	$I_1$	$I_2$
L	H	L	$I_{-2}$	$I_{-1}$	$I_0$	$I_1$
L	H	H	$I_{-3}$	$I_{-2}$	$I_{-1}$	$I_0$

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

## Logic Diagram

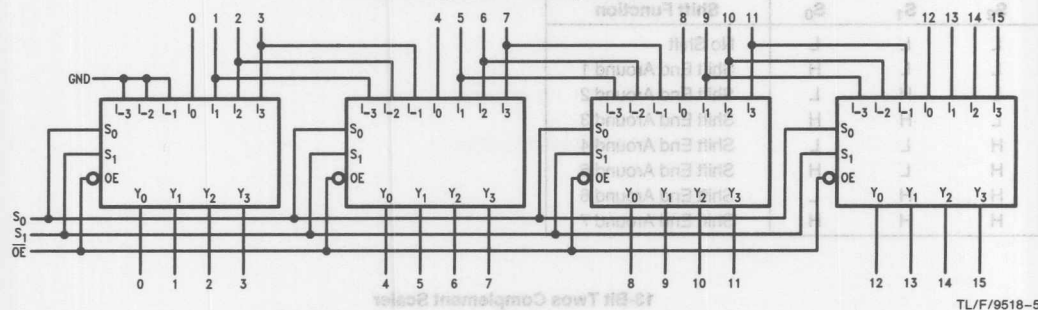


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

TL/F/9518-4

## Applications

16-Bit Shift-Up 0 to 3 Places, Zero Backfill

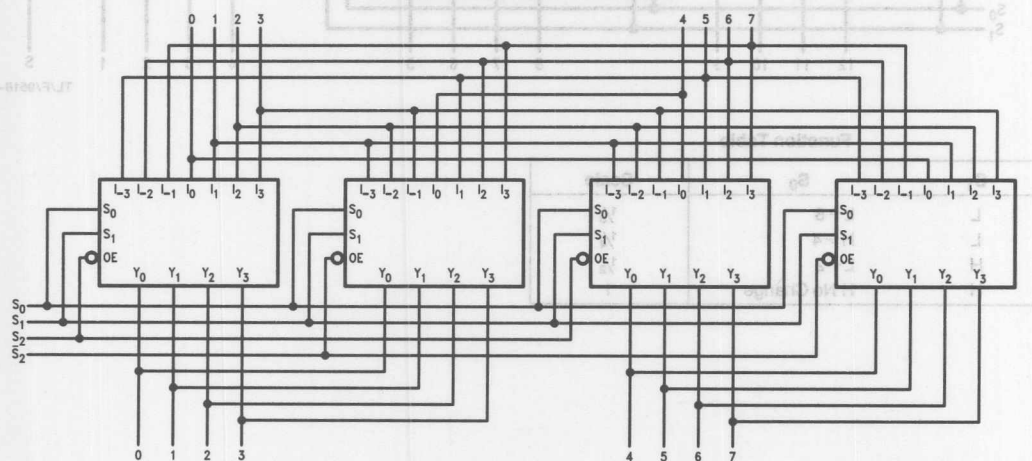


TL/F/9518-5

Function Table

S <sub>1</sub>	S <sub>0</sub>	Shift Function
L	L	No Shift
L	H	Shift 1 Place
H	L	Shift 2 Places
H	H	Shift 3 Places

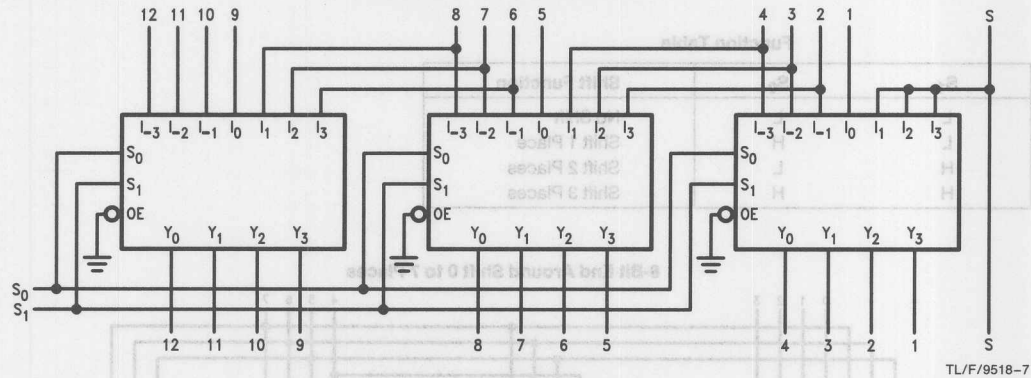
8-Bit End Around Shift 0 to 7 Places



TL/F/9518-6

S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	Shift Function
L	L	L	No Shift
L	L	H	Shift End Around 1
L	H	L	Shift End Around 2
L	H	H	Shift End Around 3
H	L	L	Shift End Around 4
H	L	H	Shift End Around 5
H	H	L	Shift End Around 6
H	H	H	Shift End Around 7

13-Bit Twos Complement Scaler



Function Table

S <sub>1</sub>	S <sub>0</sub>	Scale
L	L ÷ 8	1/8
L	H ÷ 4	1/4
H	L ÷ 2	1/2
H	H No Change	1

Storage Temperature	−65°C to +150°C	TRI-STATE Output	−0.5V to +5.5V
Ambient Temperature under Bias	−55°C to +125°C	Current Applied to Output	
Junction Temperature under Bias	−55°C to +175°C	in LOW State (Max)	twice the rated $I_{OL}$ (mA)
$V_{CC}$ Pin Potential to Ground Pin	−0.5V to +7.0V	<b>Recommended Operating Conditions</b>	
Input Voltage (Note 2)	−0.5V to +7.0V		
Input Current (Note 2)	−30 mA to +5.0 mA		
<b>Note 1:</b> Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.		Free Air Ambient Temperature	
<b>Note 2:</b> Either voltage limit or current limit is sufficient to protect inputs.		Military	−55°C to +125°C
		Commercial	0°C to +70°C
		Supply Voltage	
		Military	+4.5V to +5.5V
		Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	$V_{CC}$	Conditions
			Min	Typ	Max			
$V_{IH}$	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
$V_{IL}$	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
$V_{CD}$	Input Clamp Diode Voltage				−1.2	V	Min	$I_{IN} = -18$ mA
$V_{OH}$	Output HIGH Voltage	54F 10% $V_{CC}$	2.5			V	Min	$I_{OH} = -1$ mA
		54F 10% $V_{CC}$	2.4					$I_{OH} = -3$ mA
		74F 10% $V_{CC}$	2.5					$I_{OH} = -1$ mA
		74F 10% $V_{CC}$	2.4					$I_{OH} = -3$ mA
		74F 5% $V_{CC}$	2.7					$I_{OH} = -1$ mA
		74F 10% $V_{CC}$	2.7					$I_{OH} = -3$ mA
$V_{OL}$	Output LOW Voltage	54F 10% $V_{CC}$			0.5	V	Min	$I_{OL} = 20$ mA
		74F 10% $V_{CC}$			0.5			$I_{OL} = 24$ mA
$I_{IH}$	Input HIGH Current	54F			20.0	$\mu$ A	Max	$V_{IN} = 2.7$ V
		74F			5.0			
$I_{BVI}$	Input HIGH Current Breakdown Test	54F			100	$\mu$ A	Max	$V_{IN} = 7.0$ V
		74F			7.0			
$I_{CEX}$	Output HIGH Leakage Current	54F			250	$\mu$ A	Max	$V_{OUT} = V_{CC}$
		74F			50			
$V_{ID}$	Input Leakage Test	74F	4.75			V	0.0	$I_{ID} = 1.9$ $\mu$ A All Other Pins Grounded
$I_{OD}$	Output Leakage Circuit Current	74F			3.75	$\mu$ A	0.0	$V_{IOD} = 150$ mV All Other Pins Grounded
$I_{IL}$	Input LOW Current				−1.2	mA	Max	$V_{IN} = 0.5$ V
$I_{OZH}$	Output Leakage Current				50	$\mu$ A	Max	$V_{OUT} = 2.7$ V
$I_{OZL}$	Output Leakage Current				−50	$\mu$ A	Max	$V_{OUT} = 0.5$ V
$I_{OS}$	Output Short-Circuit Current		−60		−150	mA	Max	$V_{OUT} = 0$ V
$I_{ZZ}$	Bus Drainage Test				500	$\mu$ A	0.0V	$V_{OUT} = 5.25$ V
$I_{CCH}$	Power Supply Current			34	42	mA	Max	$V_O = \text{HIGH}$
$I_{CCL}$	Power Supply Current			40	57	mA	Max	$V_O = \text{LOW}$
$I_{CCZ}$	Power Supply Current			40	57	mA	Max	$V_O = \text{HIGH Z}$



# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay $I_n$ to $O_n$	3.0	4.5	6.0			3.0	7.0	ns	2-3
$t_{PHL}$		2.5	4.0	5.5			2.5	6.5		
$t_{PLH}$	Propagation Delay $S_n$ to $O_n$	4.0	7.8	10.0			4.0	13.5	ns	2-3
$t_{PHL}$		3.0	6.5	8.5			3.0	9.5		
$t_{PZH}$	Output Enable Time	2.5	5.0	7.0			2.5	8.0		
$t_{PZL}$		4.0	7.0	9.0			4.0	10.0		
$t_{PHZ}$	Output Disable Time	2.0	3.9	5.5			2.0	6.5	ns	2-5
$t_{PLZ}$		2.0	4.0	5.5			2.0	7.5		

Symbol	Parameter	74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
$V_{IH}$	Input HIGH Voltage	2.0			V		Recognized as a HIGH signal
$V_{IL}$	Input LOW Voltage	0.8			V		Recognized as a LOW signal
$V_{CD}$	Input Clamp Diode Voltage	-1.2			V	Min	$I_{in} = -18\text{mA}$
$V_{OH}$	Output HIGH Voltage	2.7	2.7	2.7	V	Min	$I_{OH} = -1\text{mA}$ $I_{OH} = -3\text{mA}$ $I_{OH} = -1\text{mA}$ $I_{OH} = -3\text{mA}$ $I_{OH} = -1\text{mA}$ $I_{OH} = -3\text{mA}$
$V_{OL}$	Output LOW Voltage	0.8	0.8	0.8	V	Min	$I_{OL} = 20\text{mA}$ $I_{OL} = 24\text{mA}$
$I_{IH}$	Input HIGH Current	24F	24F	24F	$\mu\text{A}$	Max	$V_{in} = 2.7\text{V}$
$I_{BI}$	Input HIGH Current Breakdown Test	24F	100	7.0	$\mu\text{A}$	Max	$V_{in} = 7.0\text{V}$
$I_{OEH}$	Output HIGH Leakage Current	24F	280	20	$\mu\text{A}$	Max	$V_{out} = V_{CC}$
$V_{ID}$	Input Leakage Test	24F	4.75		V	0.0	$I_D = 1.8\text{mA}$ All Other Pins Grounded
$I_{OD}$	Output Leakage Current	24F	3.75		$\mu\text{A}$	0.0	$V_{OD} = 180\text{mV}$ All Other Pins Grounded
$I_{IL}$	Input LOW Current	-1.2			mA	Max	$V_{in} = 0.8\text{V}$
$I_{OLH}$	Output Leakage Current	80			$\mu\text{A}$	Max	$V_{out} = 2.7\text{V}$
$I_{OL}$	Output Leakage Current	-80			$\mu\text{A}$	Max	$V_{out} = 0.8\text{V}$
$I_{OSH}$	Output Short-Circuit Current	-80			mA	Max	$V_{out} = 0\text{V}$
$I_{Z}$	Bus Drainage Test	800			$\mu\text{A}$	0.0V	$V_{out} = 3.25\text{V}$
$I_{OSH}$	Power Supply Current	84	42		mA	Max	$V_O = \text{HIGH}$
$I_{OL}$	Power Supply Current	40	27		mA	Max	$V_O = \text{LOW}$
$I_{OCS}$	Power Supply Current	40	27		mA	Max	$V_O = \text{HIGH } Z$



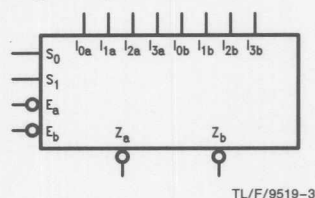
# 54F/74F352 Dual 4-Input Multiplexer

## General Description

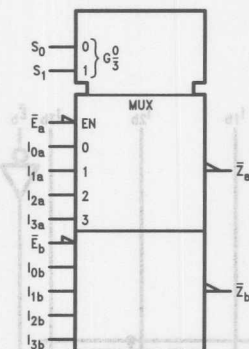
The 'F352 is a very high-speed dual 4-input multiplexer with common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The 'F352 is the functional equivalent of the 'F153 except with inverted outputs.

**Ordering Code:** See Section 5

## Logic Symbols



### IEEE/IEC

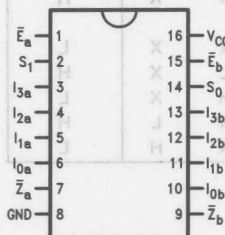


## Features

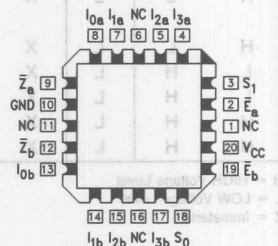
- Inverted version of 'F153
- Separate enables for each multiplexer
- Input clamp diode limits high speed termination effects

## Connection Diagrams

### Pin Assignment for DIP, SOIC and Flatpak



### Pin Assignment for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$I_{0a}-I_{3a}$	Side A Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$I_{0b}-I_{3b}$	Side B Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$S_0-S_1$	Common Select Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\bar{E}_a$	Side A Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\bar{E}_b$	Side B Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\bar{Z}_a, \bar{Z}_b$	Multiplexer Outputs (Inverted)	50/33.3	-1 mA/20 mA

## Functional Description

The 'F352 is a dual 4-input multiplexer. It selects two bits of data from up to four sources under the control of the common Select inputs ( $S_0, S_1$ ). The two 4-input multiplexer circuits have individual active LOW Enables ( $\bar{E}_a, \bar{E}_b$ ) which can be used to strobe the outputs independently. When the Enables ( $\bar{E}_a, \bar{E}_b$ ) are HIGH, the corresponding outputs ( $\bar{Z}_a, \bar{Z}_b$ ) are forced HIGH.

The logic equations for the outputs are shown below:

$$\bar{Z}_a = \bar{E}_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

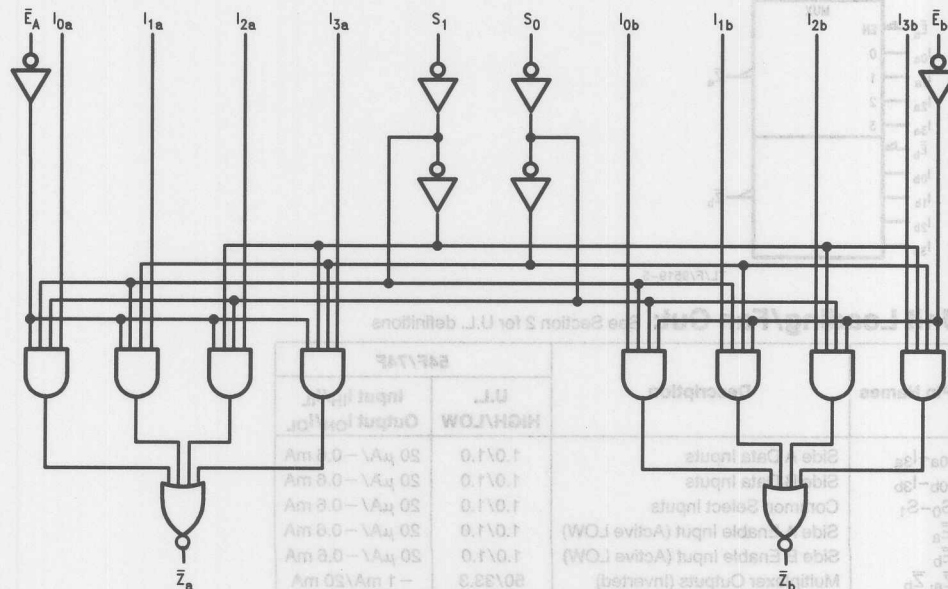
$$\bar{Z}_b = \bar{E}_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

## Truth Table

Select Inputs		Inputs (a or b)						Output
$S_0$	$S_1$	$\bar{E}$	$I_0$	$I_1$	$I_2$	$I_3$		$\bar{Z}$
X	X	H	X	X	X	X		H
L	L	L	L	X	X	X		H
L	L	L	H	X	X	X		L
H	L	L	X	L	X	X		H
H	L	L	X	H	X	X		L
L	H	L	X	X	L	X		H
L	H	L	X	X	H	X		L
H	H	L	X	X	X	L		H
H	H	L	X	X	X	H		L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

The 'F352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is as a function generator. The 'F352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	−55°C to +125°C
Military	0°C to +70°C
Commercial	
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	

**DC Electrical Characteristics**

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5			V	Min	I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.5					I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>			0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>			0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F			20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F			100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F			250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current				−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60		−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current			9.3	14	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			13.3	20	mA	Max	V <sub>O</sub> = LOW

Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_n$ to $Z_n$	4.0 3.5	8.0 6.5	11.0 8.5	3.5 3.0	14.0 11.0	3.5 3.0	12.5 9.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{E}_n$ to $Z_n$	3.0 3.0	4.5 5.0	6.0 7.0	2.5 2.5	8.0 9.0	2.5 2.5	7.0 8.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $I_n$ to $Z_n$	2.0 1.3	5.2 2.5	7.0 4.0	2.0 1.0	9.0 5.0	2.0 1.0	8.0 4.5	ns	2-3

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Note 3: Current Applied to Output in LOW State (Max)

## DC Electrical Characteristics

Symbol	Parameter	Units		Conditions
		Min	Max	
$V_{IH}$	Input HIGH Voltage	2.0		Recognized as a HIGH Signal
$V_{IL}$	Input LOW Voltage	0.8		Recognized as a LOW Signal
$V_{CC}$	Input Clamp Diode Voltage	-1.5		$I_{IH} = -18\text{ mA}$
$V_{OH}$	Output HIGH Voltage 54F 10% $V_{CC}$ 74F 10% $V_{CC}$ 74F 5% $V_{CC}$	2.8 2.8 2.7		$I_{OH} = -1\text{ mA}$ $I_{OH} = -1\text{ mA}$ $I_{OH} = -1\text{ mA}$
$V_{OL}$	Output LOW Voltage 54F 10% $V_{CC}$ 74F 10% $V_{CC}$	0.8 0.8		$I_{OL} = 20\text{ mA}$ $I_{OL} = 20\text{ mA}$
$I_{IH}$	Input HIGH Current 54F 74F	20.0 2.0		$V_{IH} = 2.7\text{V}$
$I_{OIH}$	Input HIGH Current 54F 74F	100 7.0		$V_{IH} = 7.0\text{V}$
$I_{OEX}$	Output HIGH Leakage Current 54F 74F	250 20		$V_{OUT} = V_{CC}$
$V_{ID}$	Input Leakage Test	4.75		$I_D = 1.8\text{ }\mu\text{A}$ All Other Pins Grounded
$I_{OD}$	Output Leakage Current 54F	3.75		$V_{OD} = 150\text{ mV}$ All Other Pins Grounded
$I_{IL}$	Input LOW Current	-0.8		$V_{IH} = 0.5\text{V}$
$I_{OS}$	Output Short-Circuit Current	-80		$V_{OUT} = 0\text{V}$
$I_{OCH}$	Power Supply Current	0.3	14	$V_O = \text{HIGH}$
$I_{OCL}$	Power Supply Current	13.3	20	$V_O = \text{LOW}$



**54F/74F353**

## Dual 4-Input Multiplexer with TRI-STATE® Outputs

### General Description

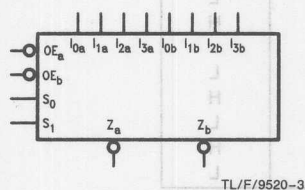
The 'F353 is a dual 4-input multiplexer with TRI-STATE outputs. It can select two bits of data from four sources using common Select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ( $\overline{OE}$ ) inputs, allowing the outputs to interface directly with bus-oriented systems.

### Features

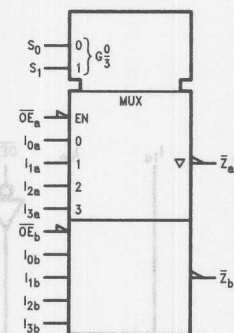
- Inverted version of 'F253
- Multifunction capability
- Separate enables for each multiplexer

**Ordering Code:** See Section 5

### Logic Symbols



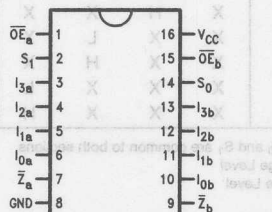
IEEE/IEC



TL/F/9520-5

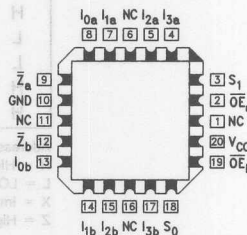
### Connection Diagrams

**Pin Assignment for DIP, SOIC and Flatpak**



TL/F/9520-1

**Pin Assignment for LCC**



TL/F/9520-2

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$I_{0a}-I_{3a}$	Side A Data Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
$I_{0b}-I_{3b}$	Side B Data Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
$S_0, S_1$	Common Select Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{OE}_a$	Side A Output Enable Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{OE}_b$	Side B Output Enable Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$Z_a, Z_b$	TRI-STATE Outputs (Inverted)	150/40 (33.3)	-3 mA/24 mA (20 mA)



## Functional Description

The 'F353 contains two identical 4-input multiplexers with TRI-STATE outputs. They select two bits from four sources selected by common Select inputs ( $S_0$ ,  $S_1$ ). The 4-input multiplexers have individual Output Enable ( $\overline{OE}_a$ ,  $\overline{OE}_b$ ) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$\overline{Z}_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

## Truth Table

Select Inputs		Data Inputs				Output Enable	Output
$S_0$	$S_1$	$I_0$	$I_1$	$I_2$	$I_3$	$\overline{OE}$	$\overline{Z}$
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Address inputs  $S_0$  and  $S_1$  are common to both sections.

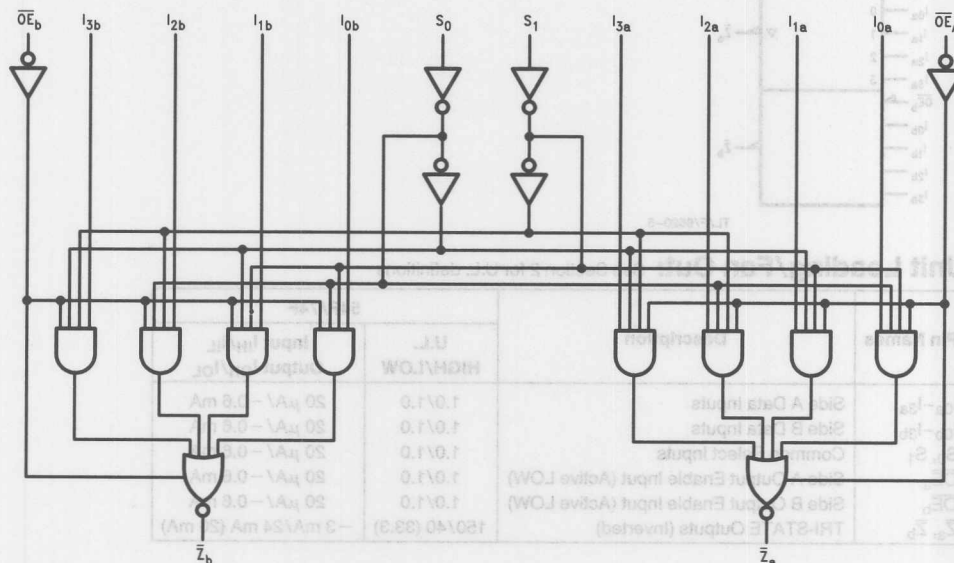
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

TL/F/9520-4

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

Voltage Applied to Output in HIGH State (with V<sub>CC</sub> = 0V)

Standard Output  
TRI-STATE Output

Current Applied to Output in LOW State (Max)

-0.5V to V<sub>CC</sub>  
-0.5V to +5.5V

twice the rated I<sub>OL</sub> (mA)

## Recommended Operating Conditions

Free Air Ambient Temperature

Military  
Commercial

-55°C to +125°C  
0°C to +70°C

Supply Voltage

Military  
Commercial

+4.5V to +5.5V  
+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5			V	Min	I <sub>OH</sub> = -1 mA
		54F 10% V <sub>CC</sub>	2.4					I <sub>OH</sub> = -3 mA
		74F 10% V <sub>CC</sub>	2.5					I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.4					I <sub>OH</sub> = -3 mA
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = -3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>			0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>			0.5			I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F			20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F			100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F			250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current				-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current				50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current				-50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test				500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current			9.3	14	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			13.3	20	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current			15.0	23	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	4.0	8.0	11.0	3.5	14.0	3.5	12.5	ns	2-3
t <sub>PHL</sub>	S <sub>n</sub> to Z <sub>n</sub>	3.5	6.5	8.5	3.0	11.0	3.0	9.5		
t <sub>PLH</sub>	Propagation Delay	3.0	5.2	7.0	3.0	9.0	3.0	8.0	ns	2-3
t <sub>PHL</sub>	I <sub>n</sub> to Z <sub>n</sub>	1.3	2.5	4.0	1.0	5.0	1.0	4.5		
t <sub>pZH</sub>	Output Enable Time	2.5	5.5	8.0	2.0	10.5	2.0	9.0	ns	2-5
t <sub>pZL</sub>		3.0	6.0	8.0	2.5	10.5	2.5	9.0		
t <sub>PHZ</sub>	Output Disable Time	2.0	3.7	5.0	2.0	7.0	2.0	6.0		
t <sub>PLZ</sub>		2.0	4.4	6.0	2.0	8.0	2.0	7.0		



## 54F/74F365

### Hex Buffer/Driver with TRI-STATE® Outputs

#### General Description

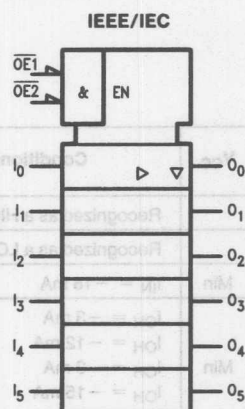
The 'F365 is a hex buffer and line driver designed to be employed as a memory and address driver, clock driver and bus-oriented transmitter/receiver.

#### Features

- TRI-STATE buffer outputs
- Outputs sink 64 mA
- Bus-oriented

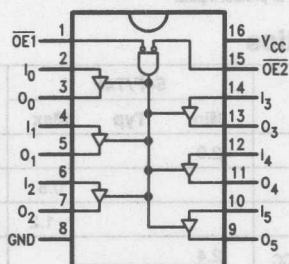
**Ordering Code:** See Section 5

#### Logic Symbol



TL/F/9522-4

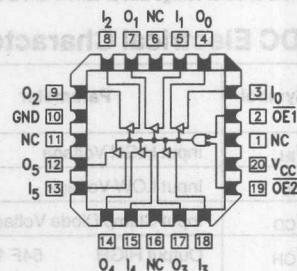
#### Pin Assignment for DIP, SOIC and Flatpak



TL/F/9522-1

#### Connection Diagrams

#### Pin Assignment for LCC



TL/F/9522-2

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{OE}_1, \overline{OE}_2$	Output Enable Input (Active LOW)	1.0/0.033	20 $\mu$ A/20 $\mu$ A
$I_n$ $O_n$	Inputs Outputs	1.0/0.033 600/106.6 (80)	20 $\mu$ A/20 $\mu$ A -12 mA/64 mA (48 mA)

Function Table

Inputs		Output	
$\overline{OE}_1$	$\overline{OE}_2$	I	O
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

L = LOW Voltage Level  
H = HIGH Voltage Level  
X = Immaterial  
Z = High Impedance

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	-0.5V to V <sub>CC</sub>
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	-55°C to +125°C
Military	0°C to +70°C
Commercial	
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.4 2.0 2.4 2.0 2.7		V	Min	I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -12 mA I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -15 mA I <sub>OH</sub> = -3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.55 0.55	V	Min	I <sub>OL</sub> = 48 mA I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current			20	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			100	μA	0.0	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current			-20	μA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			-50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-100		-225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CEx</sub>	Output HIGH Leakage Current			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current		25	35	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		44	62	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		35	48	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	2.5	4.6	6.5	2.0	7.0	2.0	7.0	ns	2-3
$t_{PHL}$	$I_n$ to $O_n$	2.5	4.9	7.0	2.0	7.0	2.0	7.5		
$t_{PZH}$	Enable Time	2.5	5.1	9.5	2.0	8.5	2.5	10.0	ns	2-5
$t_{PZL}$		2.5	5.7	9.0	2.0	8.5	2.5	9.5		
$t_{PHZ}$	Disable Time	2.0	3.6	6.5	1.5	6.5	2.0	7.0	ns	2-5
$t_{PLZ}$		2.0	4.4	6.5	1.5	9.0	2.0	7.0		




**54F/74F366•54F/74F368**

# Hex Inverter Buffer with TRI-STATE® Outputs

## Features

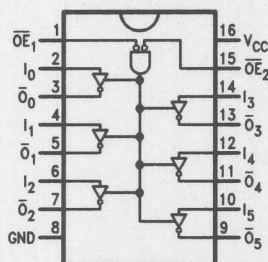
- TRI-STATE buffer outputs sink 64 mA
- High-speed
- Bus-oriented
- High impedance npn base inputs for reduced loading

**Ordering Code:** See Section 5

## Connection Diagrams

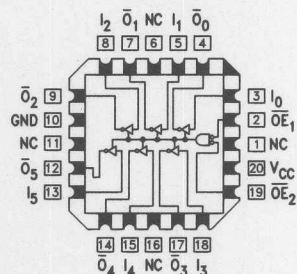
**'F366**

Pin Assignment  
for DIP, SOIC and Flatpak



TL/F/9521-2

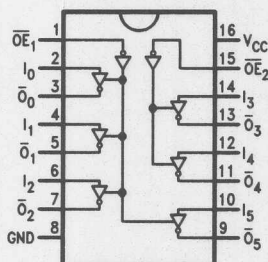
Pin Assignment  
for LCC



TL/F/9521-1

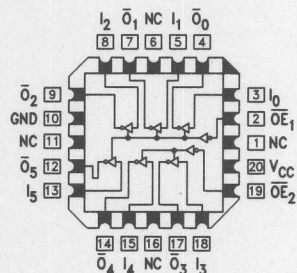
**'F368**

Pin Assignment  
for DIP, SOIC and Flatpak



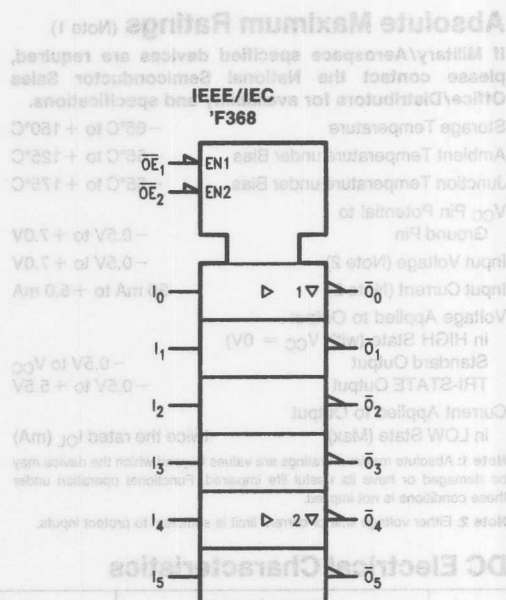
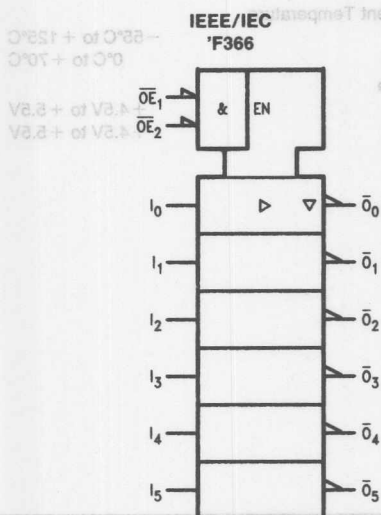
TL/F/9521-4

Pin Assignment  
for LCC



TL/F/9521-3

## Logic Symbols



## Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{OE}_1, \overline{OE}_2$	Output Enable Input (Active LOW)	1.0/0.033	20 $\mu$ A / -20 $\mu$ A
$I_n$	Input	1.0/0.033	20 $\mu$ A / -20 $\mu$ A
$O_n, \overline{O}_n$	Outputs	600/106.6 (80)	-12 mA/64 mA (48 mA)

## Function Tables

'F366

Inputs		Output	
$\overline{OE}_1$	$\overline{OE}_2$	I	$\overline{O}$
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

'F368

Inputs		Output	
$\overline{OE}$	I	$\overline{O}$	
L	L	H	
L	H	L	
H	X	Z	

L = LOW Voltage Level  
H = HIGH Voltage Level  
X = Immaterial  
Z = High Impedance

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output	−0.5V to +5.5V
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

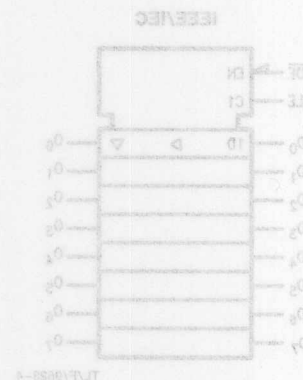
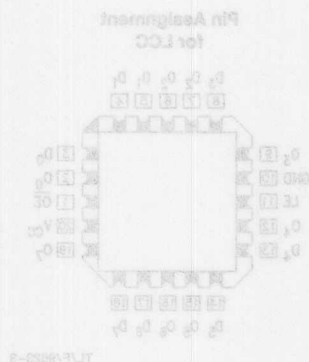
Free Air Ambient Temperature	−55°C to +125°C
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage		−1.2		V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.0		V	Min	I <sub>OH</sub> = −12 mA
		74F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = −15 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.55	V	Min	I <sub>OL</sub> = 48 mA
		74F 10% V <sub>CC</sub>		0.55			I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current			20	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			100	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current			−20	μA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	−100		−225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CEX</sub>	Output HIGH Leakage Current			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current		20	25	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		49	62	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		35	48	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay	2.5 1.0	4.0 1.8	6.5 5.0			2.0 1.0	7.5 5.5	ns	2-3
$t_{PZH}$ $t_{PZL}$	Enable Time ('F366)	2.5 2.5	4.2 4.2	9.5 9.0			2.5 2.5	10.0 9.5	ns	2-5
$t_{PZH}$ $t_{PZL}$	Enable Time ('F368)	2.5 3.0	4.2 5.6	7.5 8.5			2.0 3.0	8.5 9.0	ns	2-5
$t_{PHZ}$ $t_{PLZ}$	Disable Time	2.0 2.0	3.3 4.1	6.5 6.5			2.0 2.0	7.0 7.0	ns	2-5



Unit Loading Fan Out: See Section 3 for U.L. Definitions

Pin Name	Description	TLV1622	
		U.L. HIGH/LOW	Input/Output Output/Load
$O_1$ - $O_7$	TRI-STATE Latch Outputs	1.0/1.0 (2.3)	-3 mA/24 mA (50 mA)
$O_8$	Output Enable Input (Active LOW)	1.0/1.0	20 $\mu\text{A}$ /-0.6 mA
$LE$	Latch Enable Input (Active HIGH)	1.0/1.0	20 $\mu\text{A}$ /-0.6 mA
$O_9$ - $O_7$	Data Inputs	1.0/1.0	20 $\mu\text{A}$ /-0.6 mA


**54F/74F373**

## Octal Transparent Latch with TRI-STATE® Outputs

### General Description

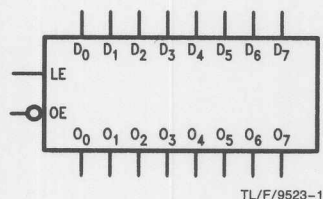
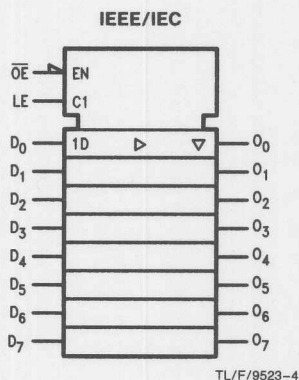
The 'F373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH the bus output is in the high impedance state.

### Features

- Eight latches in a single package
- TRI-STATE outputs for bus interfacing
- Guaranteed 4000V minimum ESD protection

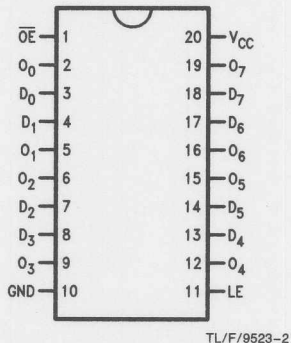
**Ordering Code:** See Section 5

### Logic Symbols

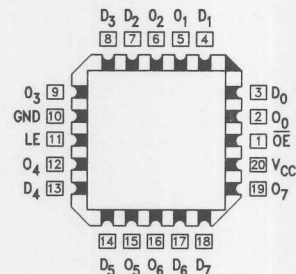


### Connection Diagrams

Pin Assignment  
for DIP, SOIC and Flatpak



Pin Assignment  
for LCC



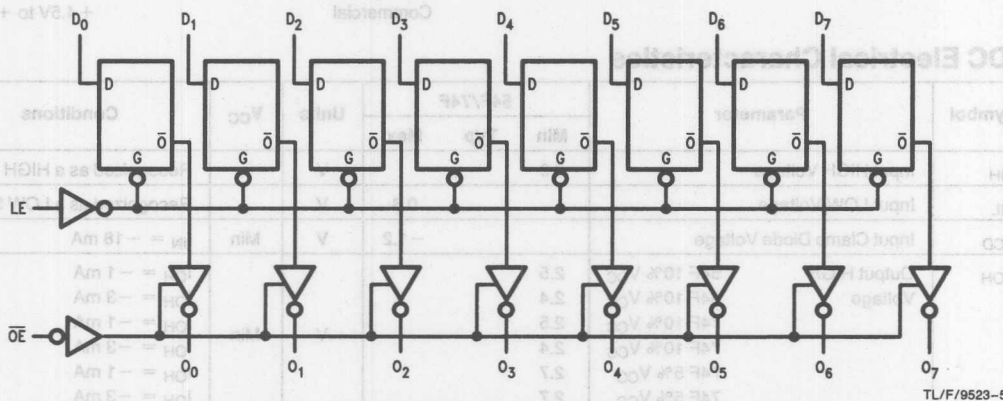
**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
D <sub>0</sub> -D <sub>7</sub>	Data Inputs	1.0/1.0	20 $\mu$ A / -0.6 mA
LE	Latch Enable Input (Active HIGH)	1.0/1.0	20 $\mu$ A / -0.6 mA
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A / -0.6 mA
O <sub>0</sub> -O <sub>7</sub>	TRI-STATE Latch Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

## Functional Description

The 'F373 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the buffers are in the bi-state mode. When  $\overline{OE}$  is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Truth Table

Inputs		Output	
LE	$\overline{OE}$	$D_n$	$O_n$
H	L	H	H
H	L	L	L
L	L	X	$O_n$ (no change)
X	H	X	Z

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance State



## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

Voltage Applied to Output  
in HIGH State (with V<sub>CC</sub> = 0V)  
Standard Output -0.5V to V<sub>CC</sub>  
TRI-STATE Output -0.5V to +5.5V  
Current Applied to Output  
in LOW State (Max) twice the rated I<sub>OL</sub> (mA)  
ESD Last Passing Voltage (Min) 4000V

## Recommended Operating Conditions

Free Air Ambient Temperature	Military -55°C to +125°C Commercial 0°C to +70°C
Supply Voltage	Military +4.5V to +5.5V Commercial +4.5V to +5.5V

## DC Electrical Characteristics

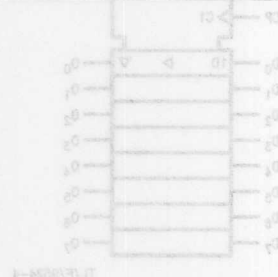
Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5			V	Min	I <sub>OH</sub> = -1 mA
		54F 10% V <sub>CC</sub>	2.4					I <sub>OH</sub> = -3 mA
		74F 10% V <sub>CC</sub>	2.5					I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.4					I <sub>OH</sub> = -3 mA
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = -3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>			0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>			0.5			I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F			20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F			100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F			250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current				-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current				50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current				-50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test				500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCZ</sub>	Power Supply Current			38	55	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	3.0	5.3	7.0	3.0	8.5	3.0	8.0	ns	2-3
$t_{PHL}$	$D_n$ to $O_n$	2.0	3.7	5.0	2.0	7.0	2.0	6.0		
$t_{PLH}$	Propagation Delay	5.0	9.0	11.5	5.0	15.0	5.0	13.0	ns	2-3
$t_{PHL}$	LE to $O_n$	3.0	5.2	7.0	3.0	8.5	3.0	8.0		
$t_{PZH}$	Output Enable Time	2.0	5.0	11.0	2.0	13.5	2.0	12.0	ns	2-5
$t_{PZL}$		2.0	5.6	7.5	2.0	10.0	2.0	8.5		
$t_{PHZ}$	Output Disable Time	1.5	4.5	6.5	1.5	10.0	1.5	7.5	ns	2-5
$t_{PLZ}$		1.5	3.8	5.0	1.5	7.0	1.5	6.0		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	2.0		2.0		2.0		ns	2-6
$t_s(\text{L})$	$D_n$ to LE	2.0		2.0		2.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	3.0		3.0		3.0			
$t_h(\text{L})$	$D_n$ to LE	3.0		4.0		3.0			
$t_w(\text{H})$	LE Pulse Width, HIGH	6.0		6.0		6.0		ns	2-4



Pin	Description	U.L.	Input
16	TRI-STATE Outputs	1.0V/0	Output
15	TRI-STATE Enable Input (Active LOW)	1.0V/0	Input
14	TRI-STATE Enable Input (Active LOW)	1.0V/0	Input
13	TRI-STATE Enable Input (Active LOW)	1.0V/0	Input
12	TRI-STATE Enable Input (Active LOW)	1.0V/0	Input
11	TRI-STATE Enable Input (Active LOW)	1.0V/0	Input
10	TRI-STATE Enable Input (Active LOW)	1.0V/0	Input
9	TRI-STATE Enable Input (Active LOW)	1.0V/0	Input
8	TRI-STATE Enable Input (Active LOW)	1.0V/0	Input
7	TRI-STATE Enable Input (Active LOW)	1.0V/0	Input
6	TRI-STATE Enable Input (Active LOW)	1.0V/0	Input
5	TRI-STATE Enable Input (Active LOW)	1.0V/0	Input
4	TRI-STATE Enable Input (Active LOW)	1.0V/0	Input
3	TRI-STATE Enable Input (Active LOW)	1.0V/0	Input
2	TRI-STATE Enable Input (Active LOW)	1.0V/0	Input
1	TRI-STATE Enable Input (Active LOW)	1.0V/0	Input


**54F/74F374**

## Octal D-Type Flip-Flop with TRI-STATE® Outputs

### General Description

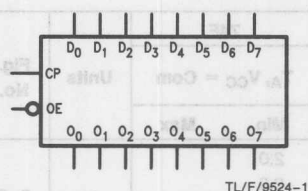
The 'F374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ( $\overline{OE}$ ) are common to all flip-flops.

### Features

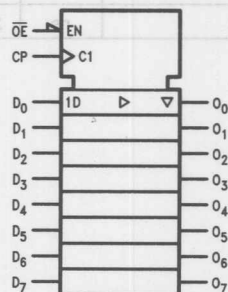
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

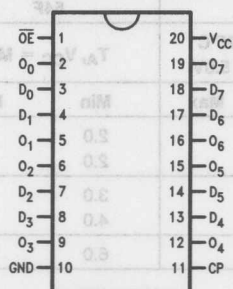
### Logic Symbols



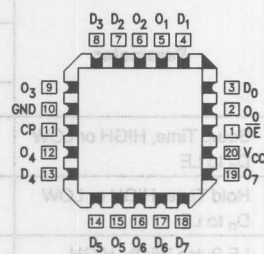
IEEE/IEC



Pin Assignment  
for DIP, SOIC and Flatpak



Pin Assignment  
for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$D_0$ - $D_7$	Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$Q_0$ - $Q_7$	TRI-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)



Storage Temperature  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$   
Ambient Temperature under Bias  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
Junction Temperature under Bias  $-55^{\circ}\text{C}$  to  $+175^{\circ}\text{C}$

$V_{CC}$  Pin Potential to Ground Pin  $-0.5\text{V}$  to  $+7.0\text{V}$

Input Voltage (Note 2)  $-0.5\text{V}$  to  $+7.0\text{V}$

Input Current (Note 2)  $-30\text{ mA}$  to  $+5.0\text{ mA}$

Voltage Applied to Output in HIGH State (with  $V_{CC} = 0\text{V}$ )  
Standard Output  $-0.5\text{V}$  to  $V_{CC}$   
TRI-STATE Output  $-0.5\text{V}$  to  $+5.5\text{V}$

Current Applied to Output in LOW State (Max) twice the rated  $I_{OL}$  (mA)

ESD Last Passing Voltage (Min) 4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	$V_{CC}$	Conditions
		Min	Typ	Max			
$V_{IH}$	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
$V_{IL}$	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
$V_{CD}$	Input Clamp Diode Voltage			-1.2	V	Min	$I_{IN} = -18\text{ mA}$
$V_{OH}$	Output HIGH Voltage	54F 10% $V_{CC}$	2.5		V	Min	$I_{OH} = -1\text{ mA}$
		54F 10% $V_{CC}$	2.4				$I_{OH} = -3\text{ mA}$
		74F 10% $V_{CC}$	2.5				$I_{OH} = -1\text{ mA}$
		74F 10% $V_{CC}$	2.4				$I_{OH} = -3\text{ mA}$
		74F 5% $V_{CC}$	2.7				$I_{OH} = -1\text{ mA}$
		74F 5% $V_{CC}$	2.7				$I_{OH} = -3\text{ mA}$
$V_{OL}$	Output LOW Voltage	54F 10% $V_{CC}$		0.5	V	Min	$I_{OL} = 20\text{ mA}$
		74F 10% $V_{CC}$		0.5			$I_{OL} = 24\text{ mA}$
$I_{IH}$	Input HIGH Current	54F		20.0	$\mu\text{A}$	Max	$V_{IN} = 2.7\text{V}$
		74F		5.0			
$I_{BVI}$	Input HIGH Current Breakdown Test	54F		100	$\mu\text{A}$	Max	$V_{IN} = 7.0\text{V}$
		74F		7.0			
$I_{CEX}$	Output HIGH Leakage Current	54F		250	$\mu\text{A}$	Max	$V_{OUT} = V_{CC}$
		74F		50			
$V_{ID}$	Input Leakage Test	74F	4.75		V	0.0	$I_{ID} = 1.9\text{ }\mu\text{A}$ All Other Pins Grounded
$I_{OD}$	Output Leakage Circuit Current	74F		3.75	$\mu\text{A}$	0.0	$V_{IOD} = 150\text{ mV}$ All Other Pins Grounded
$I_{IL}$	Input LOW Current			-0.6	mA	Max	$V_{IN} = 0.5\text{V}$
$I_{OZH}$	Output Leakage Current			50	$\mu\text{A}$	Max	$V_{OUT} = 2.7\text{V}$
$I_{OZL}$	Output Leakage Current			-50	$\mu\text{A}$	Max	$V_{OUT} = 0.5\text{V}$
$I_{OS}$	Output Short-Circuit Current		-60	-150	mA	Max	$V_{OUT} = 0\text{V}$
$I_{ZZ}$	Bus Drainage Test			500	$\mu\text{A}$	0.0V	$V_{OUT} = 5.25\text{V}$
$I_{CCZ}$	Power Supply Current		55	86	mA	Max	$V_O = \text{HIGH Z}$

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	100	140		60		70		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	4.0	6.5	8.5	4.0	10.5	4.0	10.0	ns	2-3
$t_{\text{PHL}}$	CP to $O_n$	4.0	6.5	8.5	4.0	11.0	4.0	10.0		
$t_{\text{PZH}}$	Output Enable Time	2.0	9.0	11.5	2.0	14.0	2.0	12.5	ns	2-5
$t_{\text{PZL}}$		2.0	5.8	7.5	2.0	10.0	2.0	8.5		
$t_{\text{PHZ}}$	Output Disable Time	2.0	5.3	7.0	2.0	8.0	2.0	8.0		
$t_{\text{PLZ}}$		1.5	4.3	5.5	1.5	7.5	1.5	6.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	2.0		2.5		2.0		ns	2-6
$t_s(\text{L})$	$D_n$ to CP	2.0		2.0		2.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0		2.0		2.0			
$t_h(\text{L})$	$D_n$ to CP	2.0		2.5		2.0			
$t_w(\text{H})$	CP Pulse Width	7.0		7.0		7.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	6.0		6.0		6.0			




**54F/74F377**

## Octal D Flip-Flop with Clock Enable

### General Description

The 'F377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (CE) is LOW.

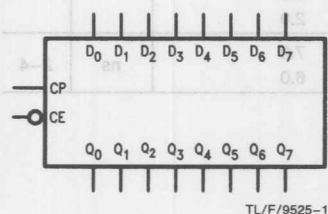
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The CE input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

### Features

- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- See 'F273 for master reset version
- See 'F373 for transparent latch version
- See 'F374 for TRI-STATE® version
- Guaranteed 4000V minimum ESD protection

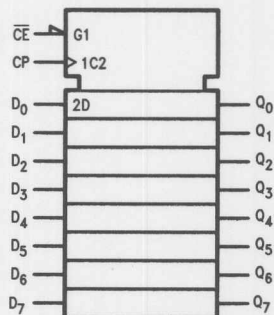
### Ordering Code: See Section 5

### Logic Symbols



TL/F/9525-1

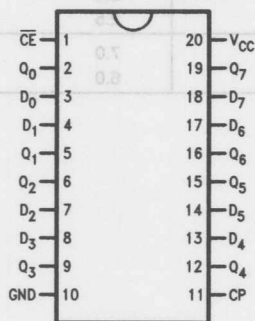
#### IEEE/IEC



TL/F/9525-4

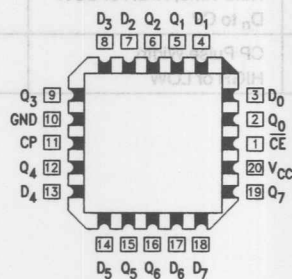
### Connection Diagrams

#### Pin Assignment for DIP, SOIC and Flatpak



TL/F/9525-2

#### Pin Assignment for LCC



TL/F/9525-3

# Unit Loading/Fan Out: See Section 2 for U.L. definitions

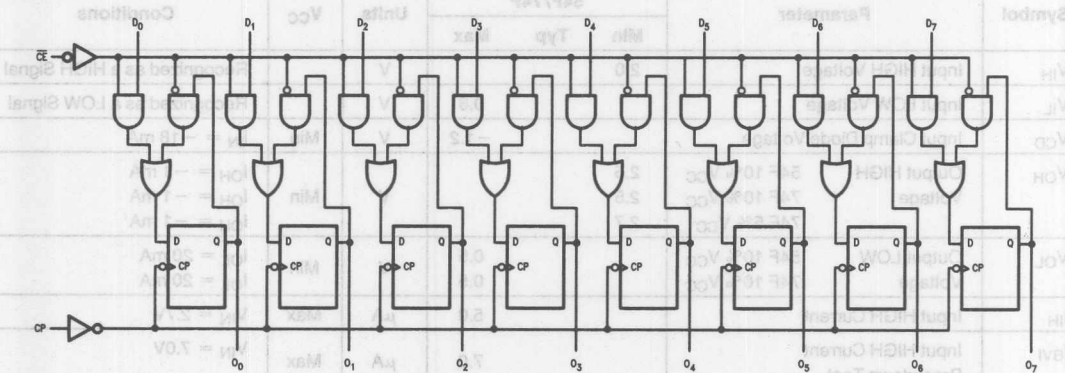
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$D_0-D_7$	Data Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{CE}$	Clock Enable (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
CP	Clock Pulse Input	1.0/1.0	20 $\mu A$ / -0.6 mA
$Q_0-Q_7$	Data Outputs	50/33.3	-1 mA / 20 mA

Mode Select-Function Table

Operating Mode	Inputs			Output
	CP	$\overline{CE}$	$D_n$	$Q_n$
Load "1"		L	h	H
Load "0"		L	L	L
Hold (Do Nothing)		h	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level  
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition  
L = LOW Voltage Level  
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition  
X = Immaterial  
 = LOW-to-HIGH Clock Transition

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

# Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA


Voltage Applied to Output  
in HIGH State (with V<sub>CC</sub> = 0V)  
Standard Output  
TRI-STATE Output

Current Applied to Output  
in LOW State (Max) twice the rated I<sub>OL</sub> (mA)  
ESD Last Passing Voltage (Min) 4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

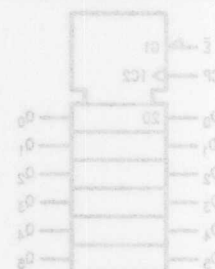
## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.5 2.7		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>ID</sub> = 150 mV All Other Pins Grounded
I <sub>CCH</sub> I <sub>CCL</sub>	Power Supply Current		35 44	46 56	mA	Max	CP =  D <sub>n</sub> = $\overline{\text{MR}}$ = HIGH

Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{Max}}$	Maximum Clock Frequency	130			85		105		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	3.0		7.0	2.0	8.5	2.5	7.5	ns	2-4
$t_{\text{PHL}}$	CP to $Q_n$	4.0		9.0	3.0	10.5	3.5	9.0		

### AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	3.0		3.5		3.0		ns	2-6
$t_s(\text{L})$	$D_n$ to CP	3.5		4.0		3.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0.5		1.0		0.5		ns	2-6
$t_h(\text{L})$	$D_n$ to CP	1.0		1.0		1.0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	4.1		4.0		4.1		ns	2-6
$t_s(\text{L})$	$\overline{\text{CE}}$ to CP	3.5		5.0		4.0			
$t_h(\text{H})$	Hold Time, HIGH to LOW	0.5		1.5		0.5		ns	2-6
$t_h(\text{L})$	$\overline{\text{CE}}$ to CP	2.0		2.5		2.0			
$t_w(\text{H})$	Clock Pulse Width, HIGH or LOW	6.0		5.0		6.0		ns	2-4
$t_w(\text{L})$		6.0		5.0		6.0			



Pin Name	Description	U.L.	
		HIGH/LOW	Input/Output
$\overline{\text{CE}}$	Enable Input (Active LOW)	1.0V/1.0	20 $\mu\text{A}$ / -0.8 mA
$D_0-D_3$	Data Inputs	1.0V/1.0	20 $\mu\text{A}$ / -0.8 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0V/1.0	20 $\mu\text{A}$ / -0.8 mA
$Q_0-Q_3$	Outputs	50/50	-1 mA/20 mA



## 54F/74F378

### Parallel D Register with Enable

#### General Description

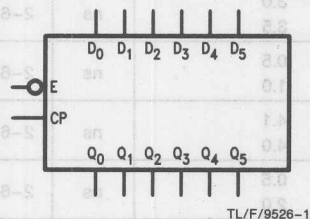
The 'F378 is a 6-bit register with a buffered common Enable. This device is similar to the 'F174, but with common Enable rather than common Master Reset.

#### Features

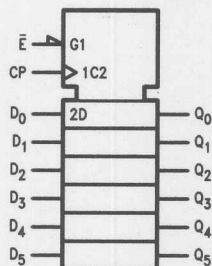
- 6-bit high-speed parallel register
- Positive edge-triggered D-type inputs
- Fully buffered common clock and enable inputs
- Input clamp diodes limit high-speed termination effects
- Full TTL and CMOS compatible

**Ordering Code:** See Section 5

#### Logic Symbols

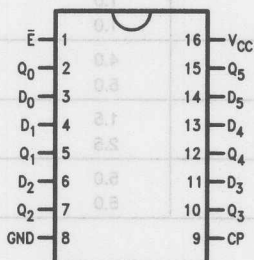


IEEE/IEC

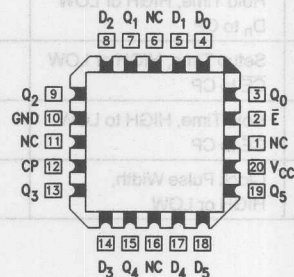


#### Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak



Pin Assignment  
for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\bar{E}$	Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$D_0$ - $D_5$	Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$Q_0$ - $Q_5$	Outputs	50/33.3	-1 mA/20 mA

## Functional Description

The 'F378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ( $\bar{E}$ ) inputs are common to all flip-flops.

When the  $\bar{E}$  input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the  $\bar{E}$  input is HIGH the register will retain the present data independent of the CP input.

## Truth Table

Inputs		Output	
$\bar{E}$	CP	$D_n$	$Q_n$
H	—	X	No Change
L	—	H	H
L	—	L	L

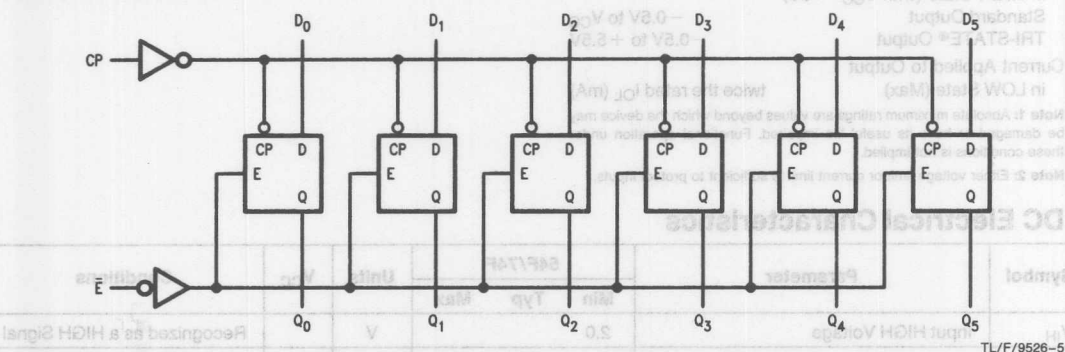
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

— = LOW-to-HIGH Clock Transition

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Symbol	Parameter	Unit	Min	Typ	Max
$V_{CC}$	Input/Output Voltage	V	-1.5		
$V_{OH}$	Output HIGH Voltage	V		2.5	2.5
$V_{OL}$	Output LOW Voltage	V		0.5	0.5
$I_{IH}$	Input HIGH Current	$\mu A$		20.0	5.0
$I_{IL}$	Input LOW Current	$\mu A$		100	7.0
$I_{OZ}$	Output Short-Circuit Current	$\mu A$		250	80
$V_{IP}$	Input Leakage Test	V		4.75	
$I_{OP}$	Output Leakage Current	$\mu A$		3.75	
$I_{IL}$	Input LOW Current	$\mu A$		-0.8	
$I_{OS}$	Output Short-Circuit Current	$\mu A$		-120	
$I_{CC}$	Power Supply Current	$\mu A$		30	



## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
---	----------------

Input Voltage (Note 2)	-0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	-30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	-0.5V to V <sub>CC</sub>
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5			V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5					I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>			0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>			0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F			20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F			5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F			100	μA	Max	V <sub>IN</sub> = 7.0V
		74F			7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F			50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current				-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCL</sub>	Power Supply Current			30	45	mA	Max	V <sub>O</sub> = LOW

## Recommended Operating Conditions

Free Air Ambient Temperature

Military -55°C to +125°C

Commercial 0°C to +70°C

Supply Voltage

Military +4.5V to +5.5V

Commercial +4.5V to +5.5V

Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{pF}$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Input Frequency	80	100		70		80		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay CP to $Q_n$	3.0	5.5	7.5	3.0	10.0	3.0	8.5	ns	2-3
$t_{\text{PHL}}$		3.5	6.0	8.5	3.5	10.5	3.5	9.5		

### AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	4.0		5.0		4.0		ns	2-6
$t_s(\text{L})$	$D_n$ to CP	4.0		5.0		4.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		2.0		0		ns	2-6
$t_h(\text{L})$	$D_n$ to CP	0		2.0		0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	6.0		4.5		6.0		ns	2-6
$t_s(\text{L})$	$\bar{E}$ to CP	10.0		13.0		10.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		0		0		ns	2-4
$t_h(\text{L})$	$\bar{E}$ to CP	0		0		0			
$t_w(\text{H})$	CP Pulse Width	4.0		5.0		4.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	6.0		7.5		6.0			

Pin Name	Description	U.L.	Input High/Low
$\bar{E}$	Enable Input (Active LOW)	1.0/1.0	20 $\mu\text{A}$ - 0.8 mA
$D_0$ - $D_3$	Data Inputs	1.0/1.0	20 $\mu\text{A}$ - 0.8 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu\text{A}$ - 0.8 mA
$Q_0$ - $Q_3$	Flip-Flop Outputs	80/83.3	-1 mA/20 mA
$\bar{Q}_0$ - $\bar{Q}_3$	Complement Outputs	80/83.3	-1 mA/20 mA



## 54F/74F379

### Quad Parallel Register with Enable

#### General Description

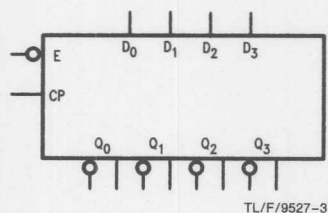
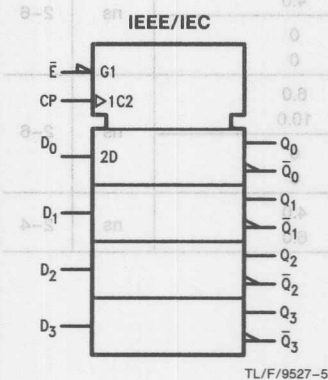
The 'F379 is a 4-bit register with buffered common Enable. This device is similar to the 'F175 but features the common Enable rather than common Master Reset.

#### Features

- Edge triggered D-type inputs
- Buffered positive edge-triggered clock
- Buffered common enable input
- True and complement outputs
- Guaranteed 4000V minimum ESD protection

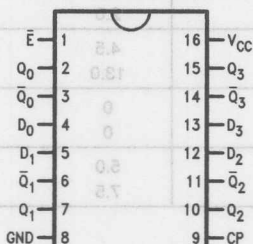
**Ordering Code:** See Section 5

#### Logic Symbols

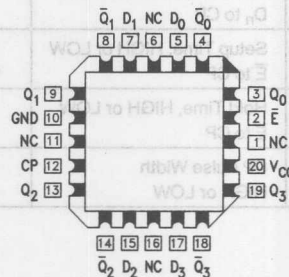


#### Connection Diagrams

Pin Assignment  
DIP, SOIC and Flatpak



Pin Assignment  
for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\bar{E}$	Enable Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$D_0-D_3$	Data Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu A$ / -0.6 mA
$Q_0-Q_3$	Flip-Flop Outputs	50/33.3	-1 mA/20 mA
$\bar{Q}_0-\bar{Q}_3$	Complement Outputs	50/33.3	-1 mA/20 mA

## Functional Description

The 'F379 consists of four edge-triggered D-Type flip-flops with individual D inputs and Q and  $\bar{Q}$  outputs. The Clock (CP) and Enable ( $\bar{E}$ ) inputs are common to all flip-flops. When the  $\bar{E}$  is input HIGH, the register will retain the present data independent of the CP input. The  $D_n$  and  $\bar{E}$  inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed.

## Truth Table

Inputs			Outputs	
$\bar{E}$	CP	$D_n$	$Q_n$	$\bar{Q}_n$
H	—	X	NC	NC
L	—	H	H	L
L	—	L	L	H

H = HIGH Voltage Level

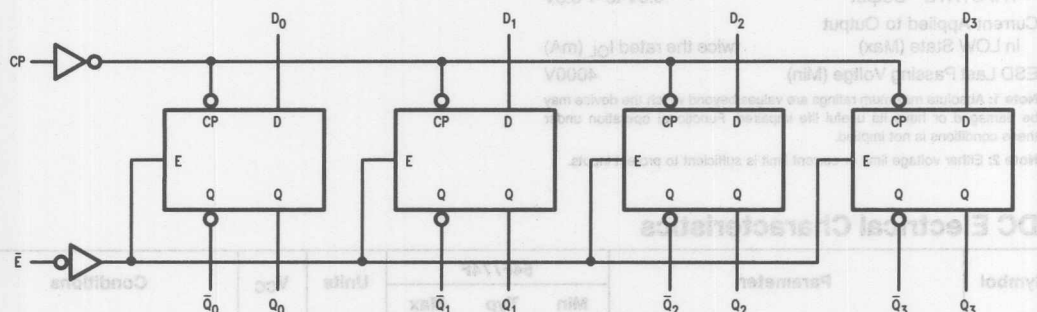
L = LOW Voltage Level

X = Immaterial

— = LOW-to-HIGH Transition

NC = No Change

## Logic Diagram



Symbol	Parameter	Units	Min	Max	Conditions
$V_{IH}$	Input HIGH Voltage	V	2.0	5.0	Recognized as a HIGH Signal
$V_{IL}$	Input LOW Voltage	V	0.8	0.8	Recognized as a LOW Signal
$V_{DD}$	Input Clamp Diode Voltage	V	-1.3	-1.3	$I_{IH} = -1.8 \text{ mA}$
	Output HIGH	54F 10 <sup>4</sup> Vcc	2.5	2.5	$I_{OH} = -1 \text{ mA}$
	Output LOW	54F 10 <sup>4</sup> Vcc	0.8	0.8	$I_{OL} = 20 \text{ mA}$
$I_{IH}$	Input HIGH Current	$\mu\text{A}$	2.0	2.0	$V_{IH} = 2.7 \text{ V}$
$I_{IHL}$	Input HIGH Current Breakdown Test	$\mu\text{A}$	100	7.0	$V_{IH} = 7.0 \text{ V}$
$I_{OH}$	Output HIGH Current	$\mu\text{A}$	250	20	$V_{OH} = V_{CC}$
$V_{IO}$	Input Leakage	V	4.75	4.75	$I_{IO} = 1.8 \mu\text{A}$
$I_{OQ}$	Output Leakage	$\mu\text{A}$	3.75	3.75	$V_{OQ} = 150 \text{ mV}$
$I_{L}$	Input LOW Current	mA	-0.8	-0.8	$V_{IL} = 0.5 \text{ V}$
$I_{OS}$	Output Short-Circuit Current	mA	-150	-150	$V_{OH} = 0 \text{ V}$
$I_{CC}$	Power Supply Current	mA	40	28	$V_{CC} = \text{LOW}$

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCL</sub>	Power Supply Current		28	40	mA	Max	V <sub>O</sub> = LOW

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	100	140		75		100		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	3.5	5.0	6.5	3.0	8.5	4.0	7.5	ns	2-3
$t_{\text{PHL}}$	CP to $Q_n, \bar{Q}_n$	5.0	6.5	8.5	4.0	10.0	5.0	9.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	3.0		4.0		3.0		ns	2-6
$t_s(\text{L})$	$D_n$ to CP	3.0		4.0		3.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	1.0		2.0		1.0		ns	2-6
$t_h(\text{L})$	$D_n$ to CP	1.0		2.0		1.0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	6.0		8.0		6.0		ns	2-6
$t_s(\text{L})$	$\bar{E}$ to CP	6.0		8.0		6.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		0		0		ns	2-4
$t_h(\text{L})$	$\bar{E}$ to CP	0		0		0			
$t_w(\text{H})$	CP Pulse Width	4.0		5.0		4.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	5.0		7.0		5.0			




**54F/74F381**

## 4-Bit Arithmetic Logic Unit

### General Description

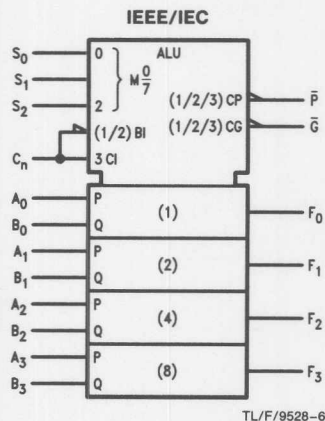
The 'F381 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional select input codes force the function outputs LOW or HIGH. Carry propagate and generate outputs are provided for use with the 'F182 carry lookahead generator for high-speed expansion to longer word lengths. For ripple expansion, refer to the 'F382 ALU data sheet.

### Features

- Low input loading minimizes drive requirements
- Performs six arithmetic and logic functions
- Selectable LOW (clear) and HIGH (preset) functions
- Carry generate and propagate outputs for use with carry lookahead generator

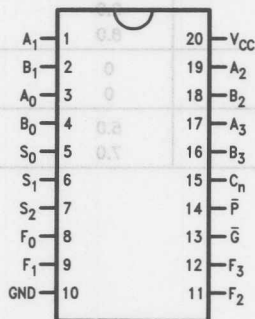
**Ordering Code:** See Section 5

### Logic Symbols

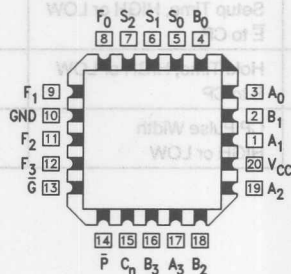


### Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak



Pin Assignment  
for LCC



# Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_0-A_3$	A Operand Inputs	1.0/3.0	20 $\mu$ A/ -1.8 mA
$B_0-B_3$	B Operand Inputs	1.0/3.0	20 $\mu$ A/ -1.8 mA
$S_0-S_2$	Function Select Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$C_n$	Carry Input	1.0/4.0	20 $\mu$ A/ -2.4 mA
$\bar{G}$	Carry Generate Output (Active LOW)	50/33.3	-1 mA/20 mA
$\bar{P}$	Carry Propagate Output (Active LOW)	50/33.3	-1 mA/20 mA
$F_0-F_3$	Function Outputs	50/33.3	-1 mA/20 mA

## Functional Description

Signals applied to the Select inputs  $S_0-S_2$  determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Truth Table. The circuit performs the arithmetic functions for either active HIGH or active LOW operands, with output levels in the same convention. In the Subtract operating modes, it is necessary to force a carry (HIGH for active

HIGH operands, LOW for active LOW operands) into the  $C_n$  input of the least significant package.

The Carry Generate ( $\bar{G}$ ) and Carry Propagate ( $\bar{P}$ ) outputs supply input signals to the 'F182 carry lookahead generator for expansion to longer word length, as shown in Figure 1. Note that an 'F382 ALU is used for the most significant package. Typical delays for Figure 1 are given in Figure 2.

Function Select Table

Select			Operation
$S_0$	$S_1$	$S_2$	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	$A \oplus B$
H	L	H	$A + B$
L	H	H	$AB$
H	H	H	Preset

H = HIGH Voltage Level  
L = LOW Voltage Level

FIGURE 2. 16-Bit Delay Tabulation

Path Segment	Toward $F_n$	Output $C_n + 4, OVR$
$A_i$ or $B_i$ to $\bar{P}$	7.2 ns	7.2 ns
$\bar{P}_i$ to $C_n + j$ ('F182)	6.2 ns	6.2 ns
$C_n$ to $F$	8.1 ns	—
$C_n$ or $C_n + 4, OVR$	—	8.0 ns
Total Delay	21.5 ns	21.4 ns

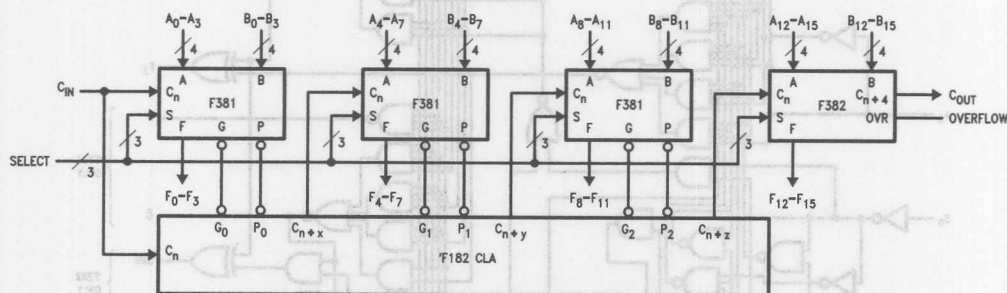
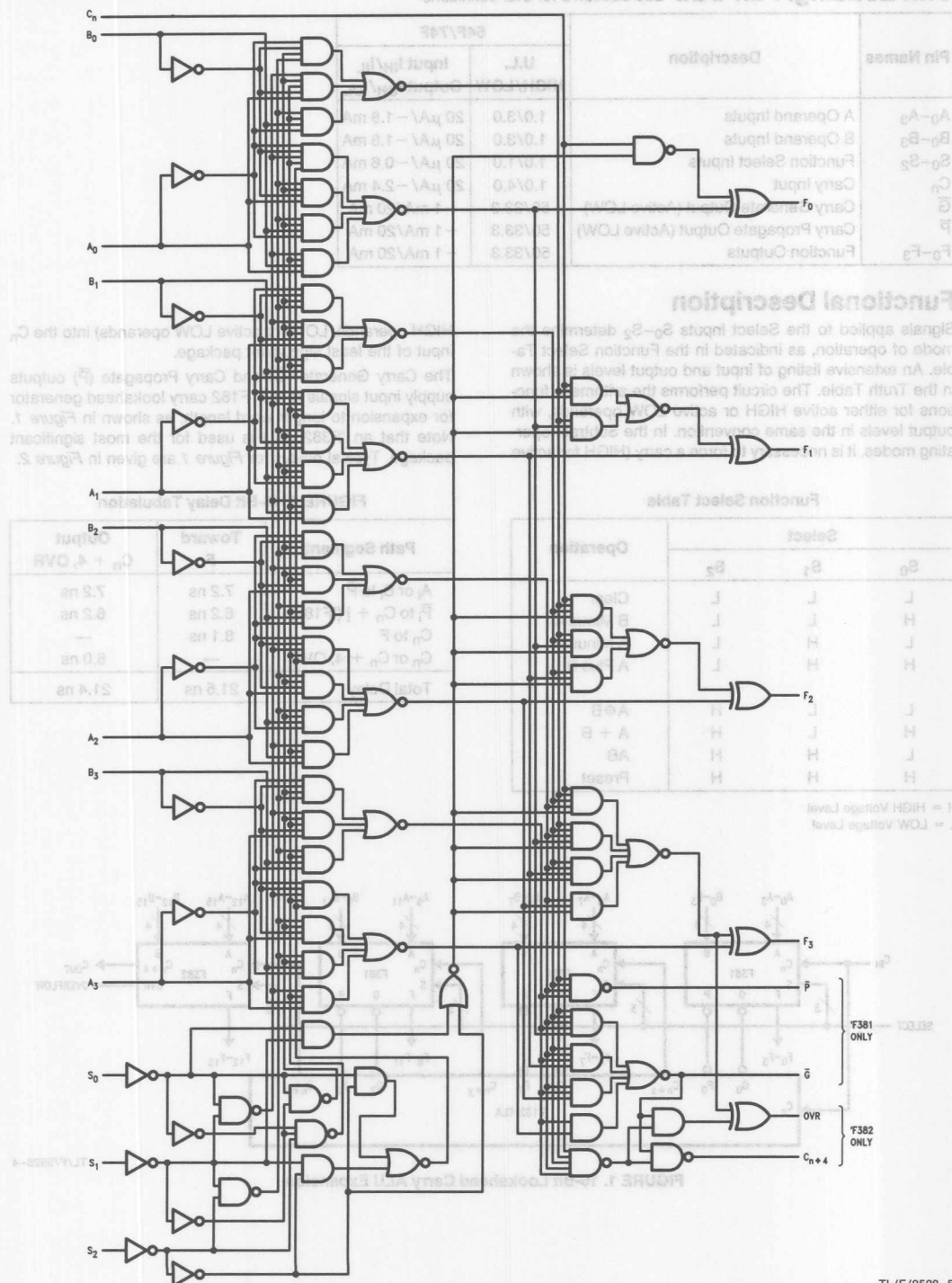


FIGURE 1. 16-Bit Lookahead Carry ALU Expansion

TL/F/9528-4

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

TL/F/9528-5

Truth Table												
Inputs				Outputs								
Function	S <sub>0</sub>	S <sub>1</sub>	S <sub>2</sub>	C <sub>n</sub>	A <sub>n</sub>	B <sub>n</sub>	F <sub>0</sub>	F <sub>1</sub>	F <sub>2</sub>	F <sub>3</sub>	G	P
CLEAR	L	L	L	X	X	X	L	L	L	L	L	L
B Minus A	H	L	L	L	L	L	L	L	L	L	L	L
A Minus B	L	H	L	L	L	L	L	L	L	L	L	L
A Plus B	H	H	L	L	L	L	L	L	L	L	L	L
A ⊕ B	L	L	H	X	L	L	L	L	L	L	L	L
A + B	H	L	H	X	L	L	L	L	L	L	L	L
AB	L	L	H	X	L	L	L	L	L	L	L	L
PRESET	H	H	H	X	L	L	L	L	L	L	L	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

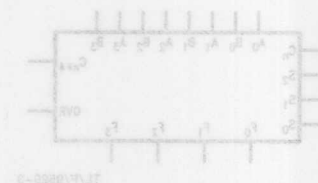
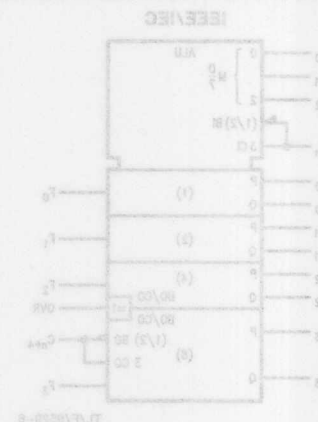
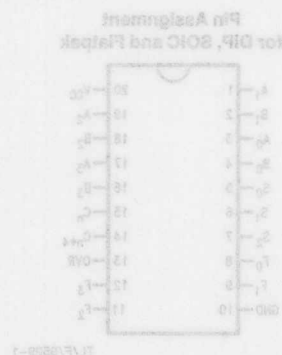
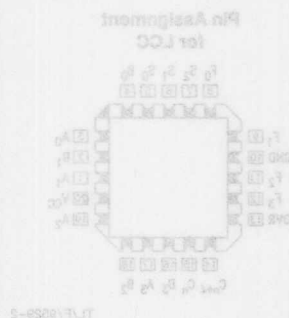
Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BV</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V (S <sub>n</sub> )
				-1.8	mA	Max	V <sub>IN</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
				-2.4	mA	Max	V <sub>IN</sub> = 0.5V (C <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		59	89	mA	Max	

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $C_n$ to $F_i$	2.5 2.5	8.1 5.7	12.0 8.0			2.5 2.5	13.0 9.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay Any A or B to Any F	4.0 3.5	10.4 8.2	15.0 11.0			4.0 3.5	16.0 12.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_i$ to $F_i$	4.5 4.0	8.3 8.2	20.5 15.0			4.5 4.0	21.5 16.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_i$ or $B_i$ to $\overline{G}$	3.5 3.5	6.4 6.8	10.0 10.0			3.5 3.0	11.0 11.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_i$ or $B_i$ to $\overline{P}$	2.5 3.5	7.2 6.5	10.5 9.5			2.5 3.5	11.5 10.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_i$ to $\overline{G}$ or $\overline{P}$	4.0 4.5	7.8 10.2	12.0 13.5			4.0 4.5	13.0 14.5	ns	2-3







# 54F/74F382

## 4-Bit Arithmetic Logic Unit

### General Description

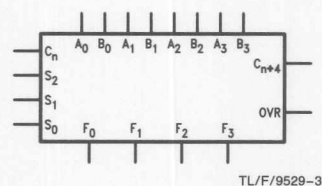
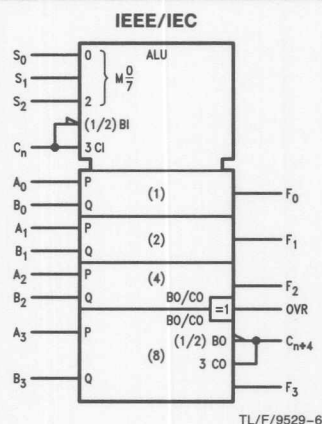
The 'F382 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select input codes force the Function outputs LOW or HIGH. An Overflow output is provided for convenience in twos complement arithmetic. A Carry output is provided for ripple expansion. For high-speed expansion using a Carry Look-ahead Generator, refer to the 'F381 data sheet.

### Features

- Performs six arithmetic and logic functions
- Selectable LOW (clear) and HIGH (preset) functions
- LOW input loading minimizes drive requirements
- Carry output for ripple expansion
- Overflow output for twos complement arithmetic

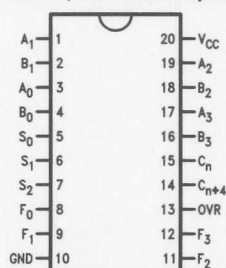
**Ordering Code:** See Section 5

### Logic Symbols

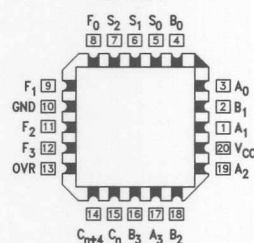


### Connection Diagrams

Pin Assignment  
for DIP, SOIC and Flatpak



Pin Assignment  
for LCC



# Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_0-A_3$	A Operand Inputs	1.0/4.0	20 $\mu$ A/−2.4 mA
$B_0-B_3$	B Operand Inputs	1.0/4.0	20 $\mu$ A/−2.4 mA
$S_0-S_2$	Function Select Inputs	1.0/1.0	20 $\mu$ A/−0.6 mA
$C_n$	Carry Input	1.0/5.0	20 $\mu$ A/−3.0 mA
$C_n + 4$	Carry Output	50/33.3	−1 mA/20 mA
OVR	Overflow Output	50/33.3	−1 mA/20 mA
$F_0-F_3$	Function Outputs	50/33.3	−1 mA/20 mA

## Functional Description

Signals applied to the Select inputs  $S_0-S_2$  determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Truth Table. The circuit performs the arithmetic functions for either active HIGH or active LOW operands, with output levels in the same convention. In the Subtract operating modes, it is necessary to force a carry (HIGH for active HIGH operands, LOW for active LOW operands) into the  $C_n$  input of the least significant package. Ripple expansion is illustrated in Figure 1. The overflow output OVR is the Exclusive-OR of  $C_n + 3$  and  $C_n + 4$ ; a HIGH signal on OVR indicates overflow in two's complement operation. Typical delays for Figure 1 are given in Figure 2.

Function Select Table

Select			Operation
$S_0$	$S_1$	$S_2$	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	$A \oplus B$
H	L	H	$A + B$
L	H	H	AB
H	H	H	Preset

H = HIGH Voltage Level  
L = LOW Voltage Level

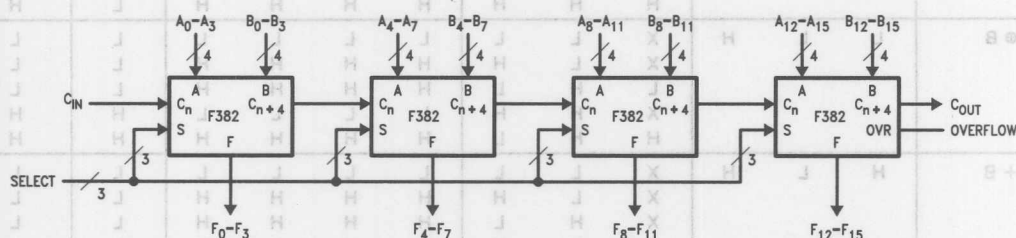


FIGURE 1. 16-Bit Ripplly Carry ALU Expansion

TL/F/9529-5

Path Segment	Toward F	Output $C_n + 4$ , OVR
$A_i$ or $B_j$ to $C_n + 4$	6.5 ns	6.5 ns
$C_n$ to $C_n + 4$	6.3 ns	6.3 ns
$C_n$ to $C_n + 4$	6.3 ns	6.3 ns
$C_n$ to F	8.1 ns	—
$C_n$ to $C_n + 4$ , OVR	—	8.0 ns
Total Delay	27.2 ns	27.1 ns

FIGURE 2. 16-Bit Delay Tabulation

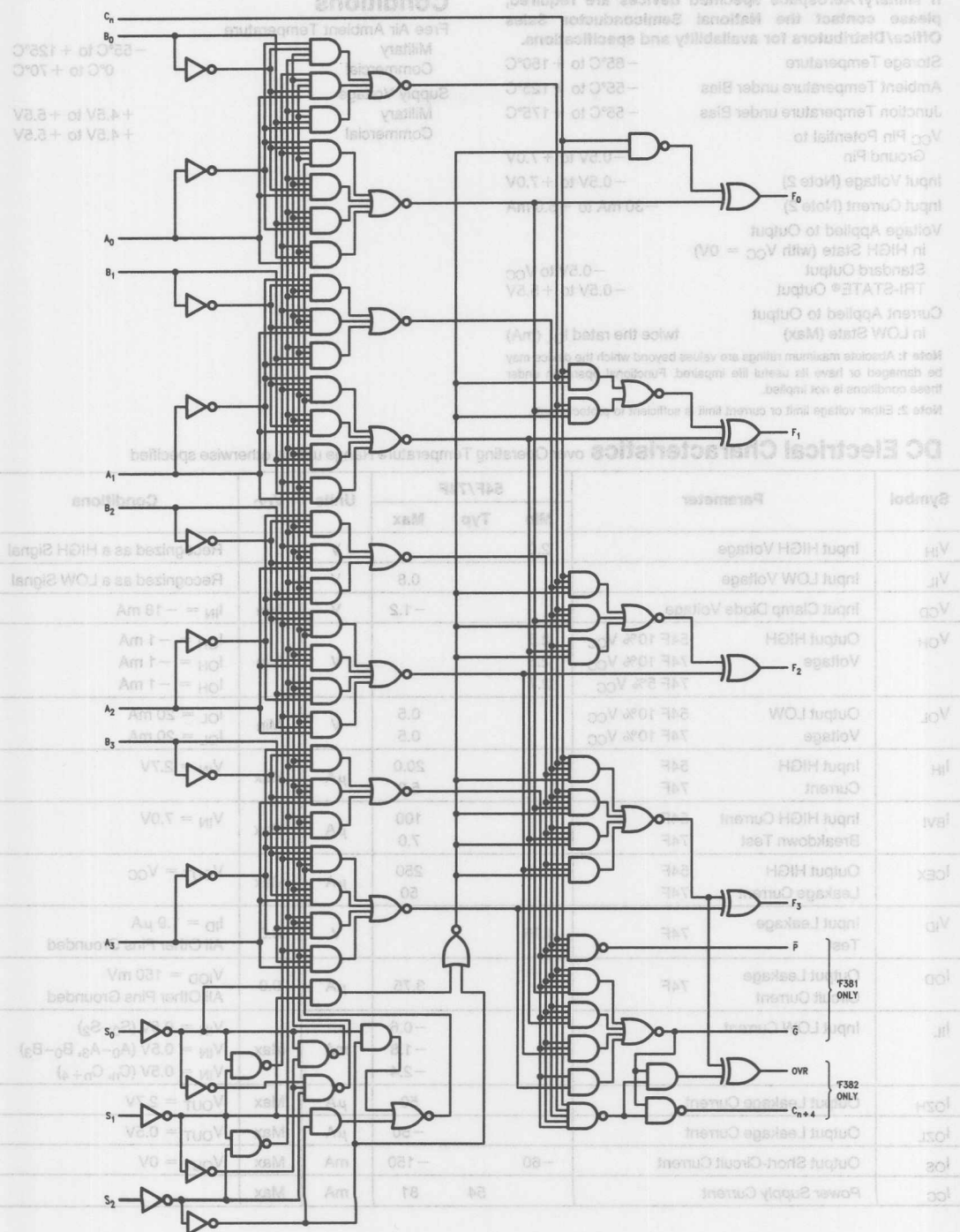
H = HIGH Voltage Level  
L = LOW Voltage Level  
t = time

## Truth Table

Function	Inputs						Outputs					
	S <sub>0</sub>	S <sub>1</sub>	S <sub>2</sub>	C <sub>n</sub>	A <sub>n</sub>	B <sub>n</sub>	F <sub>0</sub>	F <sub>1</sub>	F <sub>2</sub>	F <sub>3</sub>	OVR	C <sub>n</sub> + 4
CLEAR	L	L	L	L	X	X	L	L	L	L	H	H
				H	X	X	L	L	L	L	H	H
B MINUS A	H	L	L	L	L	L	H	H	H	H	L	L
				L	L	H	H	H	H	H	L	H
				L	L	H	L	L	L	L	L	L
				L	L	H	L	L	L	L	L	L
				L	L	H	L	L	L	L	L	L
				L	L	H	L	L	L	L	L	L
				L	L	H	L	L	L	L	L	L
				L	L	H	L	L	L	L	L	L
A MINUS B	L	H	L	L	L	L	H	H	H	H	L	L
				L	L	H	L	L	L	L	L	H
				L	L	H	L	L	L	L	L	L
				L	L	H	L	L	L	L	L	L
				L	L	H	L	L	L	L	L	L
				L	L	H	L	L	L	L	L	L
				L	L	H	L	L	L	L	L	L
				L	L	H	L	L	L	L	L	L
A PLUS B	H	H	L	L	L	L	L	L	L	L	L	L
				L	L	H	H	H	H	H	L	L
				L	L	H	H	H	H	H	L	L
				L	L	H	H	H	H	H	L	L
				L	L	H	H	H	H	H	L	L
				L	L	H	H	H	H	H	L	L
				L	L	H	H	H	H	H	L	L
				L	L	H	H	H	H	H	L	L
A ⊕ B	L	L	H	X	L	L	L	L	L	L	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
A + B	H	L	H	X	L	L	L	L	L	L	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
AB	L	H	H	X	L	L	L	L	L	L	H	H
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
PRESET	H	H	H	X	L	L	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

## Logic Diagram



TL/F/9529-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	−55°C to +125°C
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics** over Operating Temperature Range unless otherwise specified

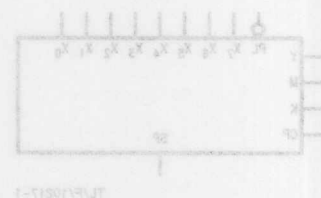
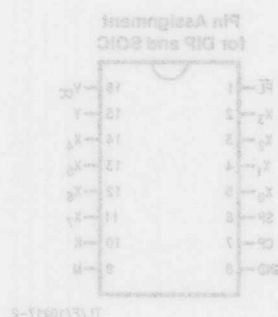
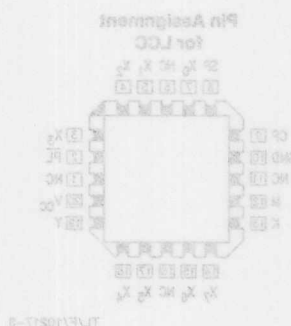
Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V (S <sub>0</sub> –S <sub>2</sub> )
				−1.8			V <sub>IN</sub> = 0.5V (A <sub>0</sub> –A <sub>3</sub> , B <sub>0</sub> –B <sub>3</sub> )
				−2.4			V <sub>IN</sub> = 0.5V (C <sub>n</sub> , C <sub>n</sub> +4)
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		54	81	mA	Max	

4-22297A-UT

Please do not use this data for any other purpose than the one intended. The information is provided only for the purpose of design and is not to be used for any other purpose.

**AC Electrical Characteristics:** See Section 2 for U.L. definitions

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $C_n$ to $F_i$	3.0 2.5	8.1 5.7	12.0 8.0			3.0 2.5	13.0 9.0	ns	2-4
$t_{PLH}$ $t_{PHL}$	Propagation Delay Any A or B to Any F	4.0 3.0	10.4 8.2	15.0 11.0			3.5 2.5	17.0 12.0	ns	2-4
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_i$ to $F_i$	6.5 4.0	11.0 8.2	20.5 15.0			5.5 4.0	21.5 17.5	ns	2-4
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_i$ or $B_i$ to $C_n + 4$	3.5 3.5	6.0 6.5	8.5 9.0			3.5 3.5	11.0 10.5	ns	2-4
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_i$ to OVR or $C_n + 4$	7.0 5.0	12.5 9.0	16.5 12.0			7.0 5.0	17.5 14.5	ns	2-4
$t_{PLH}$ $t_{PHL}$	Propagation Delay $C_n$ to $C_n + 4$	2.5 3.5	5.6 6.3	8.0 9.0			2.0 2.0	9.0 10.0	ns	2-4
$t_{PLH}$ $t_{PHL}$	Propagation Delay $C_n$ to OVR	3.5 2.5	8.0 7.1	11.0 10.0			3.5 2.5	13.0 11.0	ns	2-4
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_i$ or $B_i$ to OVR	7.0 3.0	11.5 8.0	15.5 10.5			7.0 3.0	16.5 11.5	ns	2-4



Input Loading/Fan-Out: See Section 2 For U.L. Definitions

Pin	Description	Max/Typ (U.L.)	Min/Typ
$C_p$	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu\text{A}$ - 0.8 mA
$K$	Serial Expansion Input	1.0/1.0	20 $\mu\text{A}$ - 0.8 mA
$M$	Mode Control Input	1.0/1.0	20 $\mu\text{A}$ - 0.8 mA
$F_i$	Asynchronous Parallel Load Input (Active LOW)	1.0/2.0	20 $\mu\text{A}$ - 1.2 mA
$X_0-X_7$	Multiplexed Data Inputs	1.0/1.0	20 $\mu\text{A}$ - 0.8 mA
$Y$	Serial Multiplier Input	1.0/1.0	20 $\mu\text{A}$ - 0.8 mA
$S_p$	Serial X*Y Product Output	50/33.3	-1 mA/50 mA




**54F/74F384**

## 8-Bit Serial/Parallel Twos Complement Multiplier

### General Description

The 'F384 is an 8-bit by 1-bit sequential logic element that multiplies two numbers represented in twos complement notation. The device implements Booth's algorithm internally to produce a twos complement product that needs no subsequent correction. Parallel inputs accept and store an 8-bit multiplicand ( $X_0$ – $X_7$ ). The multiplier word is then applied to the Y input in a serial bit stream, least significant bit first. The product is clocked out at the SP output, least significant bit first.

The K input is used for expansion to longer X words, using two or more 'F384 devices by connecting the output (SP) of one device to the K input of the other device. The Mode Control (M) input is used to establish the most significant

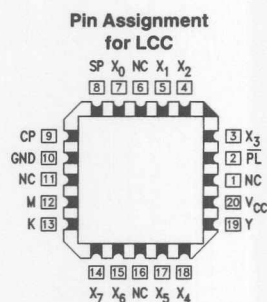
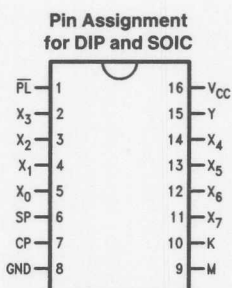
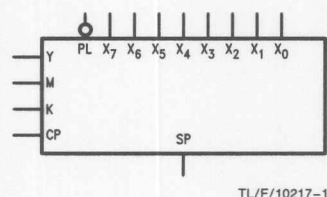
device. An asynchronous Parallel Load (PL) input clears the internal flip-flops to the start condition and enables the X latches to accept new multiplicand data. The Parallel Load (PL) also clears the output (SP).

### Features

- Twos complement multiplication
- 8-bit by 1-bit sequential logic element
- Parallel inputs accept and store an 8-bit multiplicand ( $X_0$ – $X_7$ )
- K input is used for expansion to longer X words
- Functionally and pin compatible to the Am25LS14A

**Ordering Code:** See Section 5

### Logic Symbol



**Input Loading/Fan-Out:** See Section 2 For U.L. Definitions

Pin Names	Description	54F/74F (U.L.) High/Low	$I_{IH}/I_{IL}$ $I_{OH}/I_{OL}$
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/ – 0.6 mA
K	Serial Expansion Input	1.0/1.0	20 $\mu$ A/ – 0.6 mA
M	Mode Control Input	1.0/1.0	20 $\mu$ A/ – 0.6 mA
PL	Asynchronous Parallel Load Input (Active LOW)	1.0/2.0	20 $\mu$ A/ – 1.2 mA
$X_0$ – $X_7$	Multiplicand Data Inputs	1.0/1.0	20 $\mu$ A/ – 0.6 mA
Y	Serial Multiplier Input	1.0/1.0	20 $\mu$ A/ – 0.6 mA
SP	Serial $X \times Y$ Product Output	50/33.3	– 1 mA/20 mA

## Functional Description

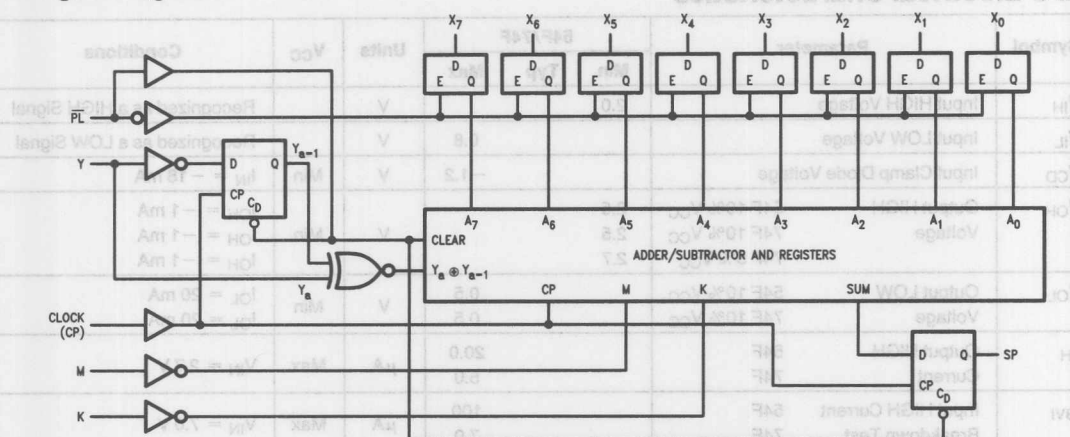
Referring to the Logic Diagram and Figure A, the multiplicand ( $X_0$ – $X_7$ ) latches are enabled to receive new data when  $\overline{PL}$  is LOW. Data that meet the setup/hold time requirements are stored when  $\overline{PL}$  goes HIGH. The LOW signal on  $\overline{PL}$  clears the output (SP) as well as the internal flip-flops.

New multiplicand data enter the X latches during bit time  $T_0$ . It is assumed that  $\overline{PL}$  goes LOW shortly after the CP rising edge that marks the beginning of  $T_0$  and goes HIGH again one recovery time before the beginning of  $T_1$ . The LSB ( $Y_0$ ) of the multiplier is applied to the Y input during  $T_0$  and must be held one hold time after the beginning of  $T_1$ . One propagation delay after the beginning of  $T_1$ , the LSB ( $S_0$ ) of the product appears at the output (SP). This multiplication process is continued by applying  $Y_1$ – $Y_6$  to the Y input causing  $S_1$ – $S_6$  of the product to appear at the output (SP).

The MSB  $Y_7$  (the sign bit) of the multiplier is first applied to the Y input during  $T_7$  and must be held through  $T_{16}$  causing  $S_7$ – $S_{15}$  of the product to appear at the output (SP). This extension of the sign bit is a necessary adjunct to the implementation of Booth's algorithm. This is a built-in feature of the 'F322 Shift Register (See Figure B).

Figure C shows the method of using two F384's to perform a  $12 \times n$  bit multiplication. Notice that the sign of X is effectively extended by connecting  $X_{11}$  to  $X_4$ – $X_7$  of the most significant package. Whereas the  $8 \times 8$  multiplication required 17 clock periods ( $m + n$  to form the product terms plus  $T_0$  to clear the multiplier), the arrangement of Figure C requires  $12 + n + 1$  bits to form the product terms.

## Logic Diagram



TL/F/10217-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

Inputs						Internal	Output	Function
$\overline{PL}$	CP	K	M	$X_i$	Y	$Y_{a-1}$	SP	
X	X	L	L	X	X	X	X	Most Significant Multiplier Device
X	X	CS	H	X	X	X	X	Devices Cascaded in Multiplier String
L	X	X	X	OP	X	L	L	Load New Multiplicand and Clear Internal Sum and Carry Registers
H	X	X	X	X	X	X	X	Device Enabled
H	↑	X	X	X	L	L	AR	Shift Sum Register
H	↑	X	X	X	L	H	AR	Add Multiplicand to Sum Register and Shift
H	↑	X	X	X	H	L	AR	Subtract Multiplicand from Sum Register and Shift
H	↑	X	X	X	H	H	AR	Shift Sum Register

H = HIGH Voltage Level

L = LOW Voltage Level

↑ = LOW-to-HIGH Transition

CS = Connected to SP output of high order device

OP =  $X_i$  latches open for new data ( $i = 0$ – $7$ )

AR = Output as required per Booth's algorithm

X = Immaterial

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

Ambient Temperature under Bias  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Junction Temperature under Bias  $-55^{\circ}\text{C}$  to  $+175^{\circ}\text{C}$

$V_{CC}$  Pin Potential to Ground Pin  $-0.5\text{V}$  to  $+7.0\text{V}$

Input Voltage (Note 2)  $-0.5\text{V}$  to  $+7.0\text{V}$

Input Current (Note 2)  $-30\text{ mA}$  to  $+5.0\text{ mA}$

Voltage Applied to Output in HIGH State (with  $V_{CC} = 0\text{V}$ )  $-0.5\text{V}$  to  $V_{CC}$

Standard Output  $-0.5\text{V}$  to  $V_{CC}$

TRI-STATE® Output  $-0.5\text{V}$  to  $+5.5\text{V}$

Current Applied to Output in LOW State (Max) twice the rated  $I_{OL}$  (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature

Military  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Commercial  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$

Supply Voltage

Military  $+4.5\text{V}$  to  $+5.5\text{V}$

Commercial  $+4.5\text{V}$  to  $+5.5\text{V}$

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	$V_{CC}$	Conditions
		Min	Typ	Max			
$V_{IH}$	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
$V_{IL}$	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
$V_{CD}$	Input Clamp Diode Voltage			-1.2	V	Min	$I_{IN} = -18\text{ mA}$
$V_{OH}$	Output HIGH Voltage	54F 10% $V_{CC}$	2.5		V	Min	$I_{OH} = -1\text{ mA}$
		74F 10% $V_{CC}$	2.5				$I_{OH} = -1\text{ mA}$
		74F 5% $V_{CC}$	2.7				$I_{OH} = -1\text{ mA}$
$V_{OL}$	Output LOW Voltage	54F 10% $V_{CC}$		0.5	V	Min	$I_{OL} = 20\text{ mA}$
		74F 10% $V_{CC}$		0.5			$I_{OL} = 20\text{ mA}$
$I_{IH}$	Output HIGH Current	54F		20.0	$\mu\text{A}$	Max	$V_{IN} = 2.7\text{ V}$
		74F		5.0			
$I_{BI}$	Input HIGH Current Breakdown Test	54F		100	$\mu\text{A}$	Max	$V_{IN} = 7.0\text{ V}$
		74F		7.0			
$I_{CEX}$	Output HIGH Leakage Current	54F		250	$\mu\text{A}$	Max	$V_{OUT} = V_{CC}$
		74F		50			
$V_{ID}$	Input Leakage Test	74F	4.75		V	0.0	$I_{ID} = 1.9\text{ }\mu\text{A}$ All Other Pins Grounded
$I_{OD}$	Output Leakage Circuit Current	74F		3.75	$\mu\text{A}$	0.0	$V_{IOD} = 150\text{ mV}$ All Other Pins Grounded
$I_{IL}$	Input LOW Current			-0.6	mA	Max	$V_{IN} = 0.5\text{V}$ (Except PL)
				-1.2		Max	$V_{IN} = 0.5\text{V}$ (PL)
$I_{OS}$	Output Short-Circuit Current		-60	-150	mA	Max	$V_{OUT} = 0\text{V}$
$I_{CC}$	Power Supply Current		60	90	mA	Max	$V_O = \text{HIGH}$

H = HIGH Voltage Level

L = LOW Voltage Level

T = LOW-to-HIGH Transition

CE = Connected to CE output of high order device

GP = X indicates open for new data (i = 0-T)

AR = Output as required per Booth's algorithm

X = Indeterminate

# **AC Electrical Characteristics** : See Section 2 for Waveforms and Load Configurations

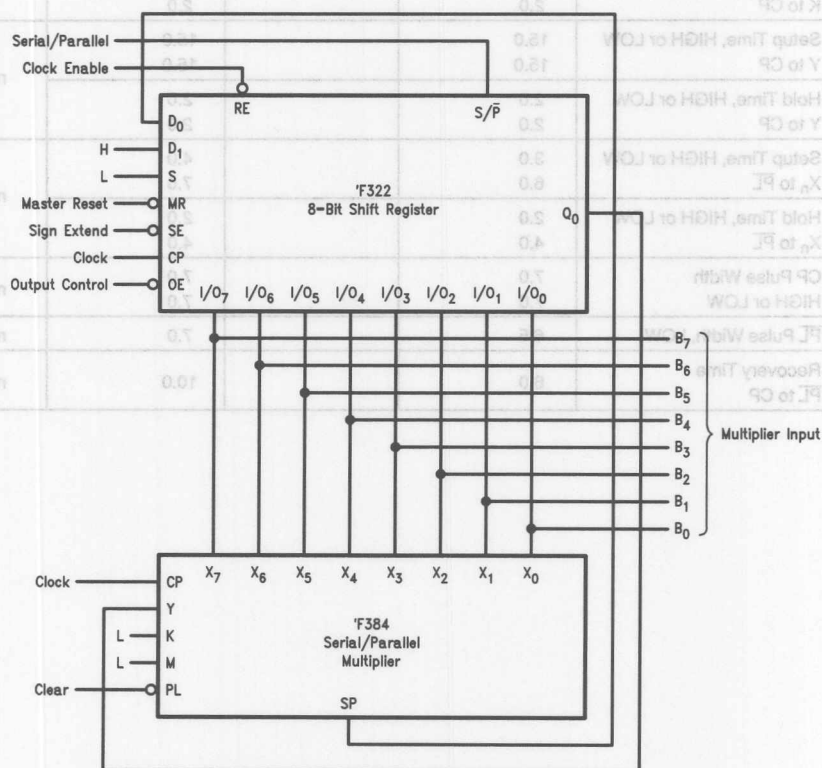
Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	50					50		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	3.5	6.5	9.0			3.5	10.0	ns	2-3
$t_{\text{PHL}}$	CP to SP	3.5	6.5	9.0			3.5	10.0		
$t_{\text{PHL}}$	Propagation Delay	6.0	10.0	13.0			6.0	14.0	ns	2-3
	PL to SP									

# **AC Operating Requirements** : See Section 2 for Waveforms

Symbol	Parameter	54F/74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	9.0				10.0		ns	2-6
$t_s(\text{L})$	K to CP	9.0				10.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0				2.0		ns	2-6
$t_h(\text{L})$	K to CP	2.0				2.0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	15.0				15.0		ns	2-6
$t_s(\text{L})$	Y to CP	15.0				15.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0				2.0		ns	2-6
$t_h(\text{L})$	Y to CP	2.0				2.0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	3.0				4.0		ns	2-6
$t_s(\text{L})$	$X_n$ to $\overline{\text{PL}}$	6.0				7.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0				2.0		ns	2-4
$t_h(\text{L})$	$X_n$ to $\overline{\text{PL}}$	4.0				4.0			
$t_w(\text{H})$	CP Pulse Width	7.0				7.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	7.0				7.0			
$t_w(\text{L})$	$\overline{\text{PL}}$ Pulse Width, LOW	6.5				7.0		ns	2-4
$t_{\text{rec}}$	Recovery Time	6.0				10.0		ns	2-6
	$\overline{\text{PL}}$ to CP								



FIGURE 2-6 4-Bit Parallel Bus Multiplier, Bus Organized, with 4-Bit Truncated Product



**FIGURE B. 8-Bit by 8-Bit Multiplier, Bus Organized, with 8-Bit Truncated Product**

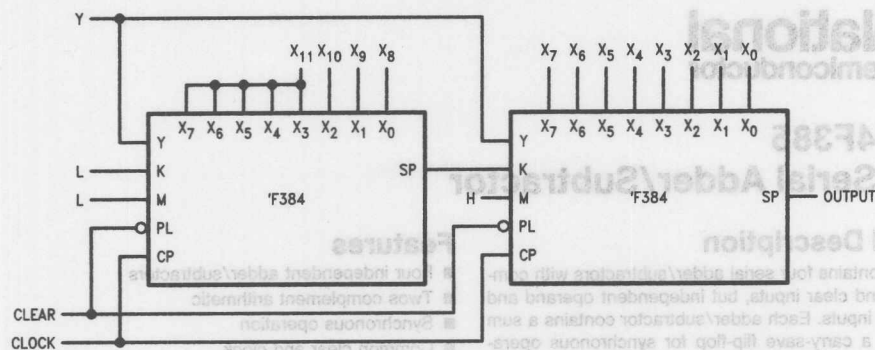
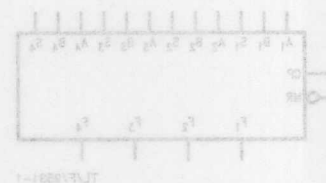


FIGURE C. 12-Bit by n-Bit Two's Complement Multiplier

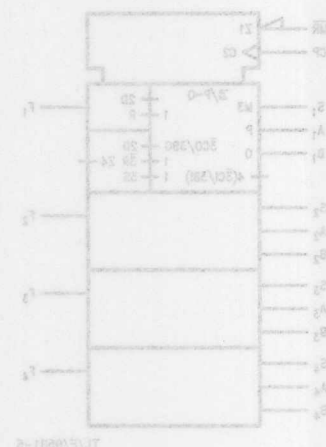
The 'F385 contains for serial adder/subtractor with a common clock and clear inputs, but independent operand and mode select inputs. Each adder/subtractor contains a sum flip-flop and a carry-save flip-flop for asynchronous operation. The 'F385 performs either A plus B or A minus B in two's complement notation, but can complement the inputs only or ones complement operation. The 'F385 is designed for use with the 'F384 and 'F784 serial multipliers in implementing digital filters or butterfly networks in fast Fourier transforms.

Ordering Code: See Section 6

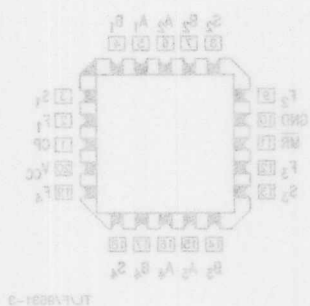
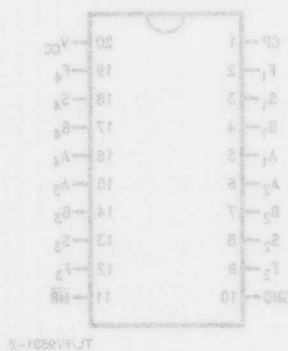
## Logic Symbols



IEEE/IEC



## Connection Diagrams

Pin Assignment  
for LCCPin Assignment  
for DIP, SOIC and Flatpak





## 54F/74F385 Quad Serial Adder/Subtractor

### General Description

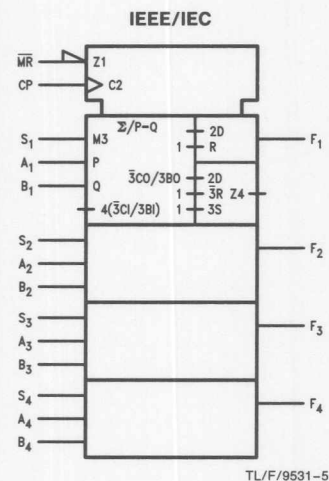
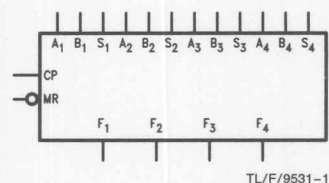
The 'F385 contains four serial adder/subtractors with common clock and clear inputs, but independent operand and mode select inputs. Each adder/subtractor contains a sum flip-flop and a carry-save flip-flop for synchronous operations. Each circuit performs either A plus B or A minus B in two's complement notation, but can also be used for magnitude-only or ones complement operation. The 'F385 is designed for use with the 'F384 and 'F784 serial multipliers in implementing digital filters or butterfly networks in fast Fourier transforms.

### Features

- Four independent adder/subtractors
- Two's complement arithmetic
- Synchronous operation
- Common clear and clock
- Ones complement or magnitude-only capability

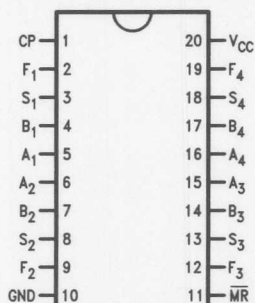
**Ordering Code:** See Section 5

### Logic Symbols

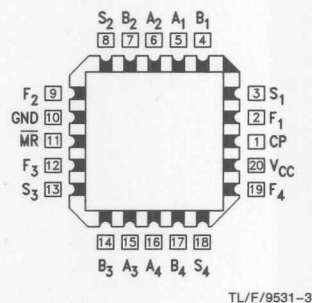


### Connection Diagrams

Pin Assignment  
for DIP, SOIC and Flatpak



Pin Assignment  
for LCC



# Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
A <sub>1</sub> -A <sub>4</sub>	A Operand Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
B <sub>1</sub> -B <sub>4</sub>	B Operand Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
S <sub>1</sub> -S <sub>4</sub>	Function Select Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 $\mu$ A/-0.6 mA
F <sub>1</sub> -F <sub>4</sub>	Sum or Difference Outputs	50/33.3	-1 mA/20 mA

## Functional Description

Each adder contains two edge-triggered flip-flops to store the sum and carry, as shown in the Logic Diagram. Flip-flop state changes occur on the rising edge of the Clock Pulse (CP) input signal. The Select (S) input should be LOW for the Add (A plus B) mode and HIGH for the Subtract (A minus B) mode. A LOW signal on the asynchronous Master Reset ( $\overline{MR}$ ) input clears the sum flip-flop and resets the carry flip-flop to zero in the Add mode or presets it to one in the Subtract mode.

In the Subtract mode, the B operand is internally complemented. Presetting the carry flip-flop to one completes the two's complement transformation by adding one to "A plus B" during the first (LSB) operation after  $\overline{MR}$  is released. For ones complement subtraction, the carry flip-flop can be set to zero by making S LOW during the reset, then making S HIGH after the reset but before the next clock.

## Truth Table

Inputs*				Internal Carry		Output*	Function
$\overline{MR}$	S	A	B	C	C <sub>1</sub>	F	
L	L	X	X	L	L	L	Clear
L	H	X	X	H	H	L	
H	L	L	L	L	L	L	Add
H	L	L	L	H	L	H	
H	L	L	H	L	L	H	
H	L	L	H	H	H	L	
H	L	H	L	L	L	H	
H	L	H	L	H	H	L	
H	L	H	H	L	H	L	
H	L	H	H	H	H	H	
H	H	L	L	L	L	H	Subtract
H	H	L	L	H	H	L	
H	H	L	H	L	L	L	
H	H	L	H	H	L	H	
H	H	H	L	L	H	L	
H	H	H	L	H	H	H	
H	H	H	H	L	L	H	
H	H	H	H	H	H	L	

H = HIGH Voltage Level

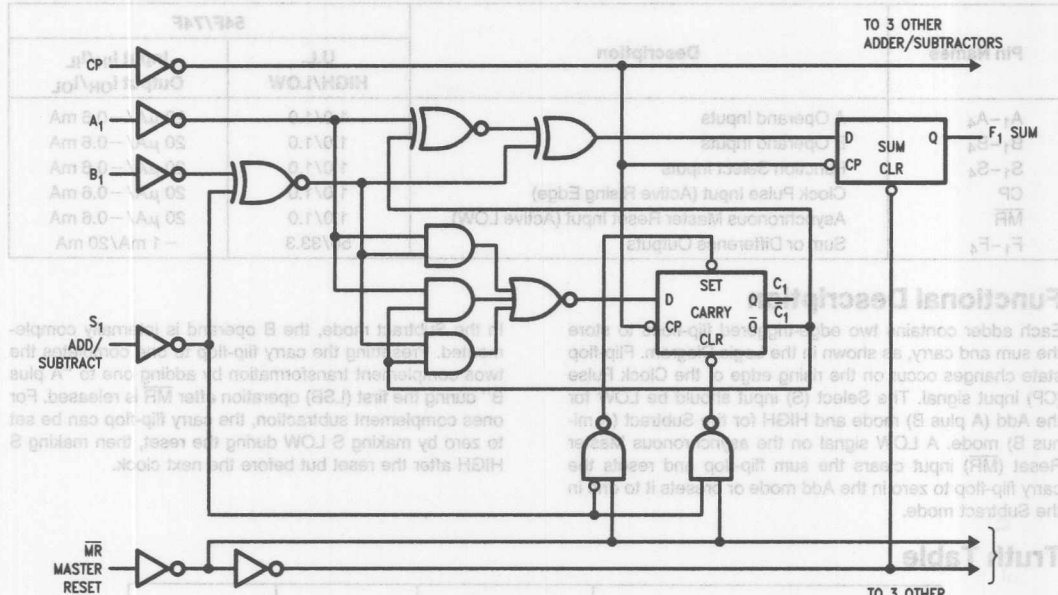
L = LOW Voltage Level

X = Immaterial

\* = Inputs before CP transition, output after C

C<sub>1</sub> = Carry flip-flop state before (C) and after (C<sub>1</sub>) clock transition

# Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function	Output*	Internal Carry	Inputs*	Inputs*	Inputs*	Inputs*	Inputs*	Inputs*
Clear	L	L	L	X	X	L	L	L
	L	H	L	X	X	L	L	L
	L	L	L	L	L	L	L	L
	L	L	L	L	L	L	L	L
	L	L	L	L	L	L	L	L
	L	L	L	L	L	L	L	L
	L	L	L	L	L	L	L	L
	L	L	L	L	L	L	L	L
Add	H	L	L	L	L	L	L	L
	H	L	L	L	L	L	L	L
	H	L	L	L	L	L	L	L
	H	L	L	L	L	L	L	L
	H	L	L	L	L	L	L	L
	H	L	L	L	L	L	L	L
	H	L	L	L	L	L	L	L
	H	L	L	L	L	L	L	L
Subtract	H	L	L	L	L	L	L	L
	H	L	L	L	L	L	L	L
	H	L	L	L	L	L	L	L
	H	L	L	L	L	L	L	L
	H	L	L	L	L	L	L	L
	H	L	L	L	L	L	L	L
	H	L	L	L	L	L	L	L
	H	L	L	L	L	L	L	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Indeterminate  
\* = Inputs before CP transition, output after CP  
C = Carry flip-flop state before (C) and after (C) clock transition

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output	−0.5V to +5.5V
TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	−55°C to +125°C
Military	0°C to +70°C
Commercial	
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		68	92*	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		68	92*	mA	Max	V <sub>O</sub> = LOW

\*95 mA for 54F

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	70	100		65		70		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay CP to $F_n$	3.5	6.0	8.0	3.0	10.0	3.5	9.0	ns	2-3
$t_{\text{PHL}}$		4.0	7.0	9.0	3.5	11.0	4.0	10.0		
$t_{\text{PHL}}$	Propagation Delay MR to $F_n$	5.5	9.0	12.0	5.0	14.0	5.5	13.0	ns	2-3

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	15.0		17.5		15.0		ns	2-6
$t_s(\text{L})$	$A_n$ to CP	15.0		17.5		15.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		0		0		ns	2-6
$t_h(\text{L})$	$A_n$ to CP	0		0		0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	15.0		17.5		15.0		ns	2-6
$t_s(\text{L})$	$B_n$ or $S_n$ to CP	15.0		17.5		15.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		0		0		ns	2-4
$t_h(\text{L})$	$B_n$ or $S_n$ to CP	0		0		0			
$t_w(\text{H})$	CP Pulse Width	6.0		7.0		6.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	6.0		7.0		6.0			
$t_w(\text{L})$	$\overline{\text{MR}}$ Width, LOW	6.0		6.5		6.0		ns	2-4
$t_{\text{rec}}$	Recovery Time, $\overline{\text{MR}}$ to CP	8.5		10.0		9.5		ns	2-6



## 54F/74F398 • 54F/74F399 Quad 2-Port Register

### General Description

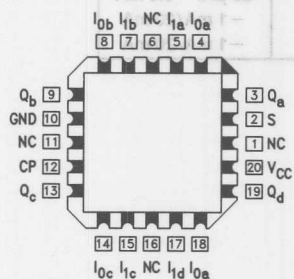
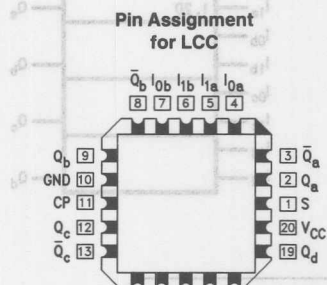
The 'F398 and 'F399 are the logical equivalents of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock. The 'F399 is the 16-pin version of the 'F398, with only the Q outputs of the flip-flops available.

### Features

- Select inputs from two data sources
- Fully positive edge-triggered operation
- Both true and complement outputs—'F398
- Guaranteed 4000V minimum ESD protection—'F399

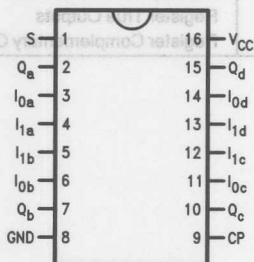
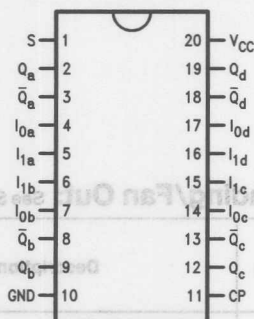
**Ordering Code:** See Section 5

### Connection Diagrams



'F398

### Pin Assignment for DIP, SOIC and Flatpak



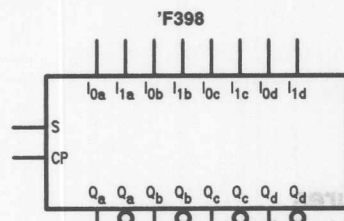
'F399

TL/F/9533-7

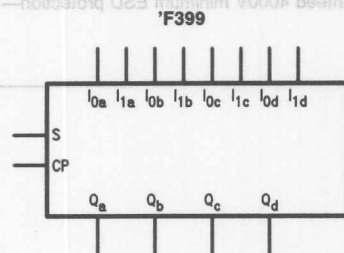
TL/F/9533-8



## Logic Symbols

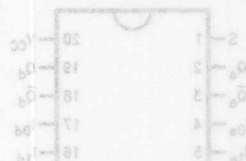


TL/F/9533-2

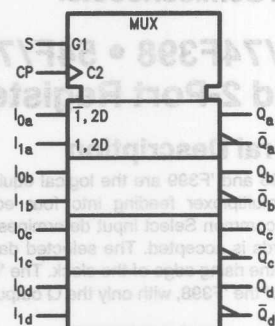


TL/F/9533-4

Pin Assignment  
for DIP, SOIC and Flatpak



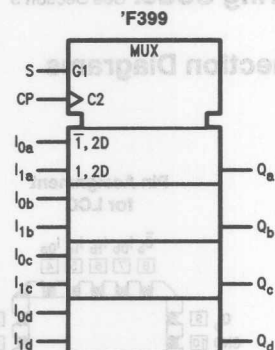
IEEE/IEC  
'F398



TL/F/9533-1

Ordering Code: See Section 2

Connection Diagram



TL/F/9533-3

## Unit Loading/Fan Out: See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
S	Common Select Input	1.0/1.0	20 $\mu$ A / -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A / -0.6 mA
$I_{0a}$ - $I_{0d}$	Data Inputs from Source 0	1.0/1.0	20 $\mu$ A / -0.6 mA
$I_{1a}$ - $I_{1d}$	Data Inputs from Source 1	1.0/1.0	20 $\mu$ A / -0.6 mA
$Q_a$ - $Q_d$	Register True Outputs	50/33.3	-1 mA/20 mA
$\bar{Q}_a$ - $\bar{Q}_d$	Register Complementary Outputs ('F398)	50/33.3	-1 mA/20 mA

## Functional Description

The 'F398 and 'F399 are high-speed quad 2-port registers. They select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs ( $I_{0x}$ ,  $I_{1x}$ ) and Select input (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The 'F398 has both Q and  $\bar{Q}$  outputs.

Function Table

Inputs			Outputs	
S	$I_0$	$I_1$	Q	$\bar{Q}$
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

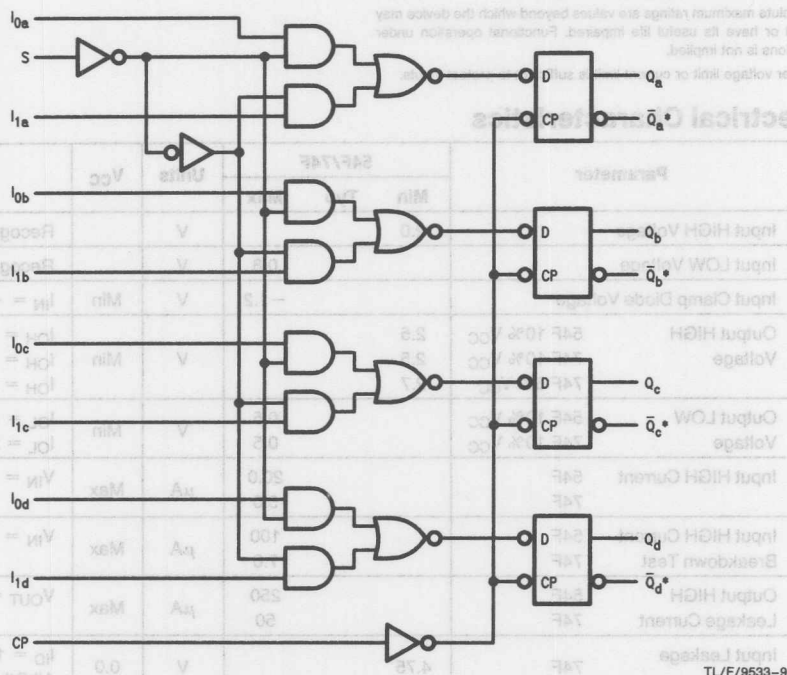
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition

l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition

X = Immaterial

\*F398 only

## Logic Diagram



\*F398 Only

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	X	-65°C to +150°C
Ambient Temperature under Bias		-55°C to +125°C
Junction Temperature under Bias		-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	X	-0.5V to +7.0V
Input Voltage (Note 2)		-0.5V to +7.0V
Input Current (Note 2)		-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)		-0.5V to V <sub>CC</sub>
Standard Output		-0.5V to V <sub>CC</sub>
TRI-STATE® Output		-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

ESD Last Passing Voltage (Min)—'F399 4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current ('F398)		25	38	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current ('F398)		25	38	mA	Max	V <sub>O</sub> = LOW
I <sub>CCH</sub>	Power Supply Current ('F399)		22	34	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current ('F399)		22	34	mA	Max	V <sub>O</sub> = LOW

Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f <sub>max</sub>	Input Clock Frequency	100	140		80		100		MHz	2-1
t <sub>PLH</sub>	Propagation Delay	3.0*	5.7	7.5	3.0	9.5	3.0	8.5	ns	2-3
t <sub>PHL</sub>	CP to Q or $\bar{Q}$	3.0	6.8	9.0	3.0	11.5	3.0	10.0		

\*F398 3.3 ns

## AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> , V <sub>CC</sub> = Mil		T <sub>A</sub> , V <sub>CC</sub> = Com			
		Min	Max	Min	Max	Min	Max		
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW I <sub>n</sub> to CP	3.0 3.0		4.5 4.5		3.0 3.0		ns	2-6
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW I <sub>n</sub> to CP	1.0 1.0		1.5 1.5		1.0 1.0			
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW S to CP ('F398)	7.5 7.5		10.5 10.5		8.5 8.5		ns	2-6
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW S to CP ('F399)	7.5 7.5		9.5 9.5		8.5 8.5			
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW S to CP	0 0		0 0		0 0		ns	2-4
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP Pulse Width HIGH or LOW	4.0 5.0		4.0 7.0		4.0 5.0			

Pin Names	Description	U.L.	
		HIGH/LOW	Input/Output
SR-2	Polynomial Select Inputs	1.0/1.0	20 mA/-0.8 mA
D	Data Input	1.0/1.0	20 mA/-0.8 mA
CP	Clock Input (Operates on HIGH-to-LOW Transition)	1.0/1.0	20 mA/-0.8 mA
CWE	Check Word Enable Input	1.0/1.0	20 mA/-0.8 mA
P	Preset (Active LOW) Input	1.0/1.0	20 mA/-0.8 mA
MR	Master Reset (Active HIGH) Input	1.0/1.0	20 mA/-0.8 mA
Q	Data Output	50/53	1 mA/20 mA
ER	Error Output	50/53	1 mA/20 mA



# 54F/74F401

## CRC Generator/Checker

### General Description

The 'F401 Cycle Redundancy Check (CRC) Generator/Checker provides an advanced tool for implementing the most widely used error detection scheme in serial digital data handling systems. A 3-bit control input selects one-of-eight generator polynomials. The list of polynomials includes CRC-16 and CRC-CCITT as well as their reciprocals (reverse polynomials). Automatic right justification is incorporated for polynomials of degree less than 16. Separate clear and preset inputs are provided for floppy disk and other applications. The Error output indicates whether or not a transmission error has occurred. Another control input inhibits its feedback during check word transmission. The 'F401 is fully compatible with all TTL families.

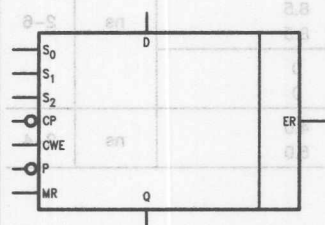
### Features

- Eight selectable polynomials
- Error indicator
- Separate preset and clear controls
- Automatic right justification
- Fully compatible with all TTL logic families
- 14-pin package
- 9401 equivalent
- Typical applications:

Floppy and other disk storage systems  
Digital cassette and cartridge systems  
Data communication systems

### Ordering Code: See Section 5

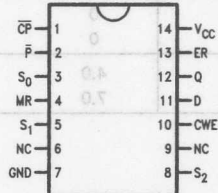
### Logic Symbol



TL/F/9534-4

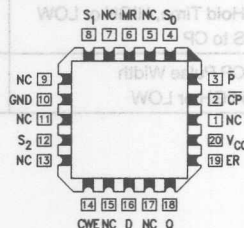
### Connection Diagrams

#### Pin Assignment for DIP, SOIC and Flatpak



TL/F/9534-1

#### Pin Assignment for LCC



TL/F/9534-2

### Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I <sub>IH</sub> /I <sub>IL</sub> Output I <sub>OH</sub> /I <sub>OL</sub>
S <sub>0</sub> -S <sub>2</sub>	Polynomial Select Inputs	1.0/1.0	20 μA/ -0.6 mA
D	Data Input	1.0/1.0	20 μA/ -0.6 mA
CP	Clock Input (Operates on HIGH-to-LOW Transition)	1.0/1.0	20 μA/ -0.6 mA
CWE	Check Word Enable Input	1.0/1.0	20 μA/ -0.6 mA
P	Preset (Active LOW) Input	1.0/1.0	20 μA/ -0.6 mA
MR	Master Reset (Active HIGH) Input	1.0/1.0	20 μA/ -0.6 mA
Q	Data Output	50/33.3	-1 mA/20 mA
ER	Error Output	50/33.3	-1 mA/20 mA

## Functional Description

The 'F401 is a 16-bit programmable device which operates on serial data streams and provides a means of detecting transmission errors. Cyclic encoding and decoding schemes for error detection are based on polynomial manipulation in modulo arithmetic. For encoding, the data stream (message polynomial) is divided by a selected polynomial. This division results in a remainder which is appended to the message as check bits. For error checking, the bit stream containing both data and check bits is divided by the same selected polynomial. If there are no detectable errors, this division results in a zero remainder. Although it is possible to choose many generating polynomials of a given degree, standards exist that specify a small number of useful polynomials. The 'F401 implements the polynomials listed in Table I by applying the appropriate logic levels to the select pins  $S_0$ ,  $S_1$  and  $S_2$ .

The 'F401 consists of a 16-bit register, a Read Only Memory (ROM) and associated control circuitry as shown in the block diagram. The polynomial control code presented at inputs  $S_0$ ,  $S_1$  and  $S_2$  is decoded by the ROM, selecting the desired polynomial by establishing shift mode operation on the register with Exclusive OR gates at appropriate inputs. To generate the check bits, the data stream is entered via the Data inputs (D), using the HIGH-to-LOW transition of the

Clock input ( $\overline{CP}$ ). This data is gated with the most significant output (Q) of the register, and controls the Exclusive OR gates (Figure 1). The Check Word Enable (CWE) must be held HIGH while the data is being entered. After the last data bit is entered, the CWE is brought LOW and the check bits are shifted out of the register and appended to the data bits using external gating (Figure 2).

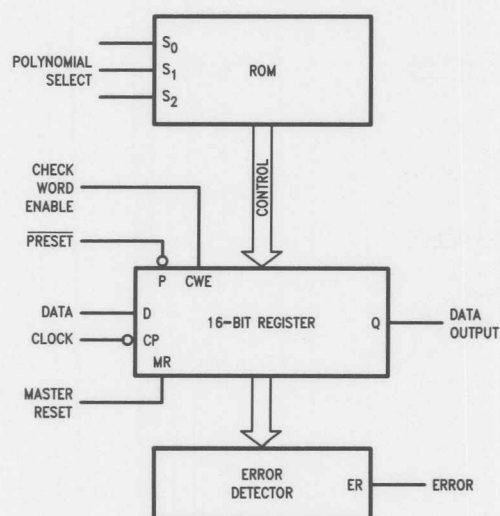
To check an incoming message for errors, both the data and check bits are entered through the D input with the CWE input held HIGH. The 'F401 is not in the data path, but only monitors the message. The Error Output becomes valid after the last check bit has been entered into the 'F401 by a HIGH-to-LOW transition of  $\overline{CP}$ . If no detectable errors have occurred during the data transmission, the resultant internal register bits are all LOW and the Error Output (ER) is LOW. If a detectable error has occurred, ER is HIGH.

A HIGH on the Master Reset input (MR) asynchronously clears the register. A LOW on the Preset input ( $\overline{P}$ ) asynchronously sets the entire register if the control code inputs specify a 16-bit polynomial; in the case of 12- or 8-bit check polynomials only the most significant 12 or 8 register bits are set and the remaining bits are cleared.

TABLE I

Select Code			Polynomial	Remarks
$S_2$	$S_1$	$S_0$		
L	L	L	$X^{16} + X^{15} + X^2 + 1$	CRC-16
L	L	H	$X^{16} + X^{14} + X + 1$	CRC-16 REVERSE
L	H	L	$X^{16} + X^{15} + X^{13} + X^7 + X^4 + X^2 + X + 1$	CRC-12
L	H	H	$X^{12} + X^{11} + X^3 + X^2 + X + 1$	
H	L	L	$X^8 + X^7 + X^5 + X^4 + X + 1$	LRC-8
H	L	H	$X^8 + 1$	
H	H	L	$X^{16} + X^{12} + X^5 + 1$	CRC-CCITT
H	H	H	$X^{16} + X^{11} + X^4 + 1$	CRC-CCITT REVERSE

## Block Diagram



TL/F/9534-5



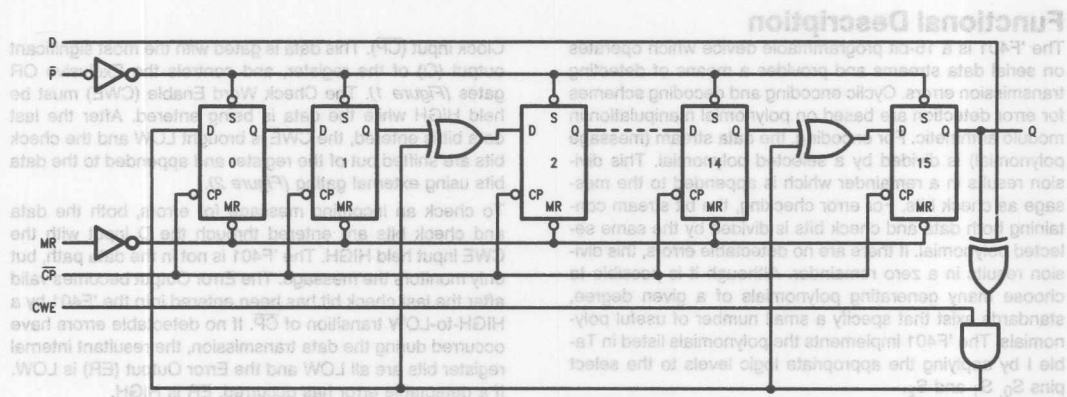


FIGURE 1. Equivalent Circuit for  $X^{16} + X^{15} + X^2 + 1$

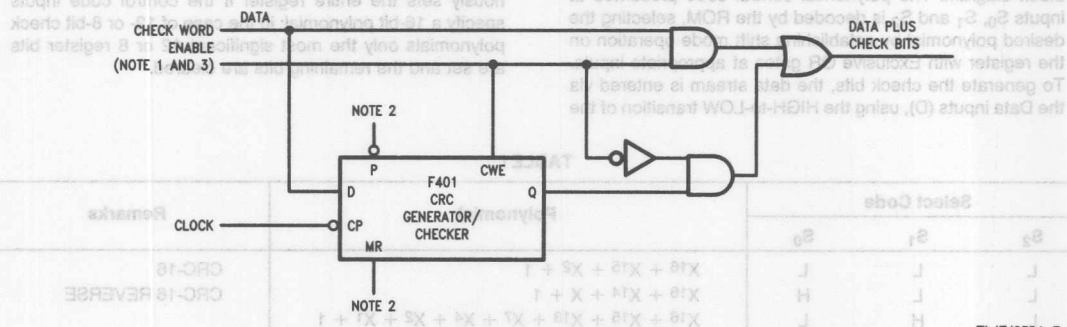
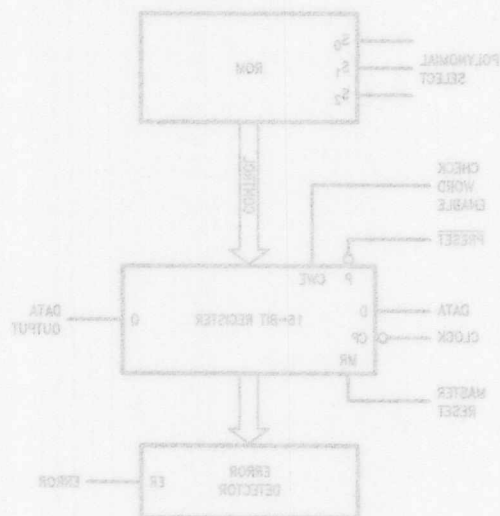


FIGURE 2. Check Word Generation

**Note 1:** Check word Enable is HIGH while data is being clocked, LOW while transmission of check bits.

**Note 2:** F401 must be reset or preset before each computation.

**Note 3:** CRC check bits are generated and appended to data bits.



**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	-55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		70	105	mA	Max	V <sub>O</sub> = HIGH

Symbol	Parameter	$V_{CC} = +5.0V$ $C_L = 50\text{ pF}$			$I_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	100					85		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay $\overline{\text{CP}}$ to Q	4.5		11.5			4.5	13.5	ns	2-3
$t_{\text{PHL}}$	Propagation Delay MR to Q	4.0		10.0			4.0	11.0	ns	2-3
$t_{\text{PHL}}$	Propagation Delay MR to Q	3.0		7.5			3.0	8.0	ns	2-3
$t_{\text{PLH}}$	Propagation Delay $\overline{\text{P}}$ to Q	3.0		8.5			3.0	9.5	ns	2-3
$t_{\text{PHL}}$	Propagation Delay MR to ER	3.5		11.0			3.5	12.0	ns	2-3
$t_{\text{PLH}}$	Propagation Delay $\overline{\text{P}}$ to ER	3.0		8.5			3.0	10.0	ns	2-3
$t_{\text{PLH}}$	Propagation Delay $\overline{\text{CP}}$ to ER	5.0		13.0			5.0	14.5	ns	2-3
$t_{\text{PHL}}$	Propagation Delay $\overline{\text{CP}}$ to ER	4.5		11.5			4.5	12.5	ns	2-3

### AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Set-up Time, HIGH or LOW	5.0				5.5			
$t_s(\text{L})$	D to $\overline{\text{CP}}$	5.0				5.5			
$t_s(\text{H})$	Set-up Time, HIGH or LOW	4.0				4.5		ns	2-6
$t_s(\text{L})$	CWE to $\overline{\text{CP}}$	4.0				4.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0				2.0			
$t_h(\text{L})$	D and CWE to $\overline{\text{CP}}$	2.0				2.0			
$t_w(\text{L})$	$\overline{\text{P}}$ Pulse Width, LOW	7.0				8.0		ns	2-4
$t_w(\text{H})$	Clock Pulse Width,	5.0				6.0			
$t_w(\text{L})$	HIGH or LOW	5.0				6.0		ns	2-4
$t_w(\text{H})$	MR Pulse Width, HIGH	5.0				5.5		ns	2-4
$t_{\text{rec}}$	Recovery Time MR to $\overline{\text{CP}}$	4.0				4.5		ns	2-6
$t_{\text{rec}}$	Recovery Time $\overline{\text{P}}$ to $\overline{\text{CP}}$	2.0				2.0		ns	2-6

## 54F/74F402 Serial Data Polynomial Generator/Checker

### General Description

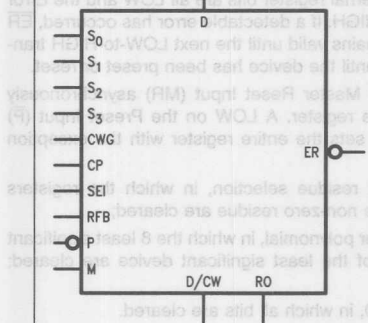
The 'F402 expandable Serial Data Polynomial generator/checker is an expandable version of the 'F401. It provides an advanced tool for the implementation of the most widely used error detection scheme in serial digital handling systems. A 4-bit control input selects one-of-six generator polynomials. The list of polynomials includes CRC-16, CRC-CCITT and Ethernet®, as well as three other standard polynomials (56<sup>th</sup> order, 48<sup>th</sup> order, 32<sup>nd</sup> order). Individual clear and preset inputs are provided for floppy disk and other applications. The Error output indicates whether or not a transmission error has occurred. The CWG Control input inhibits feedback during check word transmission. The 'F402 is compatible with FAST® devices and with all TTL families.

### Features

- Guaranteed 30 MHz data rate
- Six selectable polynomials
- Other polynomials available
- Separate preset and clear controls
- Expandable
- Automatic right justification
- Error output open collector
- Typical applications:  
Floppy and other disk storage systems  
Digital cassette and cartridge systems  
Data communication systems
- Available in SOIC, (300 mil only)

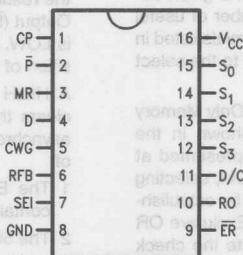
**Ordering Code:** See Section 5

### Logic Symbol



TL/F/9535-4

**Pin Assignment  
for DIP, SOIC and Flatpak**



TL/F/9535-1

**Pin Assignment  
for LCC**



TL/F/9535-2

## Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
S <sub>0</sub> –S <sub>3</sub>	Polynomial Select Inputs	1.0/0.67	20 $\mu$ A/–0.4 mA
CWG	Check Word Generate Input	1.0/0.67	20 $\mu$ A/–0.4 mA
D/CW	Serial Data/Check Word	285(100)/13.3(6.7)	–5.7 mA(–2 mA)/8 mA (4 mA)
D	Data Input	1.0/0.67	20 $\mu$ A/–0.4 mA
$\overline{ER}$	Error Output	* /26.7(13.3)	* /16 mA (8 mA)
RO	Register Output	285(100)/13.3(6.7)	–5.7 mA(–2 mA)/8 mA (4 mA)
CP	Clock Pulse	1.0/0.67	20 $\mu$ A/–0.4 mA
SEI	Serial Expansion Input	1.0/0.67	20 $\mu$ A/–0.4 mA
RFB	Register Feedback	1.0/0.67	20 $\mu$ A/–0.4 mA
MR	Master Reset	1.0/0.67	20 $\mu$ A/–0.4 mA
P	Preset	1.0/0.67	20 $\mu$ A/–0.4 mA

\*Open Collector

## Functional Description

The 'F402 Serial Data Polynomial Generator/Checker is an expandable 16-bit programmable device which operates on serial data streams and provides a means of detecting transmission errors. Cyclic encoding and decoding schemes for error detection are based on polynomial manipulation in modulo arithmetic. For encoding, the data stream (message polynomial) is divided by a selected polynomial. This division results in a remainder (or residue) which is appended to the message as check bits. For error checking, the bit stream containing both data and check bits is divided by the same selected polynomial. If there are no detectable errors, this division results in a zero remainder. Although it is possible to choose many generating polynomials of a given degree, standards exist that specify a small number of useful polynomials. The 'F402 implements the polynomials listed in Table I by applying the appropriate logic levels to the select pins S<sub>0</sub>, S<sub>1</sub>, S<sub>2</sub> and S<sub>3</sub>.

The 'F402 consists of a 16-bit register, a Read Only Memory (ROM) and associated control circuitry as shown in the Block Diagram. The polynomial control code presented at inputs S<sub>0</sub>, S<sub>1</sub>, S<sub>2</sub> and S<sub>3</sub> is decoded by the ROM, selecting the desired polynomial or part of a polynomial by establishing shift mode operation on the register with Exclusive OR (XOR) gates at appropriate inputs. To generate the check bits, the data stream is entered via the Data Inputs (D), using the LOW-to-HIGH transition of the Clock Input (CP). This data is gated with the most significant Register Output (RO) via the Register Feedback Input (RFB), and controls the

XOR gates. The Check Word Generate (CWG) must be held HIGH while the data is being entered. After the last data bit is entered, the CWG is brought LOW and the check bits are shifted out of the register(s) and appended to the data bits (no external gating is needed).

To check an incoming message for errors, both the data and check bits are entered through the D Input with the CWG Input held HIGH. The Error Output becomes valid after the last check bit has been entered into the 'F402 by a LOW-to-HIGH transition of CP, with the exception of the Ethernet polynomial (see Applications paragraph). If no detectable errors have occurred during the data transmission, the resultant internal register bits are all LOW and the Error Output ( $\overline{ER}$ ) is HIGH. If a detectable error has occurred,  $\overline{ER}$  is LOW.  $\overline{ER}$  remains valid until the next LOW-to-HIGH transition of CP or until the device has been preset or reset.

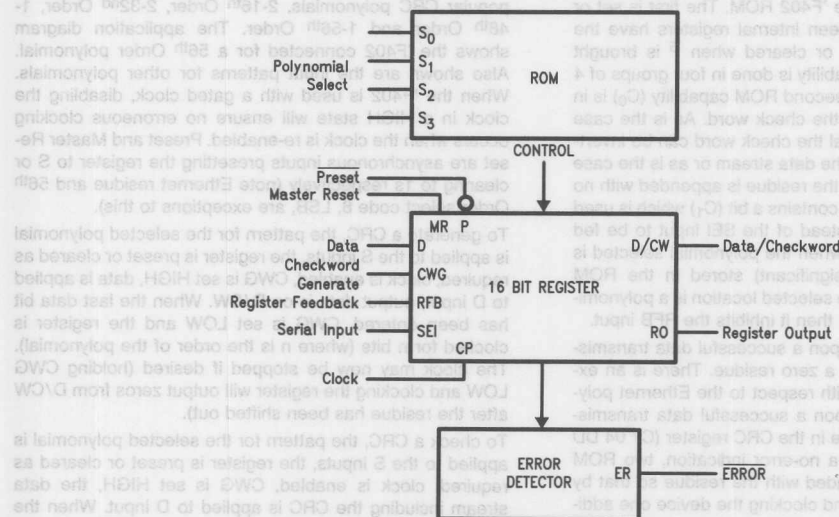
A HIGH on the Master Reset Input (MR) asynchronously clears the entire register. A LOW on the Preset Input (P) asynchronously sets the entire register with the exception of:

- 1 The Ethernet residue selection, in which the registers containing the non-zero residue are cleared;
- 2 The 56th order polynomial, in which the 8 least significant register bits of the least significant device are cleared; and,
- 3 Register S=0, in which all bits are cleared.

TABLE I

Hex	S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	Polynomial	Remarks
0	L	L	L	L	0	S = 0
C	H	H	L	L	$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} +$	Ethernet
D	H	H	L	H	$X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$	Polynomial
E	H	H	H	L	$X^{32} + X^{31} + X^{27} + X^{26} + X^{25} + X^{19} + X^{16} +$	Ethernet
F	H	H	H	H	$X^{15} + X^{13} + X^{12} + X^{11} + X^9 + X^7 + X^6 + X^5 + X^4 + X^2 + X + 1$	Residue
7	L	H	H	H	$X^{16} + X^{15} + X^2 + 1$	CRC-16
B	H	L	H	H	$X^{16} + X^{12} + X^5 + 1$	CRC-CCITT
3	L	L	H	H	$X^{56} + X^{55} + X^{49} + X^{45} + X^{41} +$	56th Order
2	L	L	H	L	$X^{39} + X^{38} + X^{37} + X^{36} + X^{31} +$	
4	L	H	L	L	$X^{22} + X^{19} + X^{17} + X^{16} + X^{15} + X^{14} + X^{12} + X^{11} + X^9 +$	
8	H	L	L	L	$X^5 + X + 1$	
5	L	H	L	H	$X^{48} + X^{36} + X^{35} +$	48th Order
9	H	L	L	H	$X^{23} + X^{21} +$	
1	L	L	L	H	$X^{15} + X^{13} + X^8 + X^2 + 1$	
6	L	H	H	L	$X^{32} + X^{23} + X^{21} +$	32nd Order
A	H	L	H	L	$X^{11} + X^2 + 1$	

## Block Diagram



TL/F/9535-5



TABLE II

Select Code	P <sub>3</sub>	P <sub>2</sub>	P <sub>1</sub>	P <sub>0</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>	Polynomial
0	0	0	0	0	1	0	0	S = 0
C	1	1	1	1	1	0	1	Ethernet
D	1	1	1	1	1	0	1	Polynomial
E	0	0	0	0	0	0	0	Ethernet
F	0	0	0	0	0	1	0	Residue
7	1	1	1	1	1	0	0	CRC-16
B	1	1	1	1	1	0	0	CRC-CCITT
3	1	1	1	1	1	0	0	56th Order
2	1	1	1	1	1	0	0	
4	1	1	1	1	1	0	0	
8	0	0	1	1	1	0	0	
5	1	1	1	1	1	0	0	48th Order
9	1	1	1	1	1	0	0	
1	1	1	1	1	1	0	0	
6	1	1	1	1	1	0	0	32nd Order
A	1	1	1	1	1	0	0	

## Applications

In addition to polynomial selection there are four other capabilities provided for in the 'F402 ROM. The first is set or clear selectability. The sixteen internal registers have the capability to be either set or cleared when  $\bar{P}$  is brought LOW. This set or clear capability is done in four groups of 4 (see Table II, P<sub>0</sub>-P<sub>3</sub>). The second ROM capability (C<sub>0</sub>) is in determining the polarity of the check word. As is the case with the Ethernet polynomial the check word can be inverted when it is appended to the data stream or as is the case with the other polynomials, the residue is appended with no inversion. Thirdly, the ROM contains a bit (C<sub>1</sub>) which is used to select the RFB input instead of the SEI input to be fed into the LSB. This is used when the polynomial selected is actually a residue (least significant) stored in the ROM which indicates whether the selected location is a polynomial or a residue. If the latter, then it inhibits the RFB input.

As mentioned previously, upon a successful data transmission, the CRC register has a zero residue. There is an exception to this, however, with respect to the Ethernet polynomial. This polynomial, upon a successful data transmission, has a non-zero residue in the CRC register (C7 04 DD 7B)<sub>16</sub>. In order to provide a no-error indication, two ROM locations have been preloaded with the residue so that by selecting these locations and clocking the device one additional time, after the last check bit has been entered, will result in zeroing the CRC register. In this manner a no-error indication is achieved.

With the present mix of polynomials, the largest is 56th order requiring four devices while the smallest is 16th order requiring just one device. In order to accommodate multiplexing between high order polynomials (X 16th order) and lower order polynomials, a location of all zeros is provided. This allows the user to choose a lower order polynomial even if the system is configured for a higher order one.

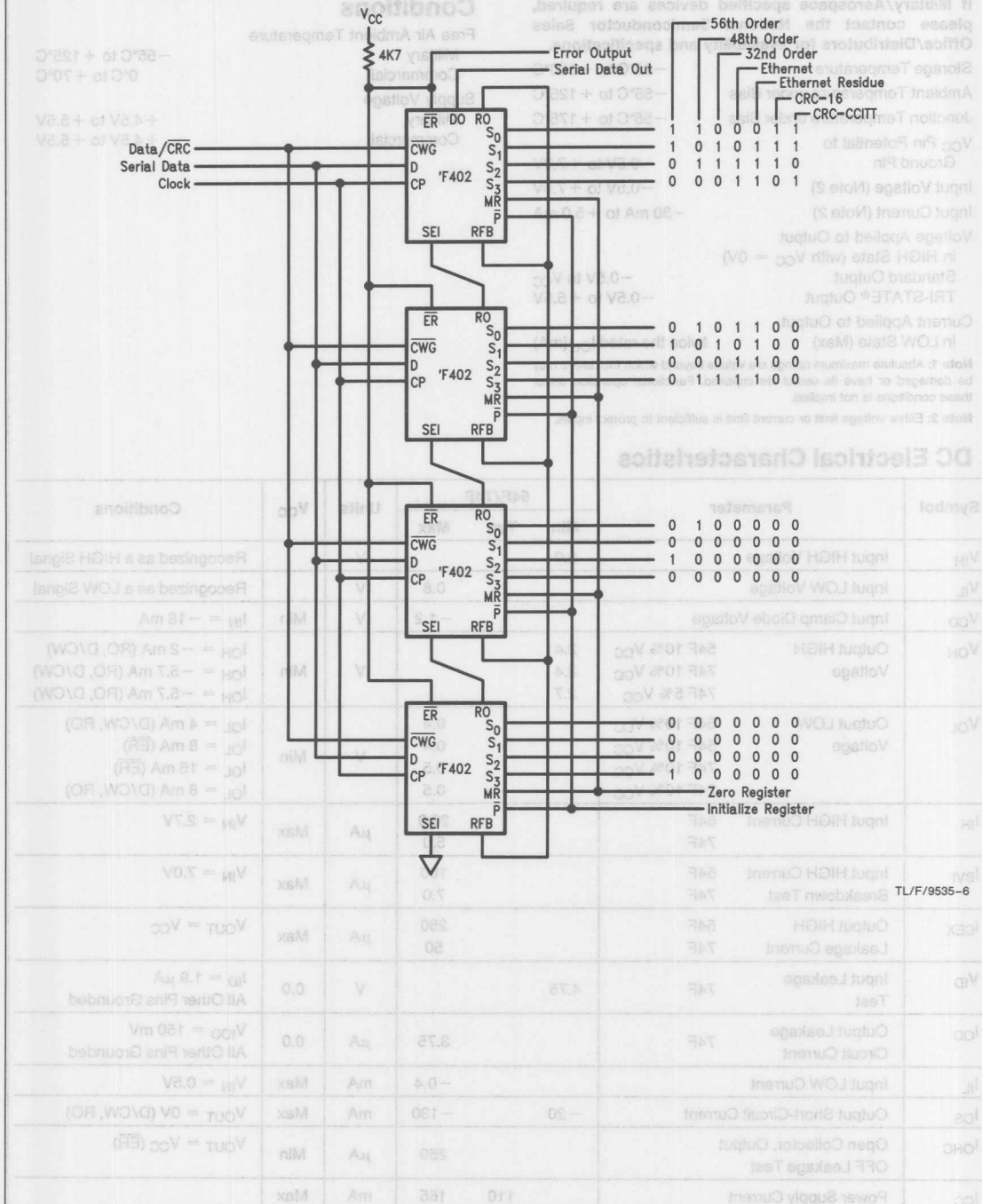
The 'F402 expandable CRC generator checker contains 6 popular CRC polynomials, 2-16th Order, 2-32nd Order, 1-48th Order and 1-56th Order. The application diagram shows the 'F402 connected for a 56th Order polynomial. Also shown are the input patterns for other polynomials. When the 'F402 is used with a gated clock, disabling the clock in a HIGH state will ensure no erroneous clocking occurs when the clock is re-enabled. Preset and Master Reset are asynchronous inputs presetting the register to S or clearing to 1s respectively (note Ethernet residue and 56th Order select code 8, LSB, are exceptions to this).

To generate a CRC, the pattern for the selected polynomial is applied to the S inputs, the register is preset or cleared as required, clock is enabled, CWG is set HIGH, data is applied to D input, output data is on D/CW. When the last data bit has been entered, CWG is set LOW and the register is clocked for n bits (where n is the order of the polynomial). The clock may now be stopped if desired (holding CWG LOW and clocking the register will output zeros from D/CW after the residue has been shifted out).

To check a CRC, the pattern for the selected polynomial is applied to the S inputs, the register is preset or cleared as required, clock is enabled, CWG is set HIGH, the data stream including the CRC is applied to D input. When the last bit of the CRC has been entered, the  $\bar{E}R$  output is checked: HIGH = error free data, LOW = corrupt data. The clock may now be stopped if desired.

To implement polynomials of lower order than 56th, select the number of packages required for the order of polynomial and apply the pattern for the selected polynomial to the S inputs (0000 on S inputs disables the package from the feedback chain).

## Applications (Continued)



**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.4		V	Min	I <sub>OH</sub> = −2 mA (RO, D/CW)
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −5.7 mA (RO, D/CW)
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −5.7 mA (RO, D/CW)
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.4	V	Min	I <sub>OL</sub> = 4 mA (D/CW, RO)
		54F 10% V <sub>CC</sub>		0.4			I <sub>OL</sub> = 8 mA (ER)
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 16 mA (ER)
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 8 mA (D/CW, RO)
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.4	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	−20	−130		mA	Max	V <sub>OUT</sub> = 0V (D/CW, RO)
I <sub>OHC</sub>	Open Collector, Output OFF Leakage Test			250	μA	Min	V <sub>OUT</sub> = V <sub>CC</sub> (ER)
I <sub>CC</sub>	Power Supply Current		110	165	mA	Max	

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	30	45		30		30		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	8.5	15.0	19.0	7.5	26.5	7.5	21.0	ns	2-3
$t_{\text{PHL}}$	CP to D/CW	10.5	18.0	23.0	9.5	26.5	9.5	25.0		
$t_{\text{PLH}}$	Propagation Delay	8.0	13.5	17.0	7.0	26.0	7.0	19.0	ns	2-3
$t_{\text{PHL}}$	CP to RO	8.0	14.0	18.0	7.0	22.5	7.0	20.0		
$t_{\text{PLH}}$	Propagation Delay	15.5	26.0	33.0	14.0	38.5	14.0	35.0	ns	2-3
$t_{\text{PHL}}$	CP to ER	8.5	14.5	18.5	7.5	23.5	7.5	20.5		
$t_{\text{PLH}}$	Propagation Delay	11.0	18.5	23.5	10.0	31.0	10.0	25.5	ns	2-3
$t_{\text{PHL}}$	$\bar{P}$ to D/CW	11.5	19.5	24.5	10.5	32.0	10.5	26.5		
$t_{\text{PLH}}$	Propagation Delay	9.5	16.0	20.5	8.5	31.5	8.5	22.5	ns	2-3
$t_{\text{PHL}}$	$\bar{P}$ to RO									
$t_{\text{PLH}}$	Propagation Delay	10.0	17.0	21.5	9.0	26.0	9.0	23.5	ns	2-3
$t_{\text{PHL}}$	$\bar{P}$ to ER									
$t_{\text{PLH}}$	Propagation Delay	10.5	18.0	23.0	9.5	29.0	9.5	25.5	ns	2-3
$t_{\text{PHL}}$	MR to D/CW	11.0	19.0	24.0	10.0	28.5	10.0	26.0		
$t_{\text{PHL}}$	Propagation Delay	9.0	15.5	19.5	8.0	23.5	8.0	21.5	ns	2-3
$t_{\text{PLH}}$	MR to RO									
$t_{\text{PLH}}$	Propagation Delay	16.5	28.0	35.5	14.5	39.0	14.5	37.5	ns	2-3
$t_{\text{PHL}}$	MR to ER									
$t_{\text{PLH}}$	Propagation Delay	6.0	10.5	13.5	5.0	19.5	5.0	15.0	ns	2-3
$t_{\text{PHL}}$	D to D/CW	7.5	12.0	16.0	6.5	20.0	6.5	18.0		
$t_{\text{PLH}}$	Propagation Delay	6.5	11.0	14.0	5.5	21.5	5.5	15.5	ns	2-3
$t_{\text{PHL}}$	CWG to D/CW	7.0	12.0	15.5	6.0	21.5	6.0	17.5		
$t_{\text{PLH}}$	Propagation Delay	11.5	19.5	24.5	9.0	29.0	10.5	26.5	ns	2-3
$t_{\text{PHL}}$	$S_n$ to D/CW	9.5	16.0	20.0	8.5	25.0	8.5	22.0		

# AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	4.5		6.0		5.0		ns	2-6
$t_s(\text{L})$	SEI to CP	4.5		6.0		5.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		1.0		0		ns	2-6
$t_h(\text{L})$	SEI to CP	0		1.0		0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	11.0		14.0		12.5		ns	2-6
$t_s(\text{L})$	RFB to CP	11.0		14.0		12.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		0		0		ns	2-6
$t_h(\text{L})$	RFB to CP	0		0		0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	13.5		16.0		15.0		ns	2-6
$t_s(\text{L})$	$S_1$ to CP	13.0		15.5		14.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		0		0		ns	2-6
$t_h(\text{L})$	$S_1$ to CP	0		0		0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	9.0		11.5		10.0		ns	2-6
$t_s(\text{L})$	D to CP	9.0		11.5		10.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		0		0		ns	2-6
$t_h(\text{L})$	D to CP	0		0		0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	7.0		9.0		8.0		ns	2-6
$t_s(\text{L})$	CWG to CP	5.5		8.0		6.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		0		0		ns	2-6
$t_h(\text{L})$	CWG to CP	0		0		0			
$t_w(\text{H})$	Clock Pulse Width	4.0		7.0		4.5		ns	2-4
$t_w(\text{L})$	HIGH or LOW	4.0		5.0		4.5		ns	2-4
$t_w(\text{H})$	MR Pulse Width, HIGH	4.0		7.0		4.5		ns	2-4
$t_w(\text{L})$	$\bar{P}$ Pulse Width, LOW	4.0		5.0		4.5		ns	2-4
$t_{\text{rec}}$	Recovery Time MR to CP	3.0		4.0		3.5		ns	2-6
$t_{\text{rec}}$	Recovery Time $\bar{P}$ to CP	5.0		6.5		6.0			

## 54F/74F403A

### First-In First-Out (FIFO) Buffer Memory

#### General Description

The 'F403A is an expandable fall-through type high-speed First-In First-Out (FIFO) Buffer Memory optimized for high-speed disk or tape controllers and communication buffer applications. It is organized as 16-words by 4-bits and may be expanded to any number of words or any number of bits in multiples of four. Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

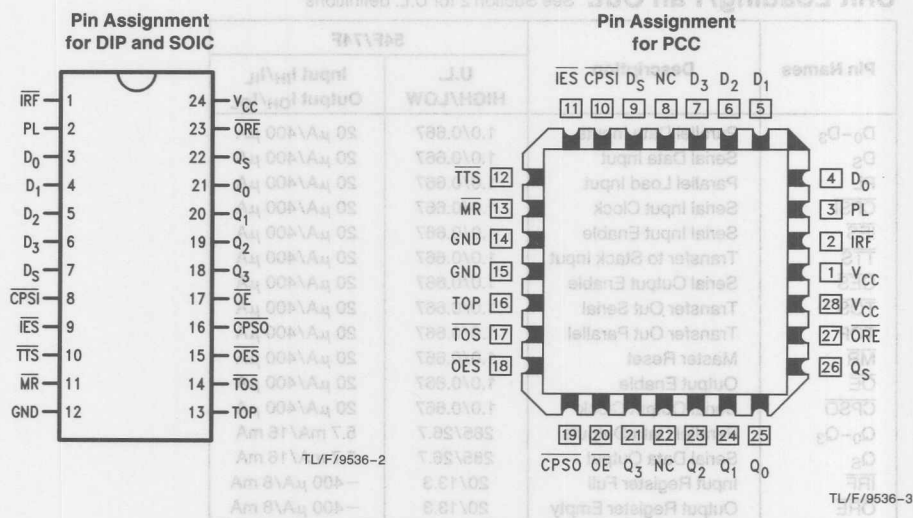
The 'F403A has TRI-STATE® outputs which provide added versatility and is fully compatible with all TTL families.

#### Features

- Serial or parallel input
- Serial or parallel output
- Expandable without external logic
- TRI-STATE outputs
- Fully compatible with all TTL families
- Slim 24-pin package
- 9403A replacement
- Guaranteed 4000V minimum ESD protection

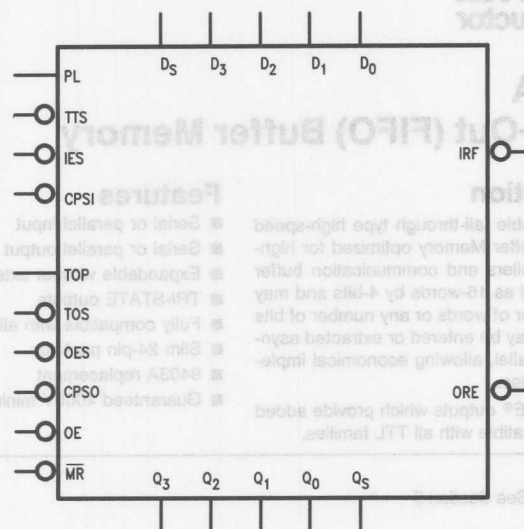
**Ordering Code:** See Section 5

#### Connection Diagrams





## Logic Symbol

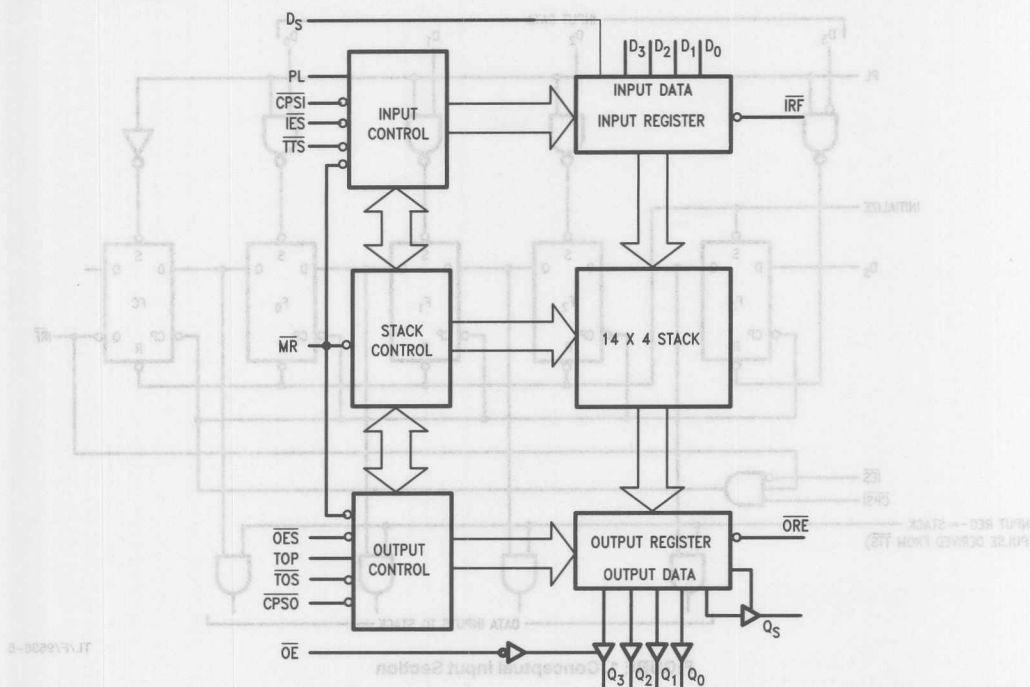


TL/F/9536-1

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
D <sub>0</sub> –D <sub>3</sub>	Parallel Data Inputs	1.0/0.667	20 $\mu$ A/400 $\mu$ A
D <sub>5</sub>	Serial Data Input	1.0/0.667	20 $\mu$ A/400 $\mu$ A
PL	Parallel Load Input	1.0/0.667	20 $\mu$ A/400 $\mu$ A
CPSI	Serial Input Clock	1.0/0.667	20 $\mu$ A/400 $\mu$ A
IES	Serial Input Enable	1.0/0.667	20 $\mu$ A/400 $\mu$ A
TTS	Transfer to Stack Input	1.0/0.667	20 $\mu$ A/400 $\mu$ A
OES	Serial Output Enable	1.0/0.667	20 $\mu$ A/400 $\mu$ A
TOS	Transfer Out Serial	1.0/0.667	20 $\mu$ A/400 $\mu$ A
TOP	Transfer Out Parallel	1.0/0.667	20 $\mu$ A/400 $\mu$ A
MR	Master Reset	1.0/0.667	20 $\mu$ A/400 $\mu$ A
OE	Output Enable	1.0/0.667	20 $\mu$ A/400 $\mu$ A
CPSO	Serial Output Clock	1.0/0.667	20 $\mu$ A/400 $\mu$ A
Q <sub>0</sub> –Q <sub>3</sub>	Parallel Data Outputs	285/26.7	5.7 mA/16 mA
Q <sub>5</sub>	Serial Data Output	285/26.7	5.7 mA/16 mA
IRF	Input Register Full	20/13.3	–400 $\mu$ A/8 mA
ORE	Output Register Empty	20/13.3	–400 $\mu$ A/8 mA

## Block Diagram



## Functional Description

As shown in the block diagram the 'F403A consists of three sections:

1. An Input Register with parallel and serial data inputs as well as control inputs and outputs for input handshaking and expansion.
2. A 4-bit wide, 14-word deep fall-through stack with self-contained control logic.
3. An Output Register with parallel and serial data outputs as well as control inputs and outputs for output handshaking and expansion.

Since these three sections operate asynchronously and almost independently, they will be described separately below.

### INPUT REGISTER (DATA ENTRY)

The Input Register can receive data in either bit-serial or in 4-bit parallel form. It stores this data until it is sent to the fall-through stack and generates the necessary status and control signals.

Figure 1 is a conceptual logic diagram of the input section. As described later, this 5-bit register is initialized by setting

the  $F_3$  flip-flop and resetting the other flip-flops. The  $\bar{Q}$  output of the last flip-flop (FC) is brought out as the 'Input Register Full' output ( $\bar{IRF}$ ). After initialization this output is HIGH.

**Parallel Entry**—A HIGH on the PL input loads the  $D_0$ – $D_3$  inputs into the  $F_0$ – $F_3$  flip-flops and sets the FC flip-flop. This forces the  $\bar{IRF}$  output LOW indicating that the input register is full. During parallel entry, the  $\bar{CPSI}$  input must be LOW. If parallel expansion is not being implemented,  $\bar{IES}$  must be LOW to establish row mastership (see Expansion section).

**Serial Entry**—Data on the  $D_5$  input is serially entered into the  $F_3, F_2, F_1, F_0, FC$  shift register on each HIGH-to-LOW transition of the  $\bar{CPSI}$  clock input, provided  $\bar{IES}$  and PL are LOW.

After the fourth clock transition, the four data bits are located in the four data flip-flops,  $F_0$ – $F_3$ . The FC flip-flop is set, forcing the  $\bar{IRF}$  output LOW and internally inhibiting  $\bar{CPSI}$  clock pulses from affecting the register, Figure 2 illustrates the final positions in a 'F403A resulting from a 64-bit serial bit train.  $B_0$  is the first bit,  $B_{63}$  the last bit.

## Functional Description (Continued)

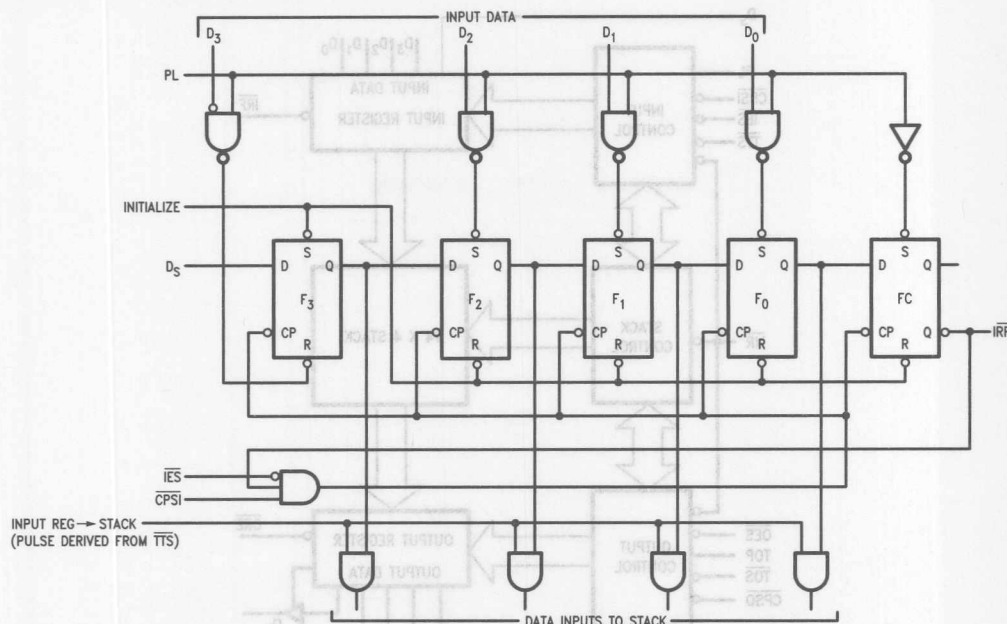


FIGURE 1. Conceptual Input Section

TL/F/9536-5

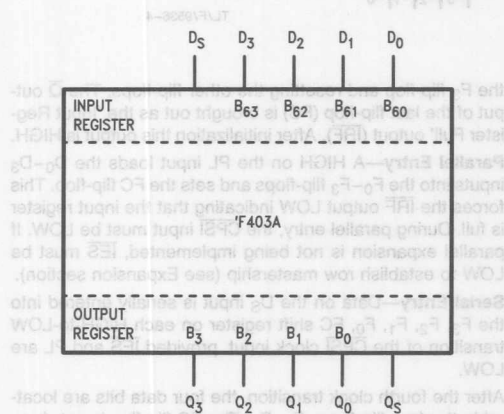


FIGURE 2. Final Positions in a 'F403A Resulting from a 64-Bit Serial Train

**Transfer to the Stack**—The outputs of Flip-Flops F<sub>0</sub>–F<sub>3</sub> feed the stack. A LOW level on the TTS input initiates a 'fail-

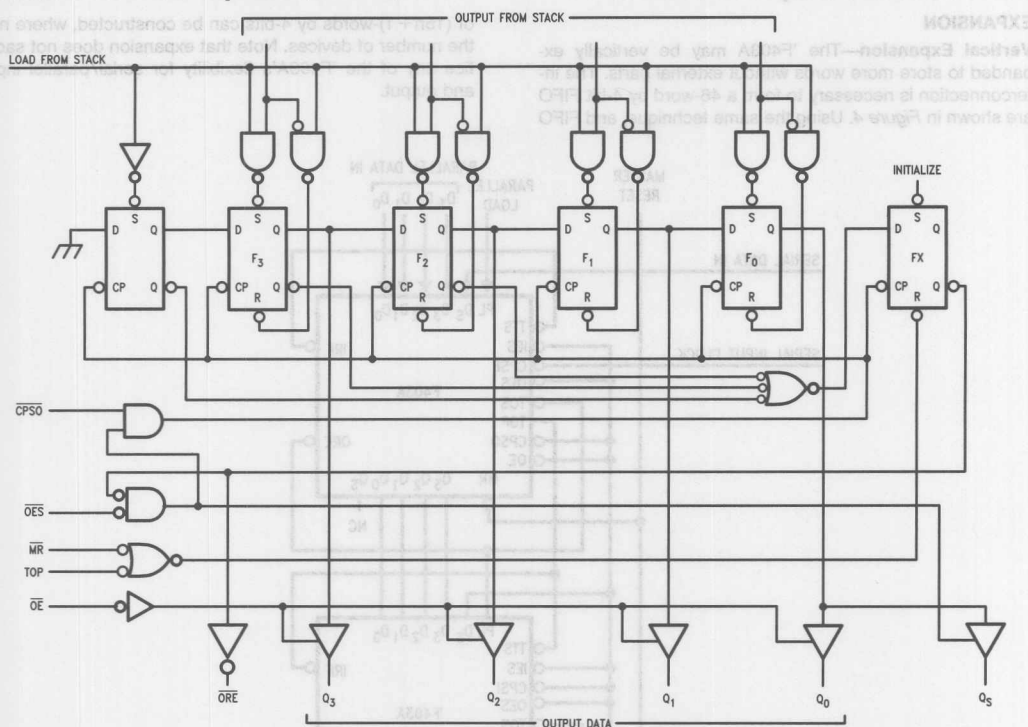
through' action. If the top location of the stack is empty, data is loaded into the stack and the input register is re-initialized. Note that this initialization is postponed until PL is LOW again. Thus, automatic FIFO action is achieved by connecting the IRF output to the TTS input.

An RS Flip-Flop (the Request Initialization Flip-Flop shown in Figure 10) in the control section records the fact that data has been transferred to the stack. This prevents multiple entry of the same word into the stack despite the fact the IRF and TTS may still be LOW. The Request Initialization Flip-Flop is not cleared until PL goes LOW. Once in the stack, data falls through the stack automatically, pausing only when it is necessary to wait for an empty next location. In the 'F403A as in most modern FIFO designs, the MR input only initializes the stack control section and does not clear the data.

**OUTPUT REGISTER (DATA EXTRACTION)**

The Output Register receives 4-bit data words from the bottom stack location, stores it and outputs data on a TRI-STATE 4-bit parallel data bus or on a TRI-STATE serial data bus. The output section generates and receives the necessary status and control signals. Figure 3 is a conceptual logic diagram of the output section.

## Functional Description (Continued)



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FIGURE 3. Conceptual Output Section

**Parallel Data Extraction**—When the FIFO is empty after a LOW pulse is applied to  $\overline{MR}$ , the Output Register Empty ( $\overline{ORE}$ ) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided the 'Transfer Out Parallel' (TOP) input is HIGH. As a result of the data transfer  $\overline{ORE}$  goes HIGH, indicating valid data on the data outputs (provided the TRI-STATE buffer is enabled). TOP can now be used to clock out the next word. When TOP goes LOW,  $\overline{ORE}$  will go LOW indicating that the output data has been extracted, but the data itself remains on the output bus until the next HIGH level at TOP permits the transfer of the next word (if available) into the Output Register. During parallel data extraction  $\overline{CP50}$  should be LOW. TOP should be grounded for single slice operation or connected to the appropriate  $\overline{ORE}$  for expanded operation (see Expansion section).

TOP is not edge triggered. Therefore, if TOP goes HIGH before data is available from the stack, but data does become available before TOP goes LOW again, that data will be transferred into the Output Register. However, internal

control circuitry prevents the same data from being transferred twice. If TOP goes HIGH and returns to LOW before data is available from the stack,  $\overline{ORE}$  remains LOW indicating that there is no valid data at the outputs.

**Serial Data Extraction**—When the FIFO is empty after a LOW pulse is applied to  $\overline{MR}$ , the Output Register Empty ( $\overline{ORE}$ ) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided TOP is LOW and TOP is HIGH. As a result of the data transfer  $\overline{ORE}$  goes HIGH indicating valid data in the register. The TRI-STATE Serial Data Output,  $Q_S$ , is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the HIGH-to-LOW transition of  $\overline{CP50}$ . To prevent false shifting,  $\overline{CP50}$  should be LOW when the new word is being loaded into the Output Register. The fourth transition empties the shift register, forces  $\overline{ORE}$  output LOW and disables the serial output,  $Q_S$  (refer to Figure 3). For serial operation the  $\overline{ORE}$  output may be tied to the TOP input, requesting a new word from the stack as soon as the previous one has been shifted out.

## Functional Description (Continued)

### EXPANSION

**Vertical Expansion**—The 'F403A may be vertically expanded to store more words without external parts. The interconnection is necessary to form a 46-word by 4-bit FIFO are shown in Figure 4. Using the same technique, and FIFO

of  $(15n + 1)$ -words by 4-bits can be constructed, where  $n$  is the number of devices. Note that expansion does not sacrifice any of the 'F403A's flexibility for serial/parallel input and output.

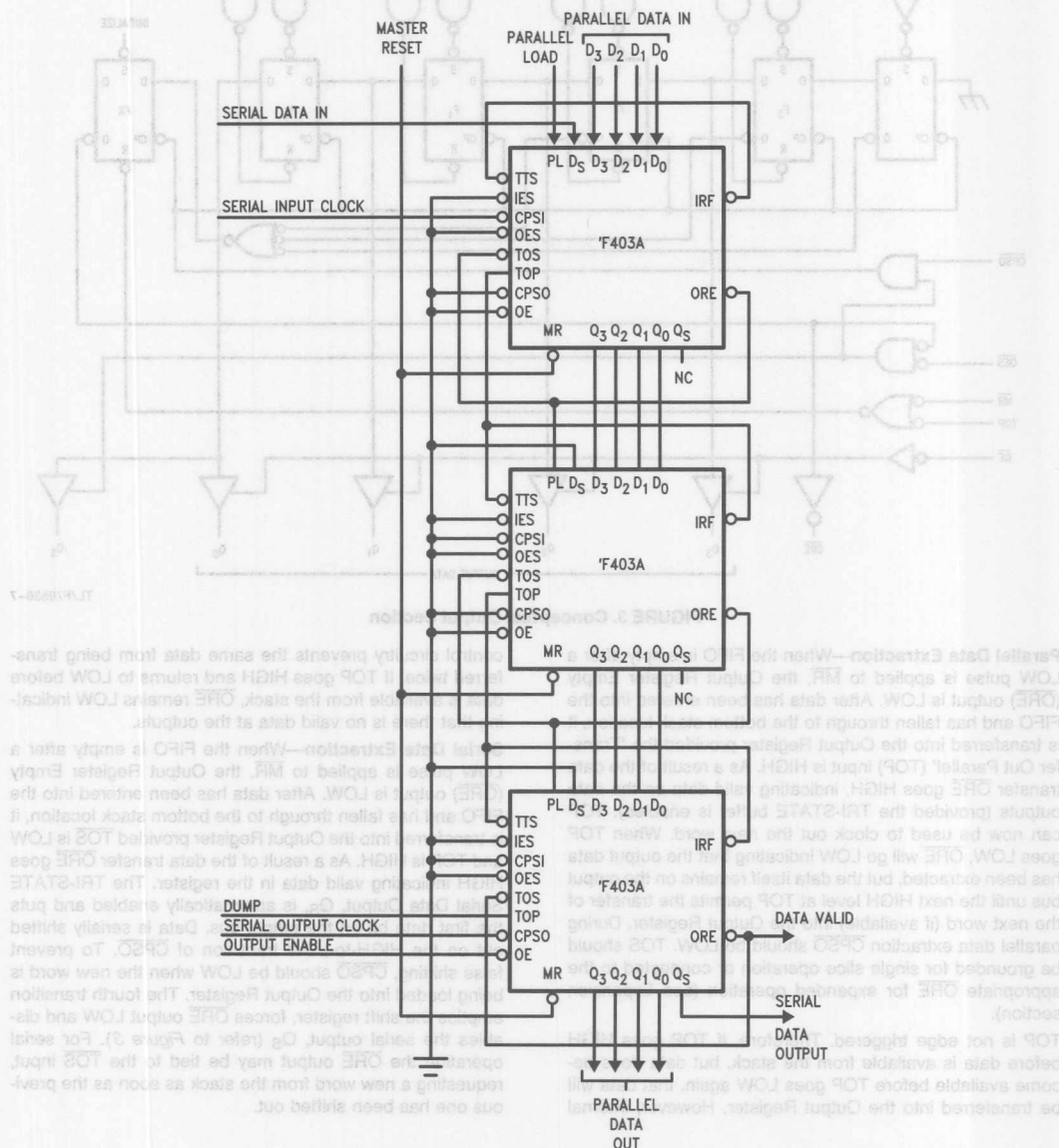


FIGURE 4. A Vertical Expansion Scheme

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## Functional Description (Continued)

**Horizontal and Vertical Expansion**—The 'F403A can be expanded in both the horizontal and vertical directions without any external parts and without sacrificing any of its FIFO's flexibility for serial/parallel input and output. The interconnections necessary to form a 31-word by 16-bit FIFO are shown in Figure 6. Using the same technique, any FIFO of  $(15m + 1)$ -words by  $(4n)$ -bits can be constructed, where  $m$  is the number of devices in a column and  $n$  is the number of devices in a row. Figures 7 and 8 show the timing diagrams for serial data entry and extraction for the 31-word by 16-bit FIFO shown in Figure 6. The final position of data after serial insertion of 496 bits into the FIFO array of Figure 6 is shown in Figure 9.

**Interlocking Circuitry**—Most conventional FIFO designs provide status signals analogous to IRF and ORE. However, when these devices are operated in arrays, variations in unit to unit operating speed require external gating to assure all devices have completed an operation. The 'F403A incorporates simple but effective 'master/slave' interlocking circuitry to eliminate the need for external gating.

In the 'F403A array of Figure 6 devices 1 and 5 are defined as 'row masters' and the other devices are slaves to the master in their row. No slave in a given row will initialize its Input Register until it has received LOW on its IES input from a row master or a slave of higher priority.

In a similar fashion, the ORE outputs of slaves will not go HIGH until their OES inputs have gone HIGH. This interlock-

ing scheme ensures that new input data may be accepted by the array when the IRF output of the final slave in that row goes HIGH and that output data for the array may be extracted when the ORE of the final slave in the output row goes HIGH.

The row master is established by connecting its IES input to ground while a slave receives its IES input from the IRF output of the next higher priority device. When an array of 'F403A FIFOs is initialized with a LOW on the MR inputs of all devices, the IRF outputs of all devices will be HIGH. Thus, only the row master receives a LOW on the IES input during initialization. Figure 10 is a conceptual logic diagram of the internal circuitry which determines master/slave operation. Whenever MR and IES are LOW, the Master Latch is set. Whenever TTS goes LOW the Request Initialization Flip-Flop will be set. If the Master Latch is HIGH, the Input Register will be immediately initialized and the Request Initialization Flip-Flop reset. If the Master Latch is reset, the Input Register is not initialized until IES goes LOW. In array operation, activating the TTS initiates a ripple input register initialization from the row master to the last slave.

A similar operation takes place for the output register. Either a TOS or TOP input initiates a load-from-stack operation and sets the ORE Request Flip-Flop. If the Master Latch is set, the last Output Register Flip-Flop is set and ORE goes HIGH. If the Master Latch is reset, the ORE output will be LOW until an OES input is received.

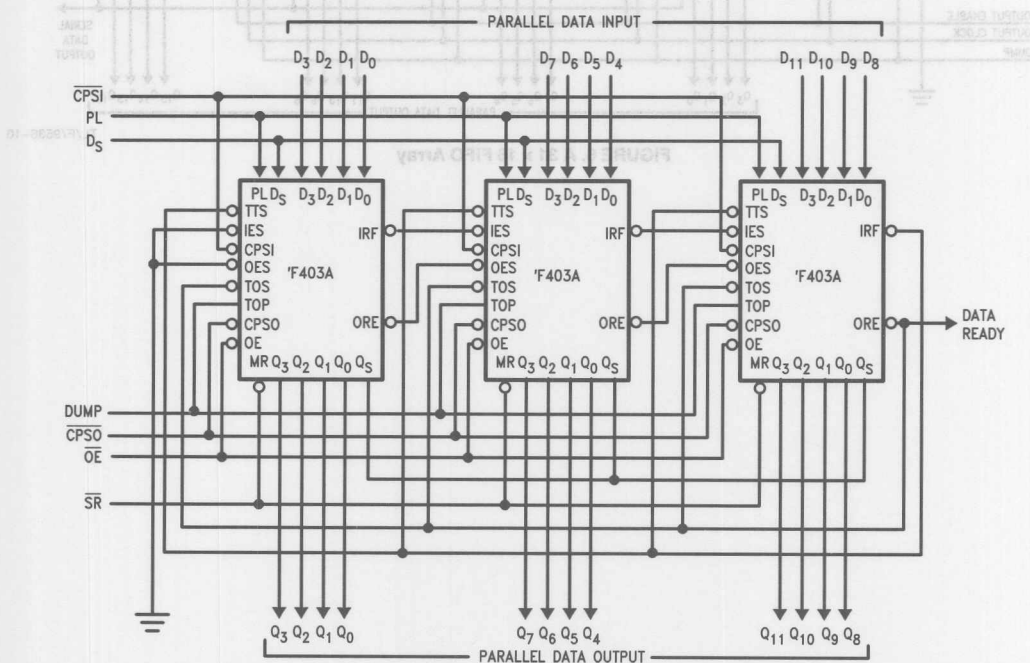


FIGURE 5. A Horizontal Expansion Scheme

TL/F/9536-9



## Functional Description (Continued)

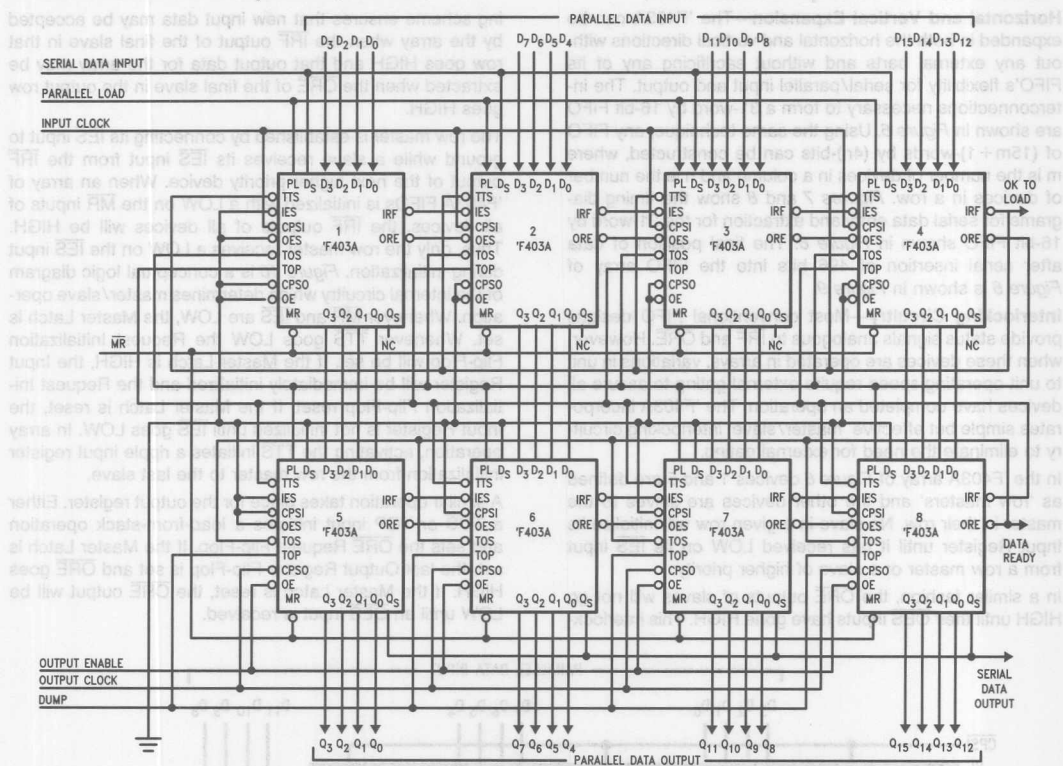


FIGURE 6. A 31 x 16 FIFO Array

TL/F/9536-10

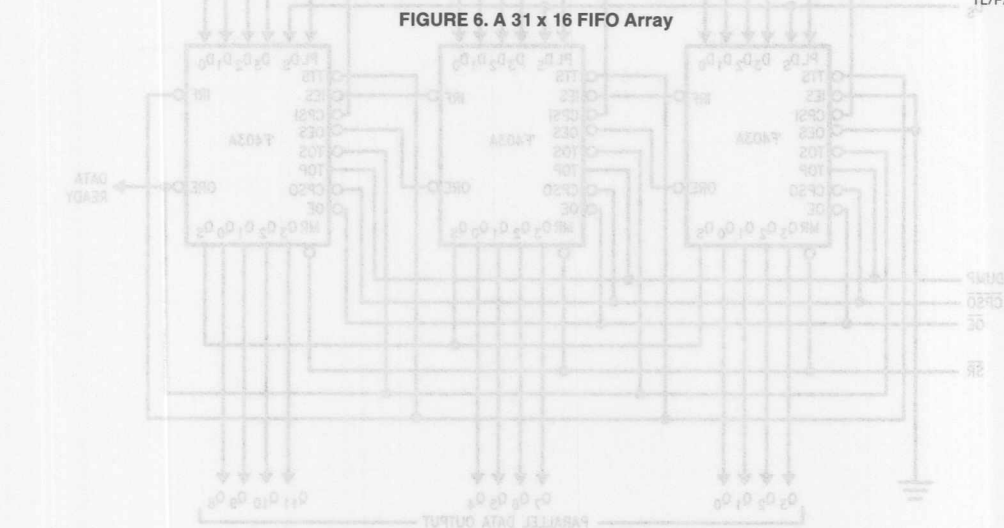


FIGURE 7. A Horizontal Expansion Scheme

## Functional Description (Continued)

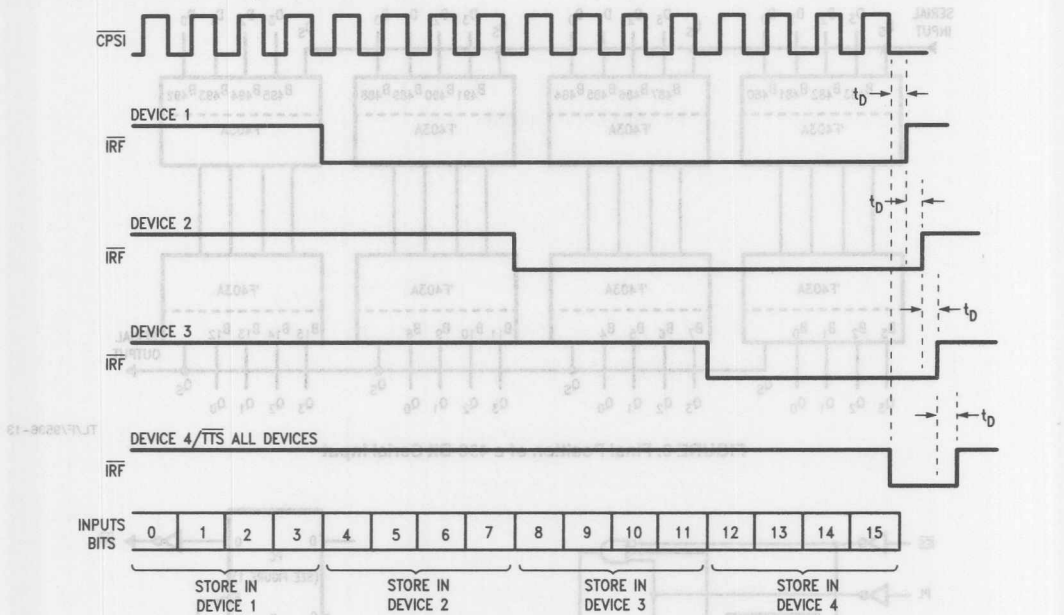


FIGURE 7. Serial Data Entry for Array of Figure 6

TL/F/9536-11

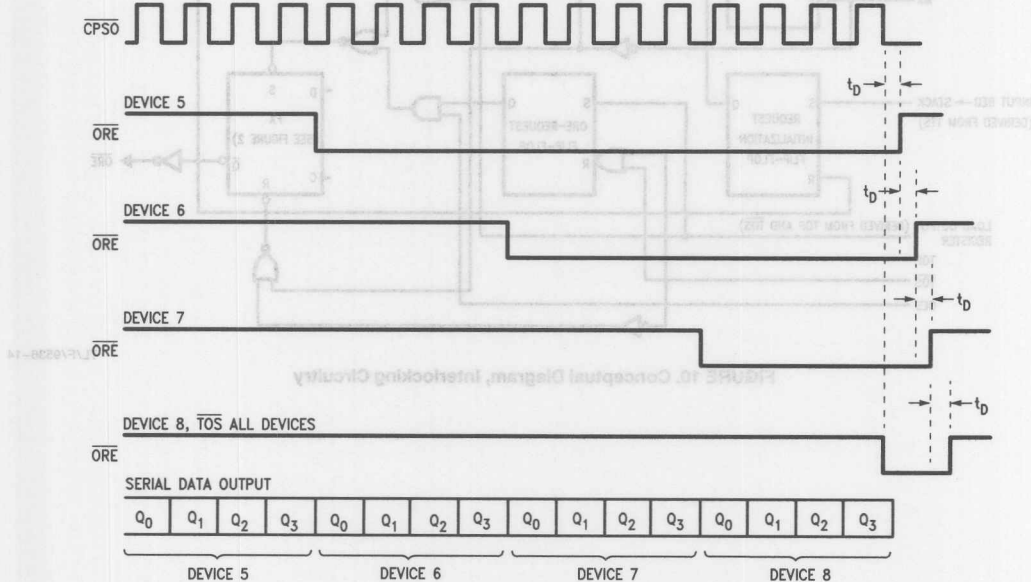


FIGURE 8. Serial Data Extraction for Array of Figure 6

TL/F/9536-12

## Functional Description (Continued)

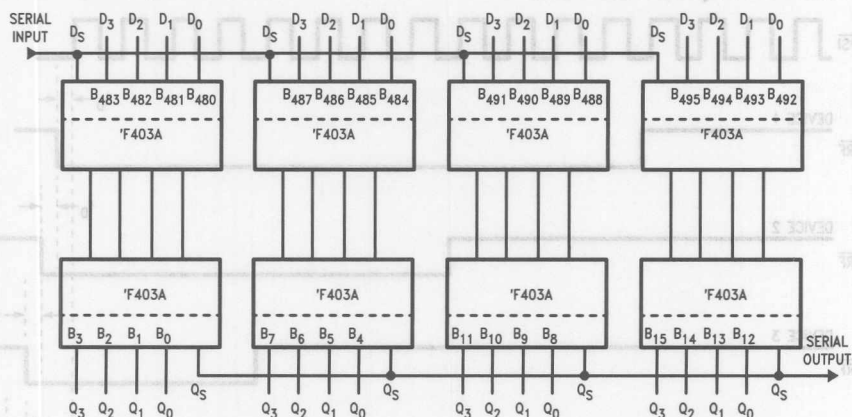


FIGURE 9. Final Position of a 496-Bit Serial Input

TL/F/9536-13

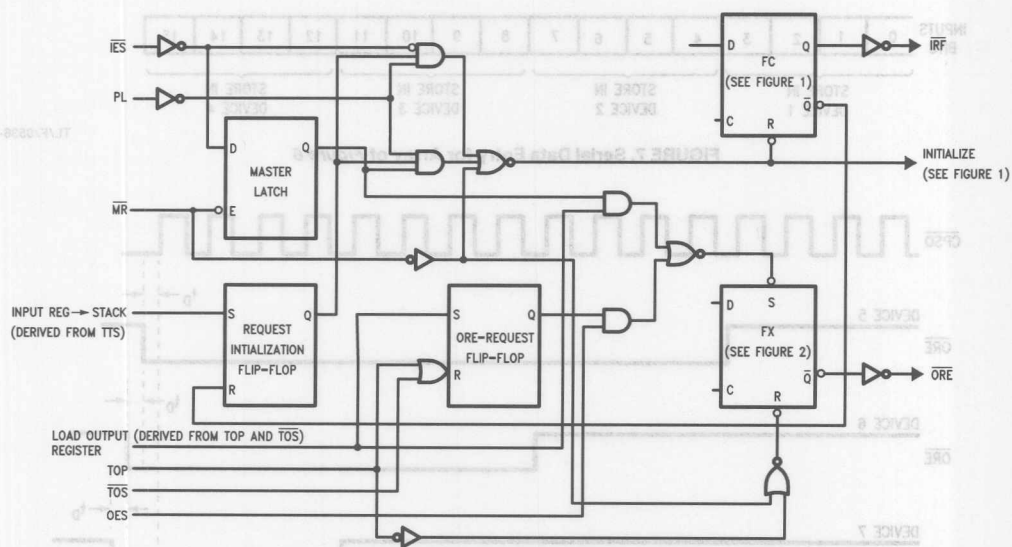


FIGURE 10. Conceptual Diagram, Interlocking Circuitry

TL/F/9536-14

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	–0.5V to V <sub>CC</sub>
Standard Output TRI-STATE Output	–0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

ESD Last Passing Voltage (Min)	4000V
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**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	–55°C to +125°C
Military	0°C to +70°C

Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			–1.5	V	Min	I <sub>IN</sub> = –18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.4		V	Min	I <sub>OH</sub> = –400 μA (IRF, $\overline{\text{ORE}}$ )
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = –2.0 mA (Q <sub>n</sub> , Q <sub>s</sub> )
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = –400 μA (IRF, $\overline{\text{ORE}}$ )
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = –5.7 mA (Q <sub>n</sub> , Q <sub>s</sub> )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = –400 μA (IRF, $\overline{\text{ORE}}$ )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = –5.7 mA (Q <sub>n</sub> , Q <sub>s</sub> )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.4	V	Min	I <sub>OL</sub> = 4 mA (IRF, $\overline{\text{ORE}}$ )
		54F 10% V <sub>CC</sub>		0.4			I <sub>OL</sub> = 8 mA (Q <sub>n</sub> , Q <sub>s</sub> )
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 8 mA (IRF, $\overline{\text{ORE}}$ )
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 16 mA (Q <sub>n</sub> , Q <sub>s</sub> )
I <sub>IH</sub>	Input HIGH Current			20	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			100	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current			–0.4	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			–50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	–20		–130	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CEX</sub>	Output HIGH Leakage Current			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>CCL</sub>	Power Supply Current			170	mA	Max	V <sub>O</sub> = LOW

## AC Electrical Characteristics

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$		$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{pF}$			
		Min	Max	Min	Max	Min	Max		
t <sub>PHL</sub>	Propagation Delay, Negative-Going CPSI to IRF Output	7.5	14.0			7.0	15.0	ns	403-a, b
t <sub>PLH</sub>	Propagation Delay, Negative-Going TTS to IRF	11.0	20.5			10.0	22.5		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Negative-Going CPSO to Q <sub>S</sub> Output	8.5 8.0	17.0 14.5			7.5 7.0	18.5 15.5	ns	403-c, d
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Positive-Going TOP to Outputs Q <sub>0</sub> –Q <sub>3</sub>	10.0 8.5	18.0 15.5			9.0 8.0	20.0 16.5	ns	403-e
t <sub>PHL</sub>	Propagation Delay, Negative-Going CPSO to ORE	9.5	17.5			9.0	19.0	ns	403-c, d
t <sub>PHL</sub>	Propagation Delay, Negative-Going TOP to ORE	8.0	15.0			7.5	16.5		
t <sub>PLH</sub>	Propagation Delay, Positive-Going TOP to ORE	12.5	22.0			11.5	25.0	ns	403-e
t <sub>PLH</sub>	Propagation Delay, Negative-Going TOS to Positive Going ORE	12.5	22.0			11.0	25.0	ns	403-c, d
t <sub>PHL</sub>	Propagation Delay, Positive-Going PL to Negative-Going IRF	7.0	13.0			6.5	14.0		
t <sub>PLH</sub>	Propagation Delay, Negative-Going PL to Positive-Going IRF	9.5	17.0			8.5	19.5	ns	403-g, h

## AC Electrical Characteristics (Continued)

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay, Positive-Going $\overline{OES}$ to $\overline{ORE}$	10.0	18.0			9.0	20.5	ns	
$t_{PLH}$	Propagation Delay, Positive-Going $\overline{IES}$ to Positive-Going $\overline{IRF}$	8.5	15.5			7.5	17.5	ns	403-h
$t_{PLH}$	Propagation Delay, $\overline{MR}$ to $\overline{IRF}$	8.0	15.0			7.5	17.0	ns	
$t_{PHL}$	Propagation Delay, $\overline{MR}$ to $\overline{ORE}$	9.0	16.0			8.0	17.5	ns	
$t_{PZH}$	Propagation Delay, $\overline{OE}$ to $Q_0, Q_1, Q_2, Q_3$	2.5	6.5			2.0	8.0	ns	
$t_{PZL}$		2.5	7.5			2.0	8.5		
$t_{PHZ}$	Propagation Delay, $\overline{OE}$ to $Q_0, Q_1, Q_2, Q_3$	2.5	6.5			2.0	8.0		
$t_{PLZ}$		2.5	7.5			2.0	8.0		
$t_{PZH}$	Propagation Delay, Negative-Going $\overline{OES}$ to $Q_S$	5.5	12.0			5.0	15.0	ns	
$t_{PZL}$		5.5	14.0			5.0	15.0		
$t_{PHZ}$	Propagation Delay, Negative-Going $\overline{OES}$ to $Q_S$	5.5	12.0			5.0	14.0	ns	
$t_{PLZ}$		5.5	14.5			5.0	16.0		
$t_{PZH}$	Turn On Time $\overline{TOS}$ to $Q_S$	8.5	21.0			8.0	24.0	ns	
$t_{PZL}$		8.5	20.0			8.0	21.0		
$t_{DFT}$	Fall Through Time	45.0	80.0			35.0	95.0	ns	403-f
$t_{AP}$	Parallel Appearance Time, $\overline{ORE}$ to $Q_0-Q_3$	-10.0	-1.0			-10.0	-1.0	ns	
$t_{AS}$	Serial Appearance Time, $\overline{ORE}$ to $Q_S$	-10.0	2.0			-10.0	2.0		



## AC Operating Requirements

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Set-up Time HIGH or LOW	1.0				1.0		ns	403-a, b
$t_s(\text{L})$	$D_S$ to Negative $\overline{\text{CPSI}}$	1.0				1.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	3.5				3.5		ns	403-a, b, g, h
$t_h(\text{L})$	$D_S$ to $\overline{\text{CPSI}}$	3.5				3.5			
$t_s(\text{L})$	Set-up Time, LOW $\overline{\text{TTS}}$ to $\overline{\text{IRF}}$ Serial or Parallel Mode	0				0		ns	403-a, b, g, h
$t_s(\text{L})$	Set-up Time, LOW Negative-Going $\overline{\text{ORE}}$ to Negative-Going $\overline{\text{TOS}}$	0				0		ns	403-c, d
$t_s(\text{L})$	Set-up Time, LOW Negative-Going $\overline{\text{IES}}$ to $\overline{\text{CPSI}}$	3.0				4.0		ns	403-b
$t_s(\text{L})$	Set-up Time, LOW Negative-Going $\overline{\text{TTS}}$ to $\overline{\text{CPSI}}$	14.0				15.5		ns	403-b
$t_s(\text{H})$	Set-up Time, HIGH or LOW	0				0		ns	
$t_s(\text{L})$	Parallel Inputs to PL	0				0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0				2.5		ns	
$t_h(\text{L})$	Parallel Inputs to PL	2.0				2.5			
$t_w(\text{H})$	$\overline{\text{CPSI}}$ Pulse Width	5.0				6.0		ns	403-a, b
$t_w(\text{L})$	HIGH or LOW	3.0				5.0			
$t_w(\text{H})$	PL Pulse Width, HIGH	4.0				5.0		ns	403-g, h
$t_w(\text{L})$	$\overline{\text{TTS}}$ Pulse Width, LOW Serial or Parallel Mode	3.5				4.0		ns	403-a, b, c, d
$t_w(\text{L})$	$\overline{\text{MR}}$ Pulse Width, LOW	3.5				4.0		ns	403-f
$t_w(\text{H})$	TOP Pulse Width	4.5				5.5		ns	403-e
$t_w(\text{L})$	HIGH or LOW	3.5				4.0			
$t_w(\text{H})$	$\overline{\text{CPSO}}$ Pulse Width	4.5				5.5		ns	403-c, d
$t_w(\text{L})$	HIGH or LOW	3.0				4.0			
$t_{\text{rec}}$	Recovery Time $\overline{\text{MR}}$ to Any Input	5.0				5.5		ns	403-f

## Timing Waveforms

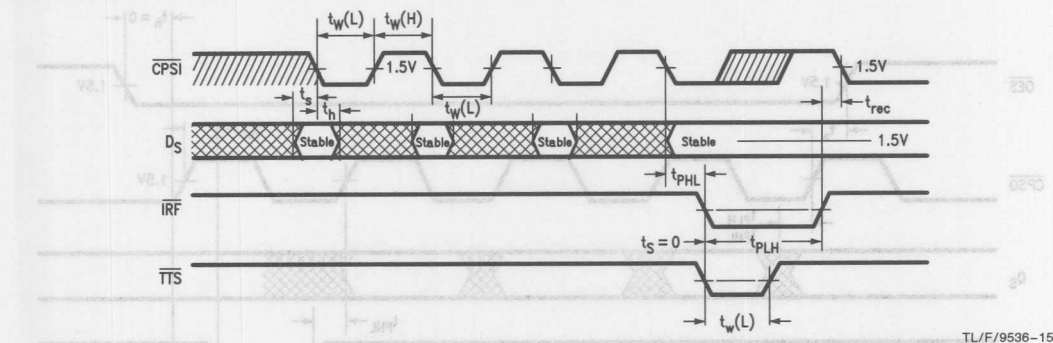


FIGURE 403-a. Serial Input, Unexpanded or Master Operation

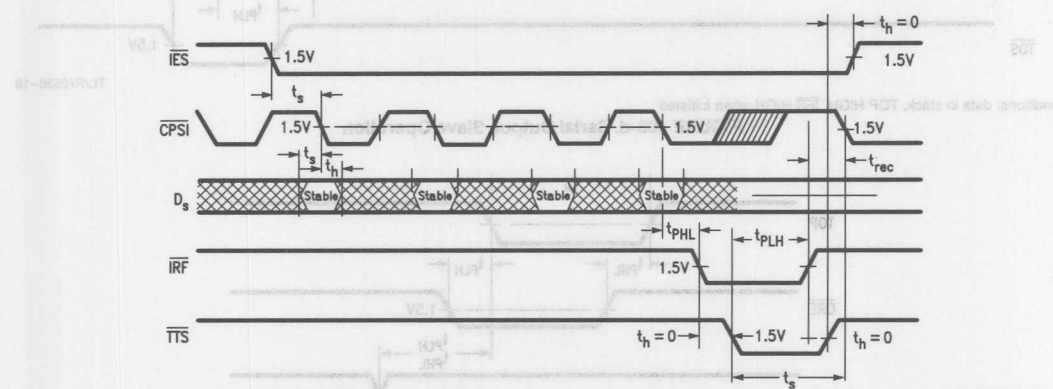


FIGURE 403-b. Serial Input, Expanded Slave Operation

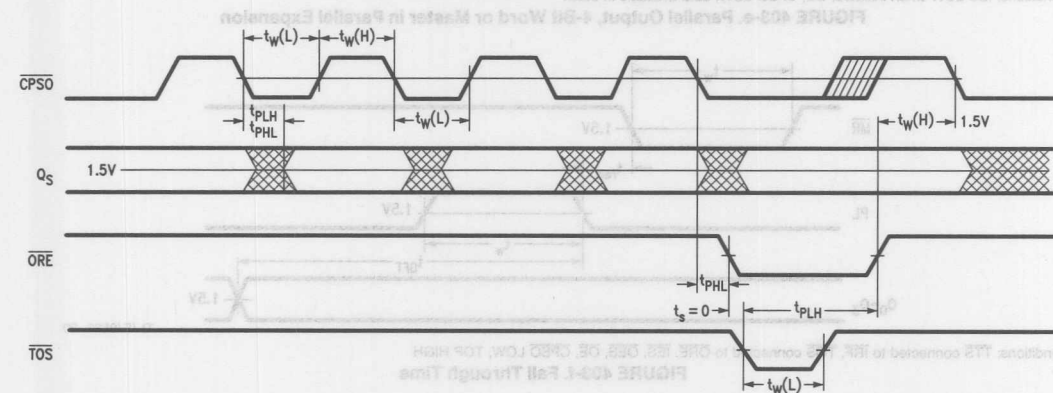
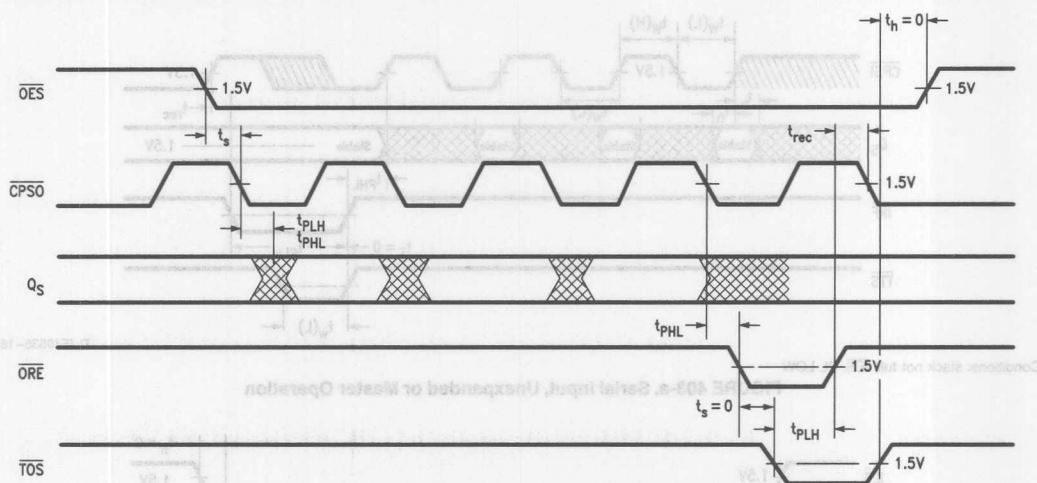


FIGURE 403-c. Serial Output, Unexpanded or Master Operation

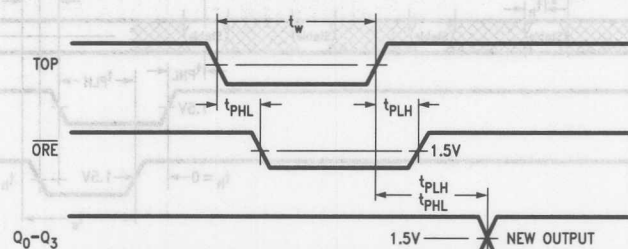
## Timing Waveforms (Continued)



Conditions: data in stack, TOP HIGH,  $\overline{IES}$  HIGH when initiated

FIGURE 403-d. Serial Output, Slave Operation

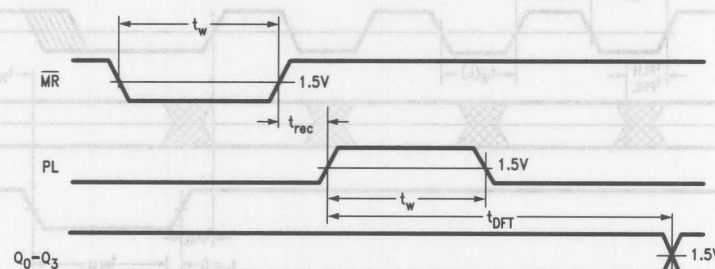
TL/F/9536-18



Conditions:  $\overline{IES}$  LOW when initiated,  $\overline{OE}$ ,  $\overline{CPSO}$  LOW; data available in stack

FIGURE 403-e. Parallel Output, 4-Bit Word or Master in Parallel Expansion

TL/F/9536-19

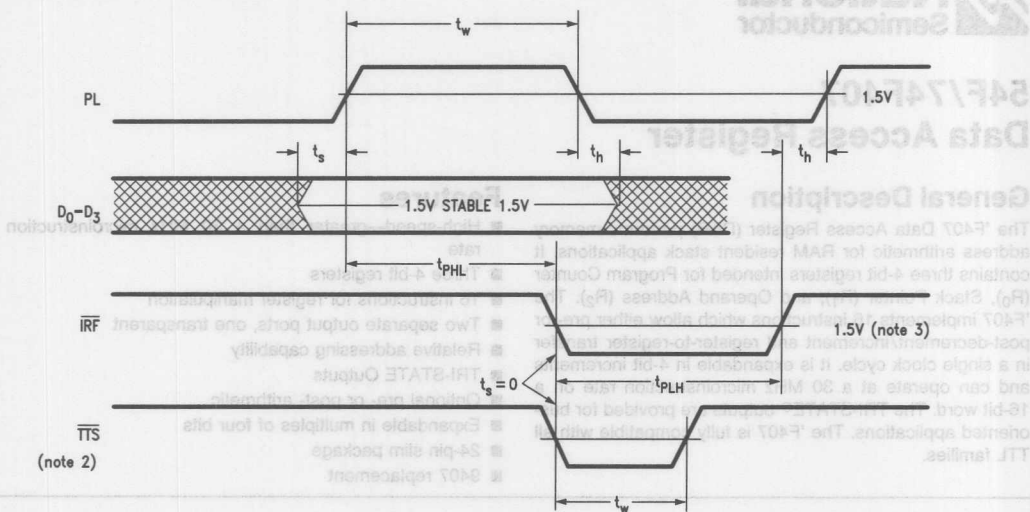


Conditions:  $\overline{TTS}$  connected to  $\overline{IRF}$ ,  $\overline{TOS}$  connected to  $\overline{ORE}$ ,  $\overline{IES}$ ,  $\overline{OES}$ ,  $\overline{OE}$ ,  $\overline{CPSO}$  LOW, TOP HIGH

FIGURE 403-f. Fall Through Time

TL/F/9536-20

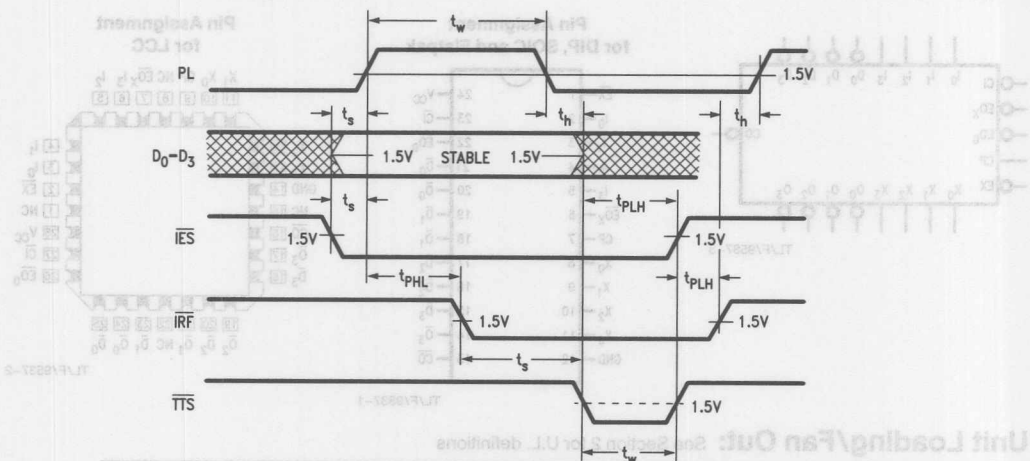
## Timing Waveforms (Continued)



TL/F/9536-21

Conditions: stack not full,  $\overline{IES}$  LOW when initialized

**FIGURE 403-g. Parallel Load Mode, 4-Bit Word (Unexpanded) or Master in Parallel Expansion**



TL/F/9536-22

Conditions: stack not full, device initialized (Note 1) with  $\overline{IES}$  HIGH

**FIGURE 403-h. Parallel Load, Slave Mode**

**Note 1:** Initialization requires a master reset to occur after power has been applied.

**Note 2:** TTS normally connected to  $\overline{IRF}$ .

**Note 3:** If stack is full,  $\overline{IRF}$  will stay LOW.

Pin Name	Description
D0-D3	Data Inputs (Active LOW)
IO-2	Instruction Word Inputs
C1	Carry Input (Active LOW)
C2	Carry Output (Active LOW)
CP	Clock Input (L-H Edge-Triggered)
EX	Execute Input (Active LOW)
EOx	Address Output Enable Input (Active LOW)
EO0	Data Output Enable Input (Active LOW)
X0-X6	Address Outputs
D0-D3	Data Outputs (Active LOW)

# 54F/74F407

## Data Access Register

### General Description

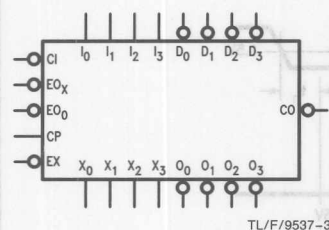
The 'F407 Data Access Register (DAR) performs memory address arithmetic for RAM resident stack applications. It contains three 4-bit registers intended for Program Counter (R<sub>0</sub>), Stack Pointer (R<sub>1</sub>), and Operand Address (R<sub>2</sub>). The 'F407 implements 16 instructions which allow either pre- or post-decrement/increment and register-to-register transfer in a single clock cycle. It is expandable in 4-bit increments and can operate at a 30 MHz microinstruction rate on a 16-bit word. The TRI-STATE® outputs are provided for bus-oriented applications. The 'F407 is fully compatible with all TTL families.

### Features

- High-speed—greater than a 30 MHz microinstruction rate
- Three 4-bit registers
- 16 instructions for register manipulation
- Two separate output ports, one transparent
- Relative addressing capability
- TRI-STATE Outputs
- Optional pre- or post- arithmetic
- Expandable in multiples of four bits
- 24-pin slim package
- 9407 replacement

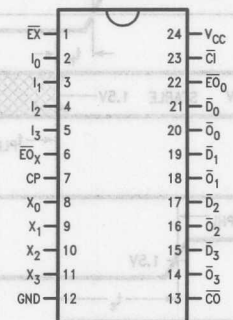
**Ordering Code:** See Section 5

### Logic Symbol

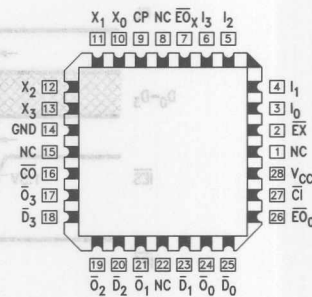


### Connection Diagrams

Pin Assignment  
for DIP, SOIC and Flatpak



Pin Assignment  
for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I <sub>IH</sub> /I <sub>IL</sub> Output I <sub>OH</sub> /I <sub>OL</sub>
$\bar{D}_0$ – $\bar{D}_3$	Data Inputs (Active LOW)	1.0/0.67	20 $\mu$ A/ –0.4 mA
I <sub>0</sub> –I <sub>3</sub>	Instruction Word Inputs	1.0/0.67	20 $\mu$ A/ –0.4 mA
$\bar{C}I$	Carry Input (Active LOW)	1.0/0.67	20 $\mu$ A/ –0.4 mA
$\bar{C}O$	Carry Output (Active LOW)	20/13.3 (0.67)	0.4 mA/8 mA (4 mA)
CP	Clock Input (L-H Edge-Triggered)	1.0/0.67	20 $\mu$ A/ –0.4 mA
EX	Execute Input (Active LOW)	1.0/0.67	20 $\mu$ A/ –0.4 mA
EO <sub>X</sub>	Address Output Enable Input (Active LOW)	1.0/0.67	20 $\mu$ A/ –0.4 mA
EO <sub>0</sub>	Data Output Enable Input (Active LOW)	1.0/0.67	20 $\mu$ A/ –0.4 mA
X <sub>0</sub> –X <sub>3</sub>	Address Outputs	284 (100)/26.7 (13.3)	–5.7 mA (2 mA)/16 mA (8 mA)
$\bar{O}_0$ – $\bar{O}_3$	Data Outputs (Active LOW)	284 (100)/26.7 (13.3)	–5.7 mA (2 mA)/16 mA (8 mA)

The output of the register contents on the data bus (refer to the Block Diagram). The DAR performs sixteen instructions, selected by  $I_0-I_3$ , as listed in the Function Table.

The 'F407 operates on a single clock. CP and  $\overline{EX}$  are inputs to a 2-input, active LOW AND gate. For normal operation  $\overline{EX}$  is brought LOW while CP is HIGH. A microcycle starts as the clock goes HIGH. Data inputs  $\overline{D}_0-\overline{D}_3$  are applied to the Adder as one of the operands. Three of the four instruction lines ( $I_1-I_2-I_3$ ) select which of the three registers, if any, is to be used as the other operand. The LOW-to-HIGH CP transition writes the result from the Adder into a register ( $R_0-R_2$ ) and into the output register provided  $\overline{EX}$  is LOW. If

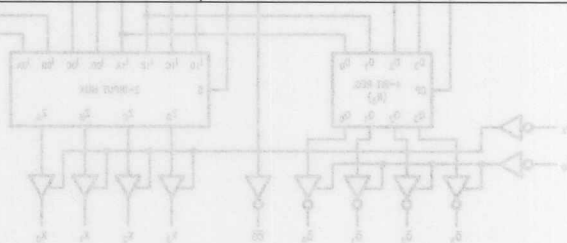
'F407 is organized as a 4-bit register slice. The active LOW  $\overline{CI}$  and  $\overline{CO}$  lines allow ripple-carry expansion over longer word lengths.

In a typical application, the register utilization in the DAR may be as follows:  $R_0$  is the Program Counter (PC),  $R_1$  is the Stack Pointer (SP) for memory resident stacks and  $R_2$  contains the operand address. For an instruction Fetch, PC can be gated on the X-Bus while it is being incremented (i.e., D-Bus = 1). If the fetched instruction calls for an effective address for execution, which is displaced from the PC, the displacement can be added to the PC and loaded into  $R_2$  during the next microcycle.

Function Table

Instruction				Combinatorial Function Available on the X-Bus	Sequential Function Occurring on the Next Rising CP Edge
$I_3$	$I_2$	$I_1$	$I_0$		
L	L	L	L	$R_0$	$R_0$ Plus D Plus CI $\rightarrow R_0$ and 0-Register
L	L	L	H	$R_0$ Plus D Plus CI	$R_0$ Plus D Plus CI $\rightarrow R_1$ and 0-Register
L	L	H	L	$R_0$	$R_0$ Plus D Plus CI $\rightarrow R_2$ and 0-Register
L	L	H	H	$R_0$ Plus D Plus CI	$R_0$ Plus D Plus CI $\rightarrow R_2$ and 0-Register
L	H	L	L	$R_0$	$R_0$ Plus D Plus CI $\rightarrow R_1$ and 0-Register
L	H	L	H	$R_0$ Plus D Plus CI	$R_0$ Plus D Plus CI $\rightarrow R_1$ and 0-Register
L	H	H	L	$R_1$	$R_1$ Plus D Plus CI $\rightarrow R_1$ and 0-Register
L	H	H	H	$R_1$ Plus D Plus CI	$R_1$ Plus D Plus CI $\rightarrow R_1$ and 0-Register
H	L	L	L	$R_2$	D Plus CI $\rightarrow R_2$ and 0-Register
H	L	L	H	D Plus CI	D Plus CI $\rightarrow R_0$ and 0-Register
H	L	H	L	$R_0$	D Plus CI $\rightarrow R_0$ and 0-Register
H	L	H	H	D Plus CI	D Plus CI $\rightarrow R_0$ and 0-Register
H	H	L	L	$R_2$	$R_2$ Plus D Plus CI $\rightarrow R_2$ and 0-Register
H	H	L	H	$R_2$ Plus D Plus CI	$R_2$ Plus D Plus CI $\rightarrow R_2$ and 0-Register
H	H	H	L	$R_1$	D Plus CI $\rightarrow R_1$ and 0-Register
H	H	H	H	D Plus CI	D Plus CI $\rightarrow R_1$ and 0-Register

H = HIGH Voltage Level  
L = LOW Voltage Level

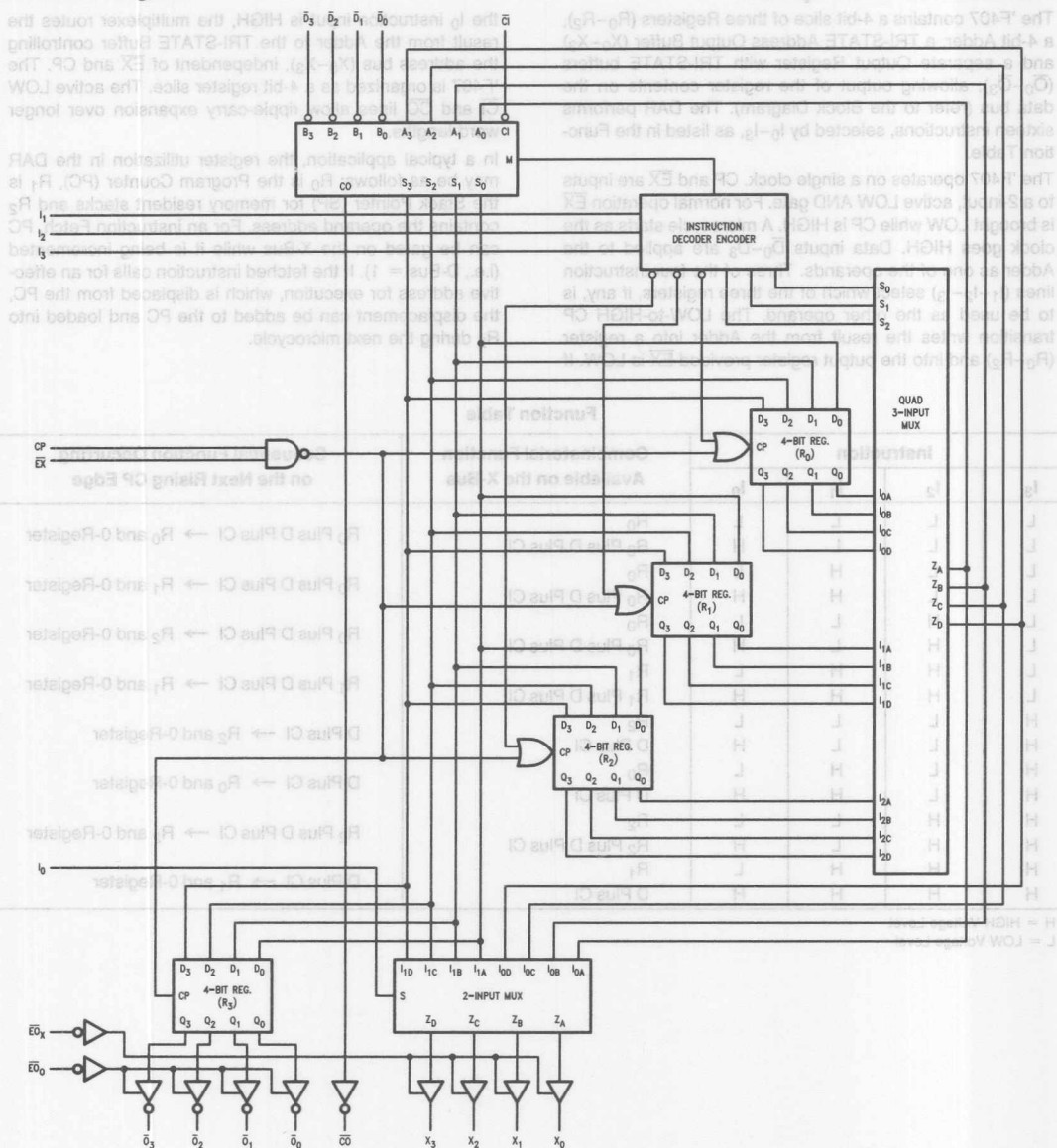


2-70581/1, J7

any other information or data should be obtained from the manufacturer or distributor of the device.



## Block Diagram



TL/F/9537-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Timing Diagrams

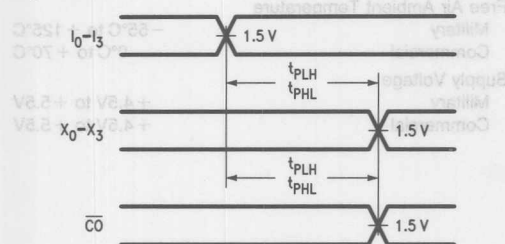
 $\overline{EO}_x = \text{LOW}$ 

FIGURE 407-a

TL/F/9537-7

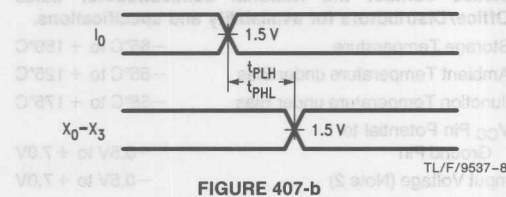
 $\overline{EO}_x = \text{LOW}$ 

FIGURE 407-b

TL/F/9537-8

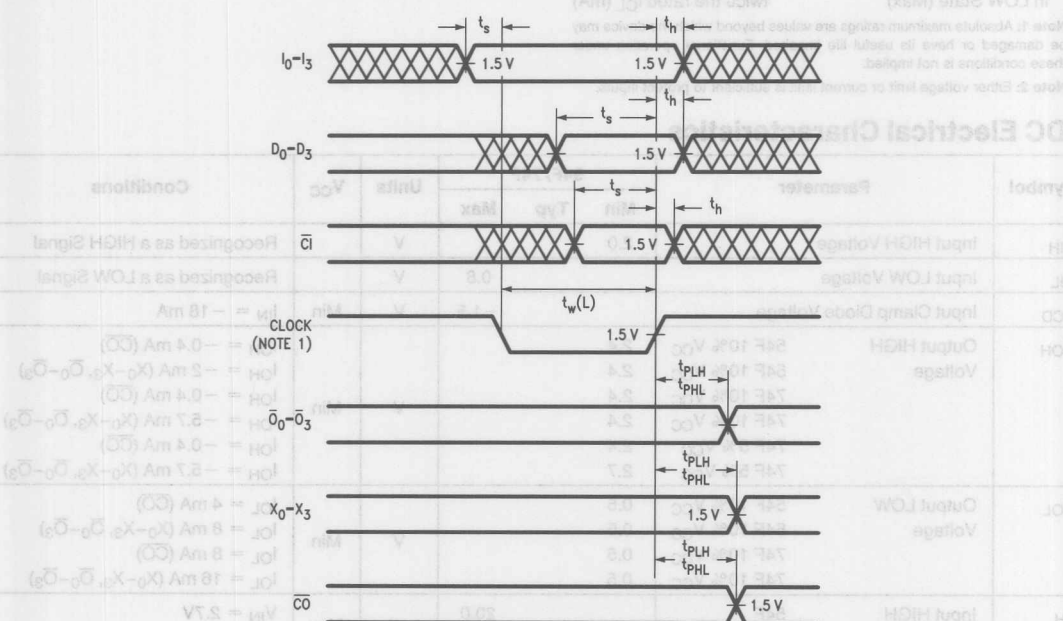
 $\overline{EO}_0 = \text{LOW}$ 

FIGURE 407-c

TL/F/9537-9

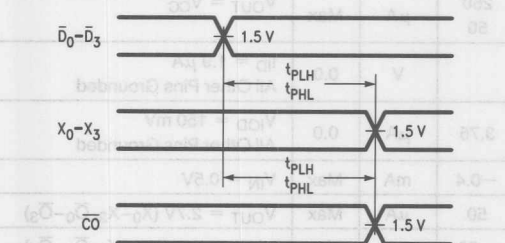
 $\overline{EO}_x = \text{LOW}, i_0 = \text{HIGH}$ 

FIGURE 407-d

TL/F/9537-5

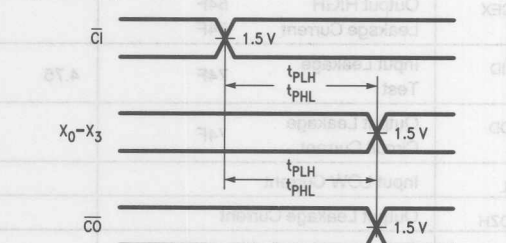
 $\overline{EO}_x = \text{LOW}, i_0 = \text{HIGH}$ 

FIGURE 407-e

TL/F/9537-6

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.5	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.4		V	Min	I <sub>OH</sub> = −0.4 mA ( $\overline{CO}$ )
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −2 mA (X <sub>0</sub> –X <sub>3</sub> , $\overline{O_0}$ – $\overline{O_3}$ )
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −0.4 mA ( $\overline{CO}$ )
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −5.7 mA (X <sub>0</sub> –X <sub>3</sub> , $\overline{O_0}$ – $\overline{O_3}$ )
		74F 5% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −0.4 mA ( $\overline{CO}$ )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −5.7 mA (X <sub>0</sub> –X <sub>3</sub> , $\overline{O_0}$ – $\overline{O_3}$ )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>	0.5		V	Min	I <sub>OL</sub> = 4 mA ( $\overline{CO}$ )
		54F 10% V <sub>CC</sub>	0.5				I <sub>OL</sub> = 8 mA (X <sub>0</sub> –X <sub>3</sub> , $\overline{O_0}$ – $\overline{O_3}$ )
		74F 10% V <sub>CC</sub>	0.5				I <sub>OL</sub> = 8 mA ( $\overline{CO}$ )
		74F 10% V <sub>CC</sub>	0.5				I <sub>OL</sub> = 16 mA (X <sub>0</sub> –X <sub>3</sub> , $\overline{O_0}$ – $\overline{O_3}$ )
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.4	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V (X <sub>0</sub> –X <sub>3</sub> , $\overline{O_0}$ – $\overline{O_3}$ )
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V (X <sub>0</sub> –X <sub>3</sub> , $\overline{O_0}$ – $\overline{O_3}$ )
I <sub>OS</sub>	Output Short-Circuit Current		−30	−100	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		90	145	mA	Max	

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## AC Electrical Characteristics

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	8.0	12.0	21.0	7.0	24.0	7.0	25.0	ns	407-c
$t_{PHL}$	CP to $\overline{O}_n$ (Note 1)	5.0	7.5	13.0	4.0	15.0	4.0	15.0		
$t_{PLH}$	Propagation Delay, $I_0$ LOW	9.0	13.0	18.0	7.5	21.0	8.0	20.0	ns	407-a
$t_{PHL}$	$I_1$ – $I_3$ to $X_0$ – $X_3$	9.5	14.0	20.5	8.0	25.0	8.5	22.0		
$t_{PLH}$	Propagation Delay, $I_0$ HIGH	16.5	23.5	33.0	8.5	50.0	14.5	36.0	ns	407-a
$t_{PHL}$	$I_1$ – $I_3$ to $X_0$ – $X_3$	11.0	17.0	25.0	6.5	35.0	10.0	27.0		
$t_{PLH}$	Propagation Delay, $I_0$ LOW	9.0	13.5	21.0	7.0	24.0	8.0	22.5	ns	407-b
$t_{PHL}$	CP to $X_n$	11.5	18.0	24.0	8.5	28.0	10.5	26.0		
$t_{PLH}$	Propagation Delay, $I_0$ HIGH	18.0	26.5	35.0	16.0	43.0	16.0	37.0	ns	407-b
$t_{PHL}$	CP to $X_n$	12.5	20.0	28.5	11.5	36.5	11.5	31.0		
$t_{PLH}$	Propagation Delay	10.5	15.0	23.0	6.5	29.0	9.5	25.0	ns	407-d
$t_{PHL}$	$\overline{D}_n$ to $X_n$	6.0	9.0	14.0	3.0	20.5	5.0	15.5		
$t_{PLH}$	Propagation Delay	7.0	10.5	16.0	4.0	22.0	6.0	17.5	ns	407-e
$t_{PHL}$	CI to $X_n$	5.5	9.0	12.0	4.5	14.0	4.5	13.5		
$t_{PLH}$	Propagation Delay	4.5	9.0	11.5	4.0	14.5	4.0	13.0	ns	407-b
$t_{PHL}$	$I_0$ to $X_n$	4.5	10.0	14.0	3.0	19.5	4.0	15.5		
$t_{PLH}$	Propagation Delay	11.0	19.0	24.0	9.0	33.0	11.0	26.0	ns	407-a
$t_{PHL}$	CP to $\overline{CO}$	11.5	18.5	27.0	6.5	38.0	11.5	29.0		
$t_{PLH}$	Propagation Delay	3.5	5.5	8.5	3.0	11.0	3.0	9.5	ns	407-e
$t_{PHL}$	$\overline{CI}$ to $\overline{CO}$	4.5	7.0	12.0	3.0	10.0	4.0	13.0		
$t_{PLH}$	Propagation Delay	3.5	5.5	9.0	3.0	10.0	3.0	9.5	ns	407-d
$t_{PHL}$	$\overline{D}_n$ to $\overline{CO}$	4.0	6.5	11.0	3.5	10.0	3.5	12.0		
$t_{PLH}$	Propagation Delay	10.0	15.0	22.0	8.0	23.0	9.0	23.5	ns	407-a
$t_{PHL}$	$I_1$ – $I_3$ to $\overline{CO}$	11.0	16.0	23.0	6.0	32.5	10.0	25.0		
$t_{PZH}$	Enable Time	7.0	10.0	14.5	4.5	26.0	5.5	17.0	ns	
$t_{PZL}$	$\overline{EO}_0$ to $\overline{O}_n$ or $\overline{EO}_x$ to $X_n$	6.0	9.0	15.0	3.5	16.0	5.5	16.5		
$t_{PHZ}$	Disable Time	1.5	4.0	7.0	2.0	9.0	1.5	8.0	ns	
$t_{PLZ}$	$\overline{EO}_0$ to $\overline{O}_n$ or $\overline{EO}_x$ to $X_n$	5.0	10.0	14.0	5.0	18.0	4.0	15.5		

**Note 1:** The internal clock is generated from CP and EX. The internal Clock is HIGH if EX or CP is HIGH, LOW if EX and CP are LOW.

		$C_L = 50 \text{ pF}$				$C_L = 50 \text{ pF}$			$C_L = 50 \text{ pF}$			Units	No.
		Min	Typ	Max	Min	Max	Min	Max	Min	Max			
$t_{cw}$	Clock Period	32.0	26.0		36.0			36.0			ns		
$t_s(H)$	Setup Time, HIGH or LOW	4.0			4.5			4.5					
$t_s(L)$	$I_1-I_3$ to Negative-Going CP	4.0			4.5			4.5			ns	407-c	
$t_h(H)$	Hold Time, HIGH or LOW	0			0			0					
$t_h(L)$	$I_1-I_3$ to Positive-Going CP	0			0			0					
$t_s(H)$	Setup Time, HIGH or LOW	16.5			18.5			18.5					
$t_s(L)$	$\bar{D}_n$ or $\bar{C}_1$ to Negative-Going CP	16.5			18.5			18.5					
$t_h(H)$	Hold Time, HIGH or LOW	0			0			0			ns	407-c	
$t_h(L)$	$\bar{D}_n$ or $\bar{C}_1$ to Negative-Going Clock	0			0			0					
$t_s(H)$	Setup Time, HIGH or LOW	13.0			14.5			14.5					
$t_s(L)$	$\bar{C}_1$ to Positive-Going CP	13.0			14.5			14.5			ns	407-c	
$t_h(H)$	Hold Time, HIGH or LOW	0			0			0					
$t_h(L)$	$\bar{C}_1$ to Positive-Going CP	0			0			0					
$t_w(H)$	Clock Pulse Width	7.5			8.5			8.5			ns	407-c	
$t_w(L)$	HIGH or LOW	7.5			8.5			8.5					
407-a	ns	33.0	24.0	23.0	36.0			36.0					
407-b	ns	33.0	24.0	23.0	36.0			36.0					
407-c	ns	33.0	24.0	23.0	36.0			36.0					
407-d	ns	33.0	24.0	23.0	36.0			36.0					
407-e	ns	33.0	24.0	23.0	36.0			36.0					
407-f	ns	33.0	24.0	23.0	36.0			36.0					
407-g	ns	33.0	24.0	23.0	36.0			36.0					
407-h	ns	33.0	24.0	23.0	36.0			36.0					
407-i	ns	33.0	24.0	23.0	36.0			36.0					
407-j	ns	33.0	24.0	23.0	36.0			36.0					
407-k	ns	33.0	24.0	23.0	36.0			36.0					
407-l	ns	33.0	24.0	23.0	36.0			36.0					
407-m	ns	33.0	24.0	23.0	36.0			36.0					
407-n	ns	33.0	24.0	23.0	36.0			36.0					
407-o	ns	33.0	24.0	23.0	36.0			36.0					
407-p	ns	33.0	24.0	23.0	36.0			36.0					
407-q	ns	33.0	24.0	23.0	36.0			36.0					
407-r	ns	33.0	24.0	23.0	36.0			36.0					
407-s	ns	33.0	24.0	23.0	36.0			36.0					
407-t	ns	33.0	24.0	23.0	36.0			36.0					
407-u	ns	33.0	24.0	23.0	36.0			36.0					
407-v	ns	33.0	24.0	23.0	36.0			36.0					
407-w	ns	33.0	24.0	23.0	36.0			36.0					
407-x	ns	33.0	24.0	23.0	36.0			36.0					
407-y	ns	33.0	24.0	23.0	36.0			36.0					
407-z	ns	33.0	24.0	23.0	36.0			36.0					



## 54F/74F410 Register Stack—16 x 4 RAM TRI-STATE® Output Register

### General Description

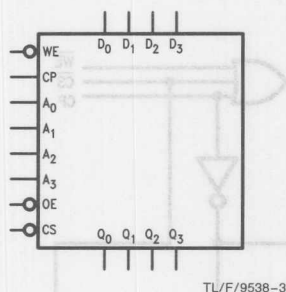
The 'F410 is a register-oriented high-speed 64-bit Read/Write Memory organized as 16-words by 4-bits. An edge-triggered 4-bit output register allows new input data to be written while previous data is held. TRI-STATE outputs are provided for maximum versatility. The 'F410 is fully compatible with all TTL families.

### Features

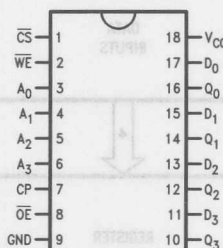
- Edge-triggered output register
- Typical access time of 35 ns
- TRI-STATE outputs
- Optimized for register stack operation
- 18-pin package
- 9410 replacement

**Ordering Code:** See Section 5

### Logic Symbols

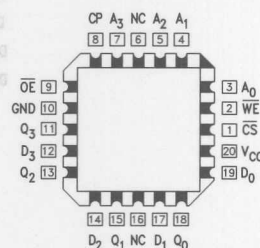


Pin Assignment  
for DIP and Flatpak



### Connection Diagrams

Pin Assignment  
for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
A <sub>0</sub> –A <sub>3</sub>	Address Inputs	1.0/1.0	20 $\mu$ A/ –0.6 mA
D <sub>0</sub> –D <sub>3</sub>	Data Inputs	1.0/1.0	20 $\mu$ A/ –0.6 mA
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/2.0	20 $\mu$ A/ –1.2 mA
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ –0.6 mA
WE	Write Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ –0.6 mA
CP	Clock Input (Outputs Change on LOW-to-HIGH Transition)	1.0/2.0	20 $\mu$ A/ –1.2 mA
Q <sub>0</sub> –Q <sub>3</sub>	TRI-STATE Outputs	150/40 (33.3)	–3 mA/24 mA (20 mA)



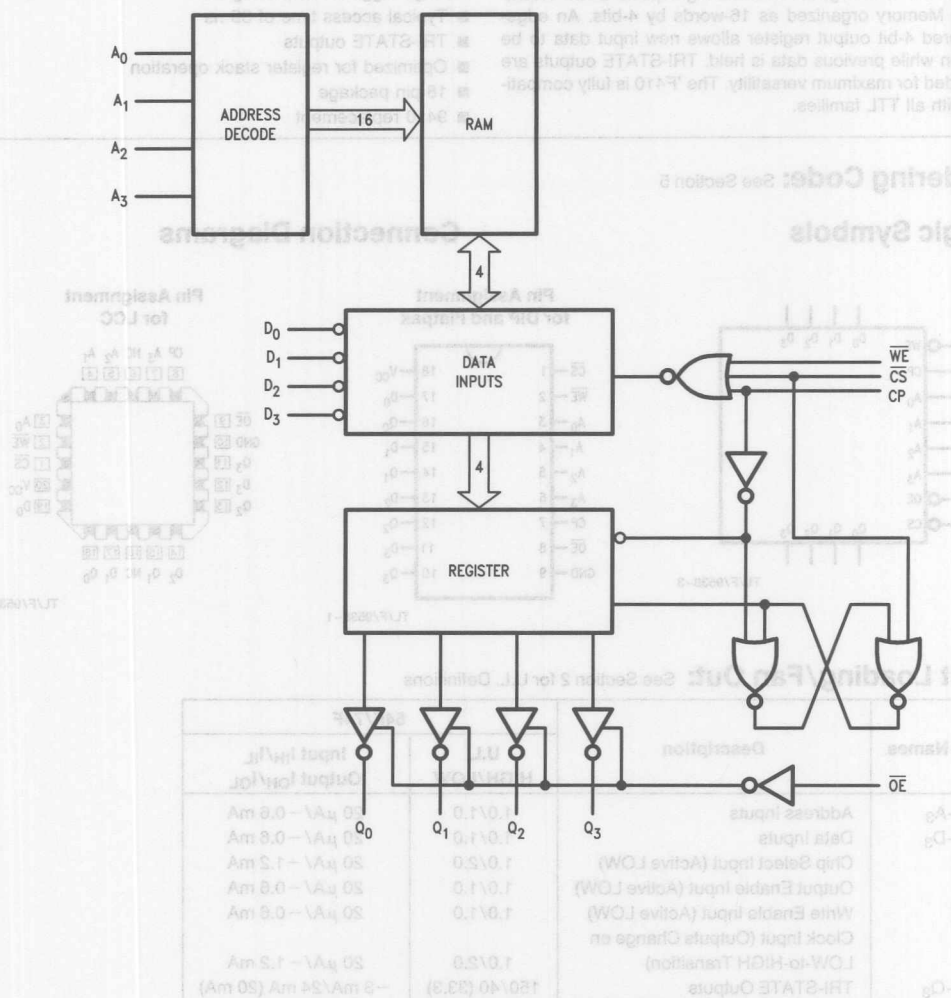
## Functional Description

**Write Operation**—When the three control inputs, Write Enable (WE), Chip Select (CS), and Clock (CP), are LOW the information on the data inputs ( $D_0$ – $D_3$ ) is written into the memory location selected by the address inputs ( $A_0$ – $A_3$ ). If the input data changes while WE, CS, and CP are LOW, the contents of the selected memory location follow these changes, provided setup and hold time criteria are met.

**Read Operation**—Whenever  $\overline{CS}$  is LOW and CP goes from LOW-to-HIGH, the contents of the memory location selected by the address inputs ( $A_0$ – $A_3$ ) are edge-triggered into the Output Register.

The ( $\overline{OE}$ ) input controls the output buffers. When  $\overline{OE}$  is HIGH the four outputs ( $Q_0$ – $Q_3$ ) are in a high impedance or OFF state; when  $\overline{OE}$  is LOW, the outputs are determined by the state of the Output Register.

## Block Diagram



TL/F/9538-4

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	–0.5V to V <sub>CC</sub>
TRI-STATE Output	–0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	–55°C to +125°C
Military	–55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			–1.2	V	Min	I <sub>IN</sub> = –18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = –1 mA
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = –3 mA
		74F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = –1 mA
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = –3 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = –1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>ID</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			–0.6	mA	Max	V <sub>IN</sub> = 0.5V (A <sub>n</sub> , D <sub>n</sub> , $\overline{\text{OE}}$ , WE)
				–1.2			V <sub>IN</sub> = 0.5V ( $\overline{\text{CS}}$ , CP)
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			–50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		–60	–150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V

**DC Electrical Characteristics** (Continued)

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
I <sub>CCH</sub>	Power Supply Current		47	70	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		47	70	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		47	70	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	3.0	8.5	2.5	11.0	2.5	9.5	ns	2-3
t <sub>PHL</sub>	CP to Q	3.5	9.0	3.0	12.0	3.0	10.0		
t <sub>PZH</sub>	Enable Time	3.0	8.0	2.5	10.5	2.5	9.0	ns	2-5
t <sub>PZL</sub>	OE to Q	3.5	9.0	3.0	13.0	3.0	10.0		
t <sub>PHZ</sub>	Disable Time	2.5	6.5	2.0	8.5	2.0	7.5		
t <sub>PLZ</sub>	OE to Q	2.5	7.0	2.0	9.5	2.0	8.0		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> , V <sub>CC</sub> = Mil		T <sub>A</sub> , V <sub>CC</sub> = Com			
		Min	Max	Min	Max	Min	Max		

**READ MODE**

t <sub>s</sub> (H)	Setup Time, HIGH or LOW	15.0		23		17.0		ns	2-6
t <sub>s</sub> (L)	A <sub>n</sub> to CP	15.0		23		17.0			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	0		0		0		ns	2-6
t <sub>h</sub> (L)	A <sub>n</sub> to CP	0		0		0			

**WRITE MODE**

t <sub>s</sub> (H)	Setup Time, HIGH or LOW	0		0		0		ns	2-6
t <sub>s</sub> (L)	A <sub>n</sub> to WE	0		0		0			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	0		0		0		ns	2-6
t <sub>h</sub> (L)	A <sub>n</sub> to WE	0		0		0			
t <sub>s</sub> (H)	Setup Time, HIGH or LOW	5.0		8.5		6.0		ns	2-6
t <sub>s</sub> (L)	D <sub>n</sub> to WE	5.0		8.5		6.0			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	0		2.5		0		ns	2-4
t <sub>h</sub> (L)	D <sub>n</sub> to WE	0		2.5		0			
t <sub>w</sub>	WE Pulse Width Required to Write	7.5		9.5		8.5		ns	2-4
t <sub>w</sub>	CS Pulse Width Required to Write	7.5		9.5		8.5		ns	2-4
t <sub>w</sub>	CP Pulse Width Required to Write	7.5		9.5		8.5		ns	2-4

**Note:** Military temperature range for this device is -40°C to +85°C.

## 54F/74F412

### Multi-Mode Buffered Latch with TRI-STATE® Outputs

#### General Description

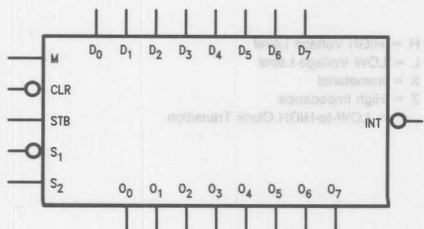
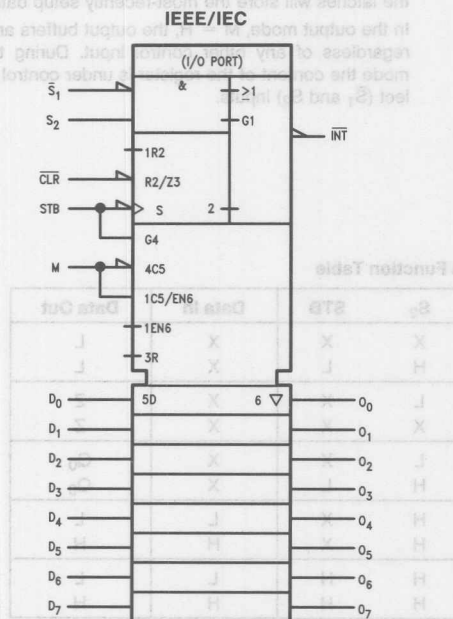
The 'F412 is an 8-bit latch with TRI-STATE output buffers. Also included is a status flip-flop for providing device-busy or request-interrupt commands. Separate Mode and Select inputs allow data to be stored with the outputs enabled or disabled. The device can also operate in a fully transparent mode. The 'F412 is the functional equivalent of the Intel 8212.

#### Features

- TRI-STATE outputs
- Status flip-flop for interrupt commands
- Asynchronous or latched receiver modes
- 300 mil 24-pin slim package

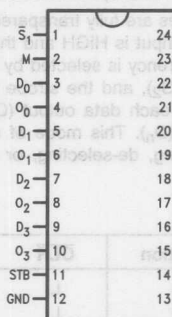
**Ordering Code:** See Section 5

#### Logic Symbols

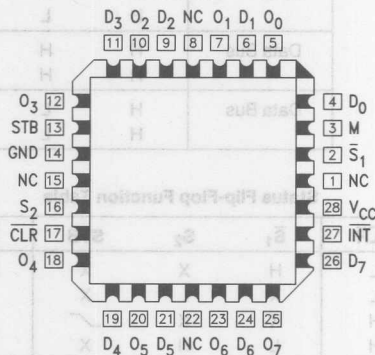


#### Connection Diagrams

##### Pin Assignment for DIP, SOIC and Flatpak



##### Pin Assignment for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$O_0-O_7$	Latch Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)
$D_0-D_7$	Data Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{CLR}$	Clear	1.0/1.0	20 $\mu$ A/-0.6 mA
STB	Strobe	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{INT}$	Interrupt	50/33.3	-1 mA/20 mA
M	Mode Control Input	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{S}_1, S_2$	Select Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA

**Functional Description**

This high-performance eight-bit parallel expandable buffer register incorporates package and mode selection inputs and an edge-triggered status flip-flop designed specifically for implementing bus-organized input/output ports. The TRI-STATE data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides busy or request interrupt commands.

The eight data latches are fully transparent when the internal gate enable, G, input is HIGH and the outputs are enabled. Latch transparency is selected by the mode control (M), select ( $\overline{S}_1$  and  $S_2$ ), and the strobe (STB) inputs and during transparency each data output ( $O_n$ ) follows its respective data input ( $D_n$ ). This mode of operation can be terminated by clearing, de-selecting, or holding the data latches.

An input mode or an output mode is selectable from the M input. In the input mode,  $M = L$ , the eight data latch inputs are enabled when the strobe is HIGH regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken LOW, the latches will store the most-recently setup data.

In the output mode,  $M = H$ , the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the select ( $\overline{S}_1$  and  $S_2$ ) inputs.

**Data Latches Function Table**

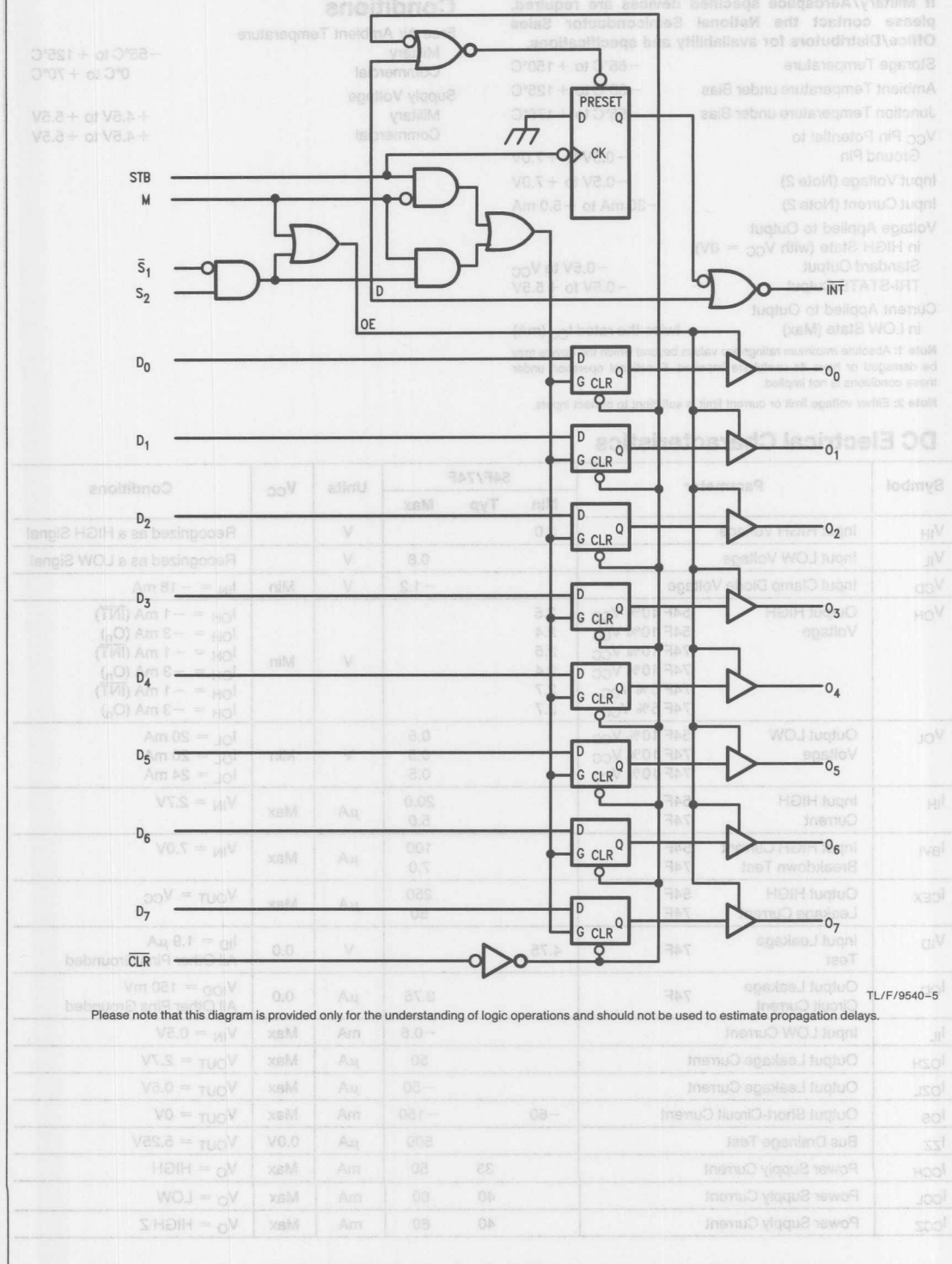
Function	$\overline{CLR}$	M	$\overline{S}_1$	$S_2$	STB	Data In	Data Out
Clear	L	H	H	X	X	X	L
	L	L	L	H	L	X	L
De-Select	X	L	X	L	X	X	Z
	X	L	H	X	X	X	Z
Hold	H	H	H	L	X	X	$Q_0$
	H	L	L	H	L	X	$Q_0$
Data Bus	H	H	L	H	X	L	L
	H	H	L	H	X	H	H
Data Bus	H	L	L	H	H	L	L
	H	L	L	H	H	H	H

**Status Flip-Flop Function Table**

$\overline{CLR}$	$\overline{S}_1$	$S_2$	STB	$\overline{INT}$
L	H	X	X	H
L	X	L	X	H
H	X	X	—	L
H	L	H	X	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 — = LOW-to-HIGH Clock Transition

## Logic Diagram





**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	-0.5V to V <sub>CC</sub>
Standard Output TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	-55°C to +125°C
Military Commercial	0°C to +70°C
Supply Voltage	+4.5V to +5.5V
Military Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	I <sub>OH</sub> = -1 mA (INT) I <sub>OH</sub> = -3 mA (O <sub>n</sub> ) I <sub>OH</sub> = -1 mA (INT) I <sub>OH</sub> = -3 mA (O <sub>n</sub> ) I <sub>OH</sub> = -1 mA (INT) I <sub>OH</sub> = -3 mA (O <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			-50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current		33	50	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		40	60	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		40	60	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	3.5	6.5	8.5	3.0	11.5	3.0	9.5	ns	2-3
$t_{PHL}$	$D_n$ to $O_n$	2.5	5.0	6.5	2.0	8.5	2.0	7.5		
$t_{PLH}$	Propagation Delay	8.5	14.5	18.5	6.5	23.0	7.5	20.5	ns	2-3
$t_{PHL}$	$\bar{S}_1, S_2$ or STB to $O_n$	7.5	12.5	16.0	6.0	19.0	6.5	17.5		
$t_{PLH}$	Propagation Delay	4.5	7.5	9.5	3.5	12.0	4.0	10.5	ns	2-3
$t_{PHL}$	$\bar{S}_1$ or $S_2$ to $\bar{INT}$	4.5	8.0	10.5	3.5	12.5	4.0	11.5		
$t_{PHL}$	Propagation Delay	7.5	12.5	16.0	5.5	18.5	6.5	17.5	ns	2-3
	$\bar{CLR}$ to $O_n$									
$t_{PHL}$	Propagation Delay	6.5	11.0	14.0	5.5	17.5	5.5	15.0	ns	2-3
	STB to $\bar{INT}$									
$t_{pZH}$	Access Time, HIGH or LOW	8.0	12.5	18.0	6.5	20.0	7.0	19.0	ns	2-5
$t_{pZL}$	$\bar{S}_1$ to $O_n$	6.5	11.0	14.0	5.5	18.0	5.5	15.0		
$t_{PHZ}$	Disable Time, HIGH or LOW	4.5	8.0	10.5	4.0	14.5	4.0	11.5	ns	2-5
$t_{PLZ}$	$\bar{S}_1$ to $O_n$	6.5	11.0	14.0	5.5	17.0	5.5	15.0		
$t_{pZH}$	Access Time, HIGH or LOW	7.5	12.5	16.0	6.5	18.5	6.5	17.5	ns	2-5
$t_{pZL}$	$S_2$ to $O_n$	5.0	9.0	11.5	4.0	15.5	4.5	12.5		
$t_{PHZ}$	Disable Time, HIGH or LOW	4.5	7.5	9.5	3.5	12.5	4.0	10.5	ns	2-5
$t_{PLZ}$	$S_2$ to $O_n$	5.5	9.5	12.0	4.5	14.5	4.5	13.0		
$t_{pZH}$	Access Time, HIGH or LOW	5.0	8.5	11.0	4.5	16.0	4.5	12.0	ns	2-5
$t_{pZL}$	M to $O_n$	5.0	8.5	11.0	4.0	15.0	4.5	12.0		
$t_{PHZ}$	Disable Time, HIGH or LOW	4.0	7.0	9.0	3.5	11.5	3.5	10.0	ns	2-5
$t_{PLZ}$	M to $O_n$	5.0	8.5	11.0	4.5	14.0	4.5	12.0		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	0		2.0		1.0		ns	2-6
$t_s(\text{L})$	$D_n$ to $\overline{S}_1, S_2$ or STB	0		2.0		1.0			
$t_h(\text{H})$	Hold Time	8.0		10.0		9.0		ns	2-4
$t_h(\text{L})$	$D_n$ to $\overline{S}_1, S_2$ or STB	8.0		10.0		9.0			
$t_w(\text{H})$	$\overline{S}_1, S_2$ or STB	8.0		11.0		9.0		ns	2-4
$t_w(\text{L})$	Pulse Width, HIGH or LOW	8.0		11.0		9.0			
$t_w(\text{L})$	$\overline{\text{CLR}}$ Pulse Width, LOW	8.0		11.5		9.0		ns	2-4



## 54F/74F413

### 64 x 4 First-In First-Out Buffer Memory with Parallel I/O

#### General Description

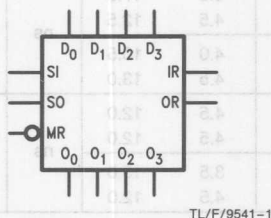
The 'F413 is an expandable fall-through type high-speed First-In First-Out (FIFO) buffer memory organized as 64 words by four bits. The 4-bit input and output registers record and transmit, respectively, asynchronous data in parallel form. Control pins on the input and output allow for handshaking and expansion. The 4-bit wide, 62-bit deep fall-through stack has self-contained control logic.

#### Features

- Separate input and output clocks
- Parallel input and output
- Expandable without external logic
- 15 MHz data rate
- Supply current 160 mA max
- Available in SOIC, (300 mil only)

#### Ordering Code: See Section 5

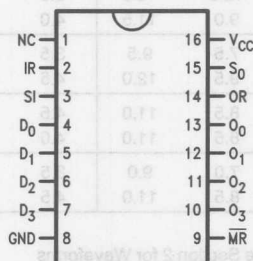
#### Logic Symbol



TL/F/9541-1

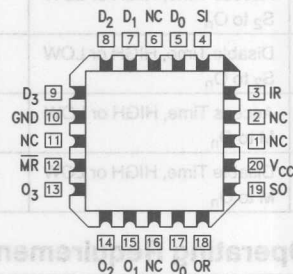
#### Connection Diagrams

Pin Assignment  
for DIP, SOIC and Flatpak



TL/F/9541-2

Pin Assignment  
for LCC



TL/F/9541-3

#### Unit Loading/Fan Out: See Section 2 for U.L. Definitions

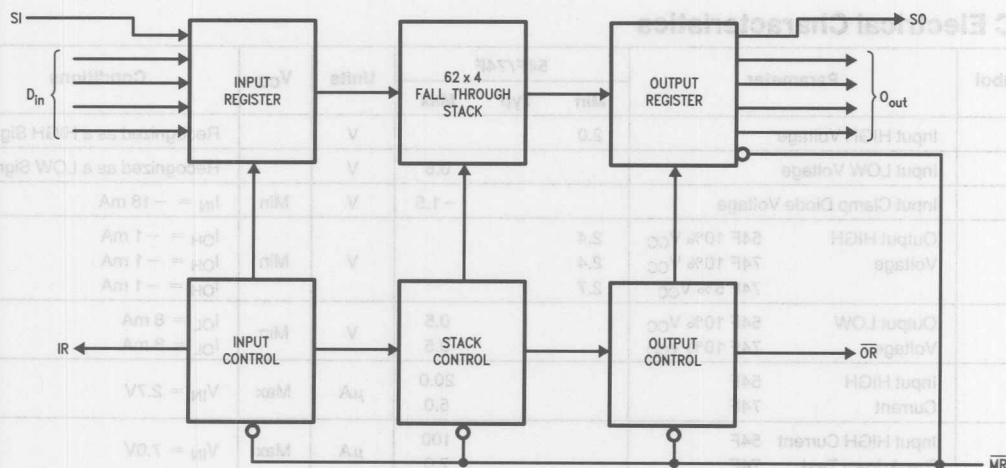
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
D <sub>0</sub> -D <sub>3</sub>	Data Inputs	1.0/0.667	20 $\mu$ A/ -0.4 mA
O <sub>0</sub> -O <sub>3</sub>	Data Outputs	50/13.3	-1 mA/8 mA
IR	Input Ready	1.0/0.667	20 $\mu$ A/ -0.4 mA
SI	Shift In	1.0/0.667	20 $\mu$ A/ -0.4 mA
SO	Shift Out	1.0/0.667	20 $\mu$ A/ -0.4 mA
OR	Output Ready	1.0/0.667	20 $\mu$ A/ -0.4 mA
MR	Master Reset	1.0/0.667	20 $\mu$ A/ -0.4 mA

## Functional Description

**Data Input**—Data is entered into the FIFO on  $D_0$ – $D_3$  inputs. To enter data the Input Ready (IR) should be HIGH, indicating that the first location is ready to accept data. Data then present at the four data inputs is entered into the first location when the Shift In (SI) is brought HIGH. An SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. If the memory is full, IR will remain LOW.

**Data Transfer**—Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will “bubble” to the front. The  $t_{PT}$  parameter defines the time required for the first data to travel from input to the output of a previously empty device.

## Block Diagram



**Data Output**—Data is read from the  $O_0$ – $O_3$  outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW, the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and  $O_0$ – $O_3$  remains as before, i.e., data does not change if FIFO is empty.

**Input Ready and Output Ready** may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least  $t_{PT}$ ) or completely empty (Output Ready stays LOW for at least  $t_{PT}$ ).

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				−1.5	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.4			V	Min	I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.4					I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>			0.5	V	Min	I <sub>OL</sub> = 8 mA
		74F 10% V <sub>CC</sub>			0.5			I <sub>OL</sub> = 8 mA
I <sub>IH</sub>	Input HIGH Current	54F			20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F			5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F			100	μA	Max	V <sub>IN</sub> = 7.0V
		74F			7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F			50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current				−0.4	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−20		−130	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current			115	160	mA	Max	V <sub>O</sub> = HIGH

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Shift In Rate	10			8.0		10		MHz	2-1
$f_{\text{max}}$	Shift Out Rate	10			8.0		10		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	1.5		44.0	1.5	50.0	1.5	48.0	ns	2-3
$t_{\text{PHL}}$	Shift In to IR	1.5		31.0	1.5	37.0	1.5	35.0		
$t_{\text{PLH}}$	Propagation Delay	1.5		52.0	1.5	57.0	1.5	55.0	ns	2-3
$t_{\text{PHL}}$	Shift Out to OR	1.5		31.0	1.5	37.0	1.5	35.0		
$t_{\text{PLH}}$	Propagation Delay	1.5		46.0	1.5	52.0	1.5	50.0	ns	2-3
$t_{\text{PHL}}$	Output Data Delay	1.5		34.0	1.5	39.0	1.5	37.0		
$t_{\text{PLH}}$	Propagation Delay Master Reset to IR	1.5		27.0	1.5	33.0	1.5	31.0	ns	2-3
$t_{\text{PLH}}$	Propagation Delay Master Reset to OR	1.5		30.0	1.5	34.0	1.5	32.0	ns	2-3

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	1.0		1.0		1.0		ns	2-6
$t_s(\text{L})$	$D_n$ to SI	1.0		1.0		1.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	10.0		10.0		10.0		ns	2-4
$t_h(\text{L})$	$D_n$ to SI	10.0		10.0		10.0			
$t_w(\text{H})$	Shift In Pulse Width	5.0		5.0		5.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	10.0		10.0		10.0			
$t_w(\text{H})$	Shift Out Pulse Width	7.5		8.5		7.5		ns	2-4
$t_w(\text{L})$	HIGH or LOW	10.0		10.0		10.0			
$t_w(\text{H})$	Input Ready Pulse Width, HIGH	7.5		8.5		7.5		ns	2-4
$t_w(\text{L})$	Output Ready Pulse Width, LOW	5.0		5.0		5.0		ns	2-4
$t_w(\text{L})$	Master Reset Pulse Width, LOW	10.0		10.0		10.0		ns	2-4
$t_{\text{rec}}$	Recovery Time, MR to SI	32.0		35.0		35.0		ns	2-6
$t_{\text{PT}}$	Data Throughput Time		0.9		1.0		1.0	$\mu\text{s}$	




**54F/74F420**

## Parallel Check Bit/Syndrome Bit Generator

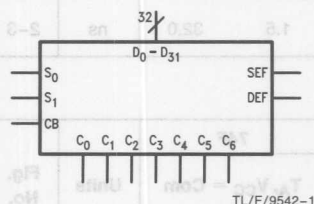
### General Description

The 'F420 is a parallel check bit/syndrome bit generator. The 'F420 utilizes a modified hamming code to generate 7 check bits from a 32-bit dataword, in 15 ns, when operated in the check bit generate mode. When operated in the syndrome generate mode, the check bits and data bits

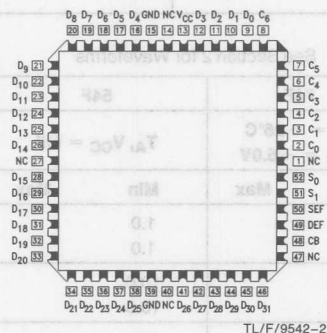
read from memory are utilized in a parity summer to generate syndrome bits upon error detection. The maximum error count detectable is 2. A single error detect can occur in 18 ns; a double error detect in 22 ns. The syndrome bit generation can be output in 15 ns (maximum).

### Ordering Code: See Section 5

### Logic Diagram



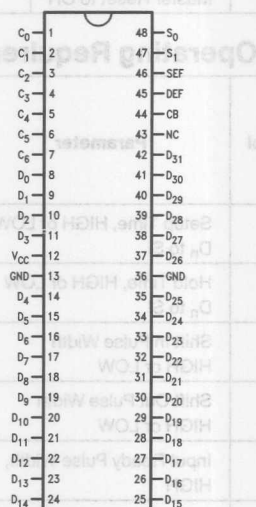
### Pin Assignment for LCC and PCC



TL/F/9542-2

### Connection Diagrams

### Pin Assignment for DIP and Flatpak



TL/F/9542-3

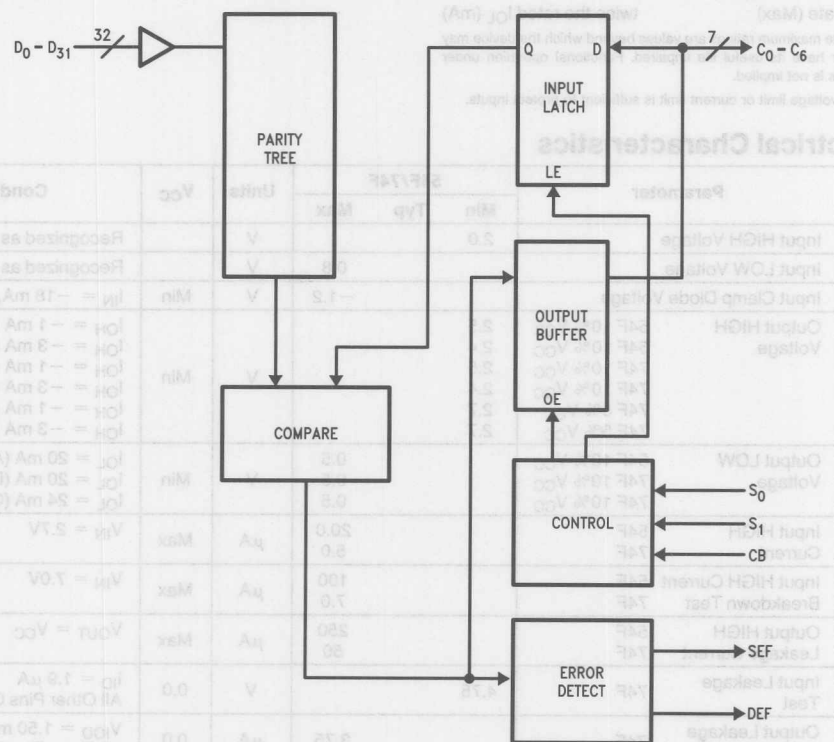
### Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$C_0-C_6$	Check Bit/Syndrome Bus Inputs/ Outputs	3.5/1.083 150/40 (33.3)	70 $\mu$ A / -0.65 mA -3 mA/24 mA (20 mA)
$D_0-D_{31}$	Data Bit Bus	1.0/1.0	20 $\mu$ A / -0.6 mA
CB	Check Bit Control	1.0/1.0	20 $\mu$ A / -0.6 mA
DEF	Double Error Flag	50/33.3	-1 mA/20 mA
SEF	Single Error Flag	50/33.3	-1 mA/20 mA
$S_0, S_1$	Mode Control	1.0/1.0	20 $\mu$ A / -0.6 mA

Function Table

Memory Cycle	Function	Control		Check Bit	CB Control I/O	Error Flags	
		S <sub>1</sub>	S <sub>0</sub>			SEF	DEF
Write	Generate Check Bits	L	L	Output Check	L	H	H
Read	Read & Flag	H	L	Input	H	Enabled	
Read	Latch Check Bits	H	H	Inputs	H	Enabled	
Read	Output Syndrome Bits	H	H	Output Syndrome Bits	L	Enabled	
Diagnostics	Input Diagnostic Data Word	H	H	Latched Check	H	Enabled	
	Input Diagnostic Data Word	L	H	Output Latched	L	Enabled	
	Input Diagnostic Data Word	H	H	Check Bits	L	Enabled	
Diagnostics	Input Diagnostic Data Word	H	H	Output Syndrome Bits	L	Enabled	

## Block Diagram



TL/F/9542-4

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA, D <sub>n</sub> , CB, S <sub>0</sub> , S <sub>1</sub>
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA (All Outputs)
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA (C <sub>0</sub> –C <sub>6</sub> )
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA (All Outputs)
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA (C <sub>0</sub> –C <sub>6</sub> )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA (All Outputs)
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −3 mA (C <sub>0</sub> –C <sub>6</sub> )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA (All Outputs)
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA (DEF, SEF)
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA (C <sub>0</sub> –C <sub>6</sub> )
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>ID</sub> = 1.50 mV All Other Pins Grounded
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)			1.0	mA	Max	V <sub>IN</sub> = 5.5V (C <sub>0</sub> –C <sub>6</sub> )
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V (D <sub>n</sub> , CB, S <sub>0</sub> , S <sub>1</sub> )
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (C <sub>0</sub> –C <sub>6</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			−650	μA	Max	V <sub>OUT</sub> = 0.5V (C <sub>0</sub> –C <sub>6</sub> )
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current			130	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			130	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current			130	mA	Max	V <sub>O</sub> = HIGH Z

## Recommended Operating Conditions

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

		V <sub>CC</sub> = 5.0V C <sub>L</sub> = 50 pF			C <sub>L</sub> = 50 pF		C <sub>L</sub> = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	5.0		20.0			5.0	22.0	ns	420-a, b
t <sub>PHL</sub>	D <sub>n</sub> to C <sub>n</sub>	5.0		17.0			5.0	19.0		
t <sub>PLH</sub>	Propagation Delay	5.0		20.0			5.0	22.0	ns	420-b
t <sub>PHL</sub>	D <sub>n</sub> /C <sub>n</sub> to SEF	4.0		16.0			4.0	18.0		
t <sub>PLH</sub>	Propagation Delay	6.0		24.0			6.0	26.0	ns	420-b
t <sub>PHL</sub>	D <sub>n</sub> /C <sub>n</sub> to DEF	5.0		21.0			5.0	22.0		
t <sub>PLH</sub>	Propagation Delay	4.0		18.0			4.0	19.0	ns	420-a, b
t <sub>PHL</sub>	S1 to C <sub>n</sub>	3.0		13.0			3.0	14.0		
t <sub>PLH</sub>	Propagation Delay	4.0		14.0			4.0	15.0	ns	420-b
t <sub>PHL</sub>	S1 to SEF/DEF	3.0		9.0			3.0	10.0		
t <sub>PZH</sub>	Output Enable Time	2.0		12.0			2.0	13.0	ns	
t <sub>PZL</sub>		2.0		11.0			2.0	12.0		
t <sub>PHZ</sub>	Output Disable Time	1.0		7.5			1.0	8.0		
t <sub>PLZ</sub>		1.0		7.5			1.0	8.0		

### AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> , V <sub>CC</sub> = Mil		T <sub>A</sub> , V <sub>CC</sub> = Com			
		Min	Max	Min	Max	Min	Max		
t <sub>S</sub> (H) t <sub>S</sub> (L)	Setup Time, HIGH or LOW C <sub>n</sub> to S <sub>0</sub>	5.0 5.0				5.0 5.0		ns	2-6
t <sub>H</sub> (H) t <sub>H</sub> (L)	Hold Time, HIGH or LOW C <sub>n</sub> to S <sub>0</sub>	5.0 5.0				5.0 5.0		ns	2-6
t <sub>w</sub> (L)	Clock Pulse Width LOW	8.0				8.0		ns	2-4





## 54F/74F432

### Multi-Mode Buffered Latch with TRI-STATE® Outputs

#### General Description

The 'F432 is an 8-bit latch with TRI-STATE output buffers and control and device selection logic. Also included is a status flip-flop for providing device-busy or request-interrupt commands. Separate Mode and Select inputs allow data to be stored with the outputs enabled or disabled. The device can also operate in a fully transparent mode.

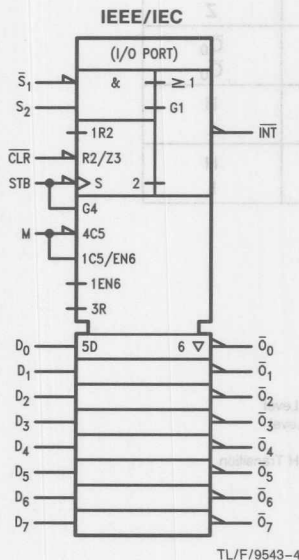
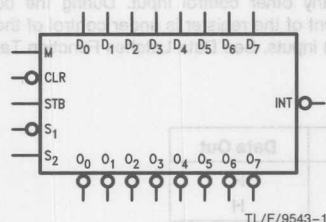
The 'F432 is the functional equivalent of the Intel 8212, but with inverting outputs.

#### Features

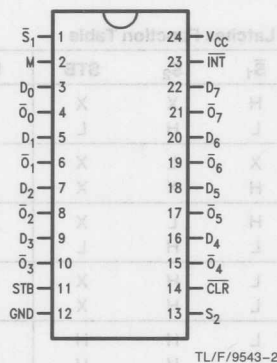
- TRI-STATE inverting outputs
- Status flip-flop for interrupt commands
- Asynchronous or latched receiver modes
- Data to output propagation delay typically 8.5 ns
- Supply current 43 mA typ
- 24-pin slim package

**Ordering Code:** See Section 5

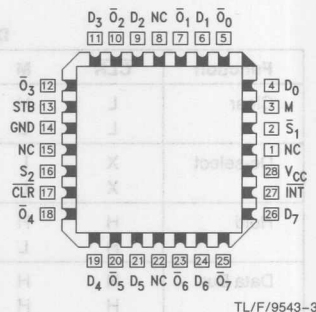
#### Logic Symbols



**Pin Assignment  
for DIP, SOIC and Flatpak**



**Pin Assignment  
for LCC**



INT	STB	S2	S1	CLR
H	X	X	H	L
L	X	L	X	H
L	~	X	X	H
L	X	H	L	H



# Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$D_0-D_7$	Data Inputs	1.0/1.0	20 $\mu$ A / -0.6 mA
$\bar{O}_0-\bar{O}_7$	Latch Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)
$\bar{S}_1, \bar{S}_2$	Select Inputs	1.0/1.0	20 $\mu$ A / -0.6 mA
M	Mode Control Input	1.0/1.0	20 $\mu$ A / -0.6 mA
STB	Strobe	1.0/1.0	20 $\mu$ A / -0.6 mA
$\bar{INT}$	Interrupt	50/33.3	-1 mA/20 mA
CLR	Clear	1.0/1.0	20 $\mu$ A / -0.6 mA

## Functional Description

This high-performance eight-bit parallel expandable buffer register incorporates package and mode selection inputs and an edge-triggered status flip-flop designed specifically for implementing bus-organized input/output ports. The TRI-STATE data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides busy or request interrupt commands.

The eight data latches are fully transparent when the internal gate enable, G, input is HIGH and the outputs are enabled. Latch transparency is selected by the mode control (M), select ( $\bar{S}_1$  and  $\bar{S}_2$ ), and the strobe (STB) inputs and during transparency each data output ( $\bar{O}_n$ ) follows its respective data input ( $D_n$ ). This mode of operation can be

terminated by clearing, de-selecting, or holding the data latches. See Data Latches Function Table.

An input mode or an output mode is selectable from this single input line. In the input mode, M = L, the eight data latch inputs are enabled when the strobe is HIGH regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken LOW the latches will store the most recently setup data.

In the output mode, M = H, the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the select ( $\bar{S}_1$  and  $\bar{S}_2$ ) inputs. See Data Latches Function Table.

Data Latches Function Table

Function	CLR	M	$\bar{S}_1$	$\bar{S}_2$	STB	Data In	Data Out
Clear	L	H	H	X	X	X	H
	L	L	L	H	L	X	H
De-select	X	L	X	L	X	X	Z
	X	L	H	X	X	X	Z
Hold	H	H	H	L	X	X	$\bar{Q}_0$
	H	L	L	H	L	X	$\bar{Q}_0$
Data Bus	H	H	L	H	X	L	H
	H	H	L	H	X	H	L
Data Bus	H	L	L	H	H	L	H
	H	L	L	H	H	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Status Flip-Flop Function Table

CLR	$\bar{S}_1$	$\bar{S}_2$	STB	$\bar{INT}$
L	H	X	X	H
L	X	L	X	H
H	X	X	—	L
H	L	H	X	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

— = LOW-to-HIGH Transition



**Office/Distributors for availability and specifications.**

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	-0.5V to V <sub>CC</sub>
Standard Output TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Free Air Ambient Temperature**

Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.4 2.5 2.4 2.7 2.7			V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5		V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0		μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0		μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50		μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75		μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)			1.0		mA	Max	V <sub>IN</sub> = 5.5V
I <sub>IL</sub>	Input LOW Current			-0.6		mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50		μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			-50		μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150		mA	Max	V <sub>OUT</sub> = 0V

# DC Electrical Characteristics (Continued)

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current		50	65	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		50	65	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		50	65	mA	Max	V <sub>O</sub> = HIGH Z

## AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D <sub>n</sub> to $\overline{O}_n$	3.5 2.5	8.5 5.5	10.5 7.0			3.0 3.0	12.0 12.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\overline{S}_1$ , S <sub>2</sub> or STB to $\overline{O}_n$	8.5 6.5	16.0 12.5	21.0 16.0			7.5 5.5	23.0 18.0	ns	2-3
t <sub>PHL</sub>	Propagation Delay $\overline{CLR}$ to $\overline{O}_n$	7.0	15.0	18.5			6.0	20.5	ns	2-3
t <sub>PHL</sub>	Propagation Delay STB to $\overline{INT}$	6.0	11.5	14.5			5.0	16.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\overline{S}_1$ to $\overline{INT}$	4.0 5.5	7.5 7.5	9.5 12.0			3.5 5.5	10.5 13.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S <sub>2</sub> to $\overline{INT}$	4.0 4.5	7.5 7.5	9.5 9.5			3.5 4.5	10.5 10.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay M to $\overline{O}_n$	9.0 6.5	15.0 11.0	19.0 14.0			9.0 6.5	20.0 15.0	ns	2-3
t <sub>PZH</sub> t <sub>PZL</sub>	Enable Time M to $\overline{O}_n$	6.0 6.0	8.5 8.5	14.0 13.0			6.0 6.0	15.0 14.5	ns	2-5
t <sub>PHZ</sub> t <sub>PLZ</sub>	Disable Time M to $\overline{O}_n$	4.5 5.5	6.5 9.5	9.5 12.0			4.5 5.5	10.5 13.0	ns	2-5
t <sub>PZH</sub> t <sub>PZL</sub>	Enable Time $\overline{S}_1$ , S <sub>2</sub> to $\overline{O}_n$	4.5 5.0	13.0 11.0	18.0 15.0			4.0 4.0	20.0 17.0	ns	2-5
t <sub>PHZ</sub> t <sub>PLZ</sub>	Disable Time $\overline{S}_1$ , S <sub>2</sub> to $\overline{O}_n$	4.0 5.0	8.0 11.0	11.0 15.5			3.5 4.0	12.5 17.5		

# AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $\bar{S}_1$ to $D_n$	0 0				0 0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $\bar{S}_1$ to $D_n$	11.0 8.5				12.5 9.5			
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $S_2$ to $D_n$	0 0				0 0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $S_2$ to $D_n$	9.0 7.0				9.0 7.0		ns	2-6
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW STB to $D_n$	0 0				0 0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW STB to $D_n$	13.0 10.0				13.0 10.0		ns	2-6
$t_w(\text{H})$ $t_w(\text{L})$	STB Pulse Width HIGH or LOW	5.0 5.0				5.0 5.0		ns	2-4
$t_w(\text{L})$	$\overline{\text{CLR}}$ Pulse Width, LOW	10.0				10.0		ns	2-4
$t_w(\text{H})$ $t_w(\text{L})$	$\bar{S}_1$ Pulse Width HIGH or LOW	9.0 7.0				9.0 7.0		ns	2-4
$t_w(\text{H})$ $t_w(\text{L})$	$S_2$ Pulse Width HIGH or LOW	7.0 9.0				7.0 9.0		ns	2-4

## 54F/74F433

### First-In First-Out (FIFO) Buffer Memory

#### General Description

The 'F433 is an expandable fall-through type high-speed first-in first-out (FIFO) buffer memory that is optimized for high-speed disk or tape controller and communication buffer applications. It is organized as 64 words by 4 bits and may be expanded to any number of words or any number of bits in multiples of four. Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

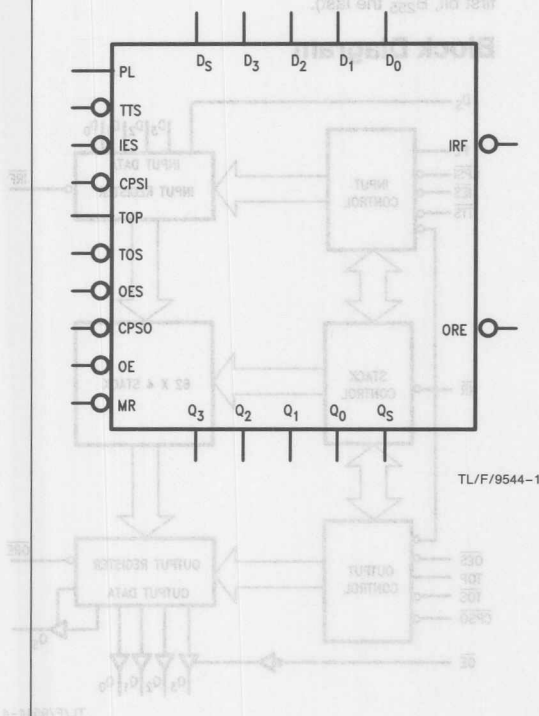
The 'F433 has TRI-STATE® outputs that provide added versatility, and is fully compatible with all TTL families.

#### Features

- Serial or parallel input
- Serial or parallel output
- Expandable without additional logic
- TRI-STATE outputs
- Fully compatible with all TTL families
- Slim 24-pin package
- 9423 replacement

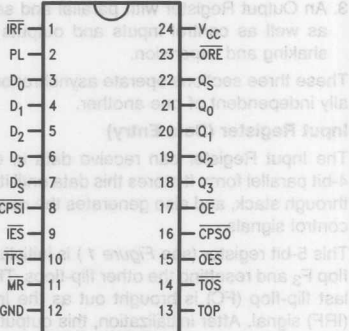
**Ordering Code:** See Section 5

#### Logic Symbol

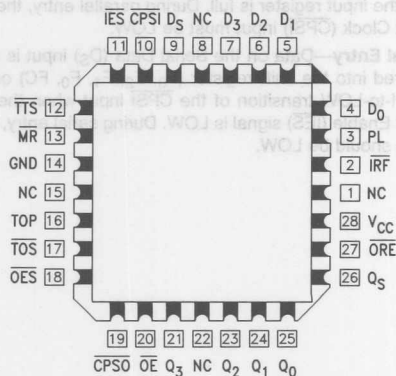


#### Connection Diagrams

##### Pin Assignment for DIP, SOIC and Flatpak



##### Pin Assignment for LCC





## Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
PL	Parallel Load Input	1.0/0.66	20 $\mu$ A/400 $\mu$ A
CPSI	Serial Input Clock	1.0/0.66	20 $\mu$ A/400 $\mu$ A
IES	Serial Input Enable	1.0/0.66	20 $\mu$ A/400 $\mu$ A
TTS	Transfer to Stack Input	1.0/0.66	20 $\mu$ A/400 $\mu$ A
MR	Master Reset	1.0/0.66	20 $\mu$ A/400 $\mu$ A
OES	Serial Output Enable	1.0/0.66	20 $\mu$ A/400 $\mu$ A
TOP	Transfer Out Parallel	1.0/0.66	20 $\mu$ A/400 $\mu$ A
TOS	Transfer Out Serial	1.0/0.66	20 $\mu$ A/400 $\mu$ A
CPSO	Serial Output Clock	1.0/0.66	20 $\mu$ A/400 $\mu$ A
OE	Output Enable	1.0/0.66	20 $\mu$ A/400 $\mu$ A
D <sub>0</sub> -D <sub>3</sub>	Parallel Data Inputs	1.0/0.66	20 $\mu$ A/400 $\mu$ A
D <sub>S</sub>	Serial Data Input	1.0/0.66	20 $\mu$ A/400 $\mu$ A
Q <sub>0</sub> -Q <sub>3</sub>	Parallel Data Outputs	285/10	5.7 mA/16 mA
Q <sub>S</sub>	Serial Data Output	285/10	5.7 $\mu$ A/16 mA
IRF	Input Register Full	20/5	400 $\mu$ A/8 mA
ORE	Output Register Empty	20/5	400 $\mu$ A/8 mA

## Functional Description

As shown in the block diagram, the 'F433 consists of three sections:

1. An Input Register with parallel and serial data inputs, as well as control inputs and outputs for input handshaking and expansion.
2. A 4-bit-wide, 62-word-deep fall-through stack with self-contained control logic.
3. An Output Register with parallel and serial data outputs, as well as control inputs and outputs for output handshaking and expansion.

These three sections operate asynchronously and are virtually independent of one another.

### Input Register (Data Entry)

The Input Register can receive data in either bit-serial or 4-bit parallel form. It stores this data until it is sent to the fall-through stack, and also generates the necessary status and control signals.

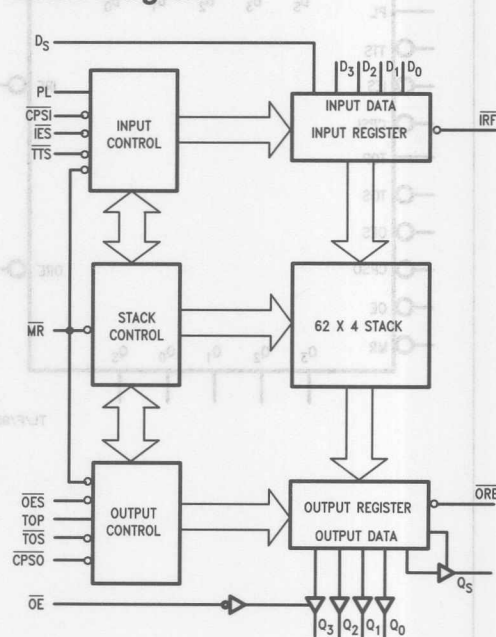
This 5-bit register (see Figure 1) is initialized by setting flip-flop F<sub>3</sub> and resetting the other flip-flops. The Q-output of the last flip-flop (FC) is brought out as the Input Register Full (IRF) signal. After initialization, this output is HIGH.

**Parallel Entry**—A HIGH on the Parallel Load (PL) input loads the D<sub>0</sub>-D<sub>3</sub> inputs into the F<sub>0</sub>-F<sub>3</sub> flip-flops and sets the FC flip-flop. This forces the IRF output LOW, indicating that the input register is full. During parallel entry, the Serial Input Clock (CPSI) input must be LOW.

**Serial Entry**—Data on the Serial Data (D<sub>S</sub>) input is serially entered into the shift register (F<sub>3</sub>, F<sub>2</sub>, F<sub>1</sub>, F<sub>0</sub>, FC) on each HIGH-to-LOW transition of the CPSI input when the Serial Input Enable (IES) signal is LOW. During serial entry, the PL input should be LOW.

After the fourth clock transition, the four data bits are located in flip-flops F<sub>0</sub>-F<sub>3</sub>. The FC flip-flop is set, forcing the IRF output LOW and internally inhibiting CPSI pulses from affecting the register. Figure 2 illustrates the final positions in an 'F433 resulting from a 256-bit serial bit train (B<sub>0</sub> is the first bit, B<sub>255</sub> the last).

## Block Diagram



TL/F/9544-4

## Functional Description (Continued)

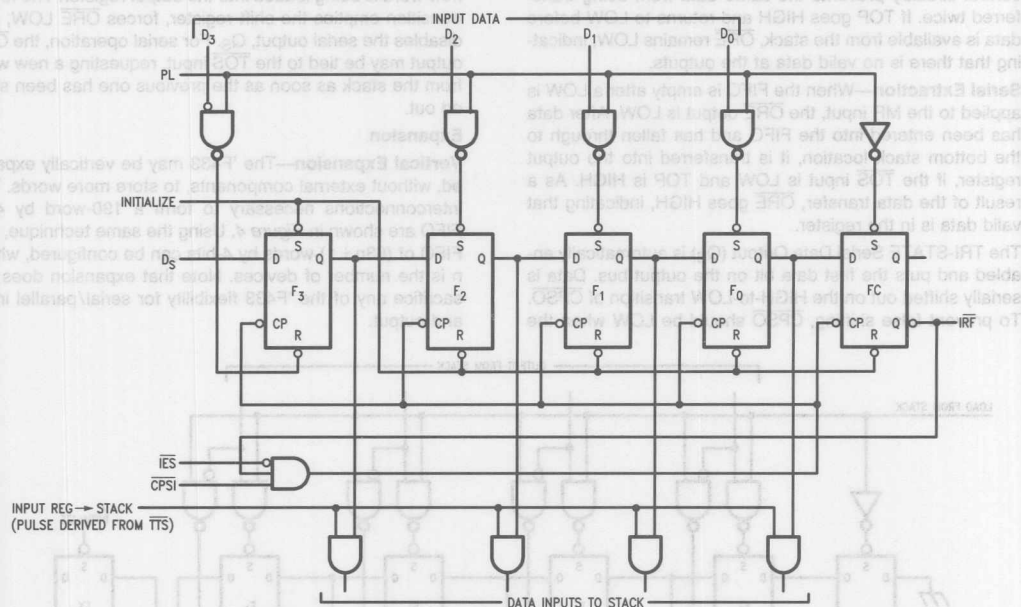
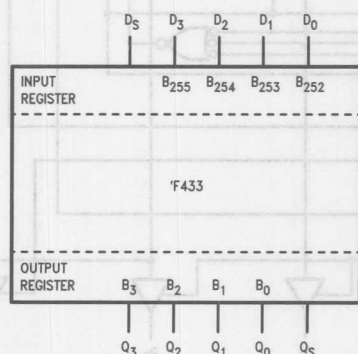


FIGURE 1. Conceptual Input Section

TL/F/9544-5



TL/F/9544-6

FIGURE 2. Final Positions in an 'F433 Resulting from a 256-Bit Serial Train

**Fall-Through Stack**—The outputs of flip-flops  $F_0$ – $F_3$  feed the stack. A LOW level on the Transfer to Stack (TTS) input initiates a fall-through action; if the top location of the stack is empty, data is loaded into the stack and the input register is reinitialized. (Note that this initialization is delayed until PL is LOW). Thus, automatic FIFO action is achieved by connecting the IRF output to the TTS input.

An RS-type flip-flop (the initialization flip-flop) in the control section records the fact that data has been transferred to the stack. This prevents multiple entry of the same word into the stack even though IRF and TTS may still be LOW; the initialization flip-flop is not cleared until PL goes LOW.

Once in the stack, data falls through automatically, pausing only when it is necessary to wait for an empty next location. In the 'F433, the master reset (MR) input only initializes the stack control section and does not clear the data.

### Output Register

The Output Register (see Figure 3) receives 4-bit data words from the bottom stack location, stores them, and outputs data on a TRI-STATE, 4-bit parallel data bus or on a TRI-STATE serial data bus. The output section generates and receives the necessary status and control signals.

**Parallel Extraction**—When the FIFO is empty after a LOW pulse is applied to the MR input, the Output Register Empty (ORE) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the output register, if the Transfer Out Parallel (TOP) input is HIGH. As a result of the data transfer, ORE goes HIGH, indicating valid data on the data outputs (provided that the TRI-STATE buffer is enabled). The TOP input can then be used to clock out the next word.

When TOP goes LOW, ORE also goes LOW, indicating that the output data has been extracted; however, the data itself remains on the output bus until a HIGH level on TOP permits the transfer of the next word (if available) into the output register. During parallel data extraction, the serial output clock (CPSO) line should be LOW. The Transfer Out Serial (TOS) line should be grounded for single-slice operation or connected to the appropriate ORE line for expanded operation (refer to the 'Expansion' section).

The TOP signal is not edge-triggered. Therefore, if TOP goes HIGH before data is available from the stack but data becomes available before TOP again goes LOW, that data is transferred into the output register. However, internal

new word is being loaded into the output register. The fourth transition empties the shift register, forces  $\overline{ORE}$  LOW, and disables the serial output,  $Q_S$ . For serial operation, the  $\overline{ORE}$  output may be tied to the  $TOS$  input, requesting a new word from the stack as soon as the previous one has been shifted out.

## Expansion

**Vertical Expansion**—The 'F433 may be vertically expanded, without external components, to store more words. The interconnections necessary to form a 190-word by 4-bit FIFO are shown in *Figure 4*. Using the same technique, any FIFO of  $(63n + 1)$ -words by 4-bits can be configured, where  $n$  is the number of devices. Note that expansion does not sacrifice any of the 'F433 flexibility for serial/parallel input and output.

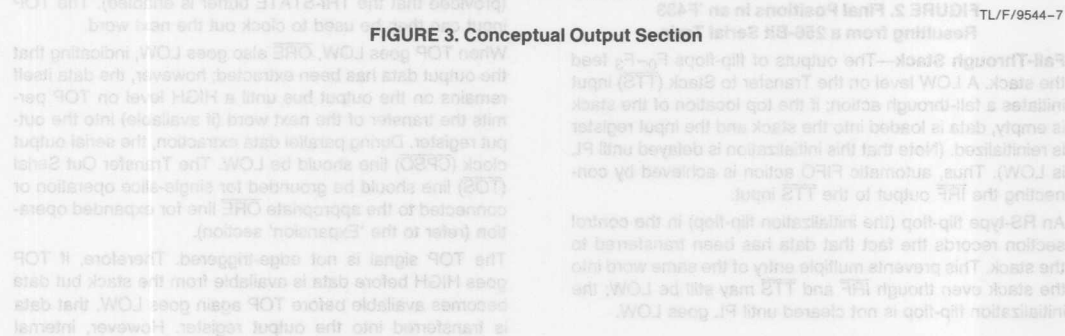


FIGURE 3. Conceptual Output Section

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## Functional Description (Continued)

**Horizontal Expansion**—The 'F433 can be horizontally expanded, without external logic, to store long words (in multiples of 4-bits). The interconnections necessary to form a 64-word by 12-bit FIFO are shown in Figure 5. Using the same technique, any FIFO of 64-words by 4n-bits can be constructed, where n is the number of devices.

The right-most (most significant) device is connected to the TTS inputs of all devices. Similarly, the ORE output of the most significant device is connected to the TOS inputs of all devices. As in the vertical expansion scheme, horizontal expansion does not sacrifice any of the 'F433 flexibility for serial/parallel input and output.

It should be noted that the horizontal expansion scheme shown in Figure 5 exacts a penalty in speed.

**Horizontal and Vertical Expansion**—The 'F433 can be expanded in both the horizontal and vertical directions without any external components and without sacrificing any of its FIFO flexibility for serial/parallel input and output. The interconnections necessary to form a 127-word by 16-bit FIFO are shown in Figure 6. Using the same technique, any FIFO of  $(63m + 1)$ -words by 4n-bits can be configured, where m is the number of devices in a column and n is the number of devices in a row. Figures 7 and 8 illustrate the timing diagrams for serial data entry and extraction for the FIFO shown in Figure 6. Figure 9 illustrates the final positions of bits in an expanded 'F433 FIFO resulting from a 2032-bit serial bit train.

**Interlocking Circuitry**—Most conventional FIFO designs provide status signal analogous to IRF and ORE. However, when these devices are operated in arrays, variations in unit-to-unit operating speed require external gating to ensure that all devices have completed an operation. The 'F433 incorporates simple but effective 'master/slave' interlocking circuitry to eliminate the need for external gating.

In the 'F433 array of Figure 6, devices 1 and 5 are the row masters; the other devices are slaves to the master in their rows. No slave in a given row initializes its input register until it has received a LOW on its IES input from a row master or a slave of higher priority.

Similarly, the ORE outputs of slaves do not go HIGH until their inputs have gone HIGH. This interlocking scheme ensures that new input data may be accepted by the array when the IRF output of the final slave in that row goes HIGH and that output data for the array may be extracted when the ORE output of the final slave in the output row goes HIGH.

The row master is established by connecting its IES input to ground, while a slave receives its IES input from the IRF output of the next-higher priority device. When an array of 'F433 FIFOs is initialized with a HIGH on the MR inputs of all devices, the IRF outputs of all devices are HIGH. Thus, only the row master receives a LOW on the IES input during initialization.

Figure 10 is a conceptual logic diagram of the internal circuitry that determines master/slave operation. When MR and IES are LOW, the master latch is set. When TTS goes LOW, the initialization flip-flop is set. If the master latch is HIGH, the input register is immediately initialized and the initialization flip-flop reset. If the master latch is reset, the input register is not initialized until IES goes LOW. In array operation, activating TTS initiates a ripple input register initialization from the row master to the last slave.

A similar operation takes place for the output register. Either a TOS or TOP input initiates a load-from-stack operation and sets the ORE request flip-flop. If the master latch is set, the last output register flip-flop is set and the ORE line goes HIGH. If the master latch is reset, the ORE output is LOW until a Serial Output Enable (OES) input is received.

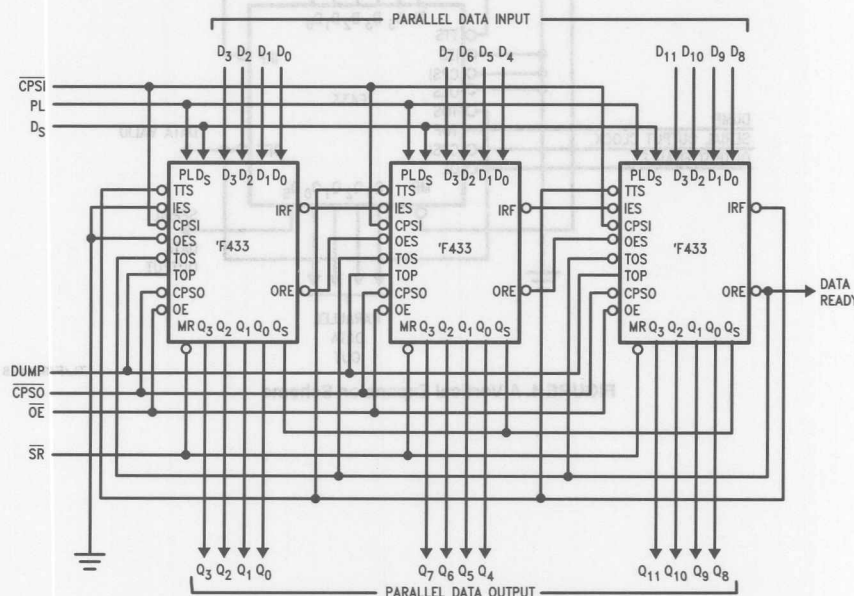
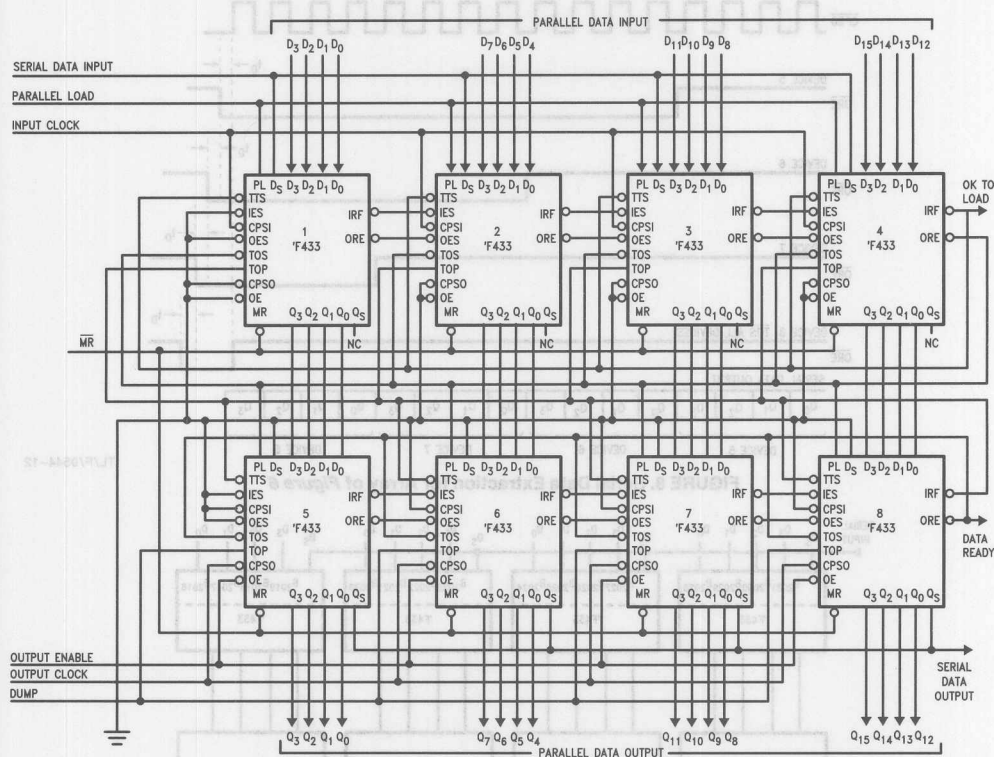


FIGURE 5. A Horizontal Expansion Scheme

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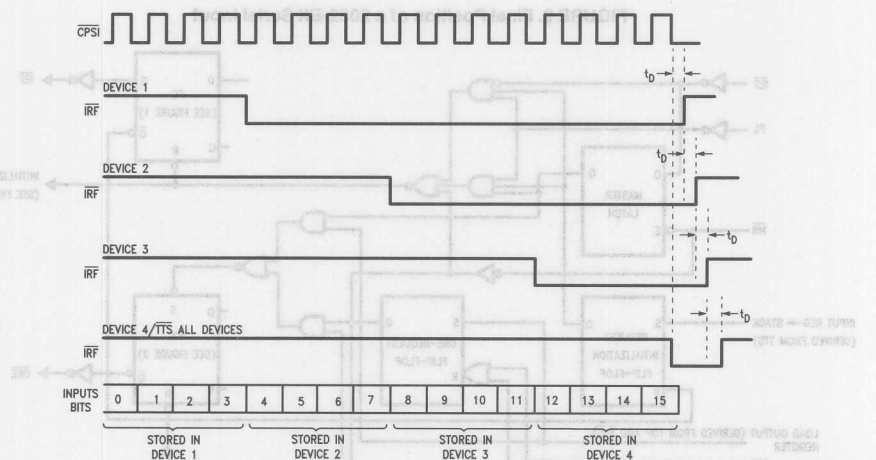


# Functional Description (Continued)



TL/F/9544-10

FIGURE 6. A 127 x 16 FIFO Array



TL/F/9544-11

FIGURE 7. Serial Data Entry for Array of Figure 6



## Functional Description (Continued)

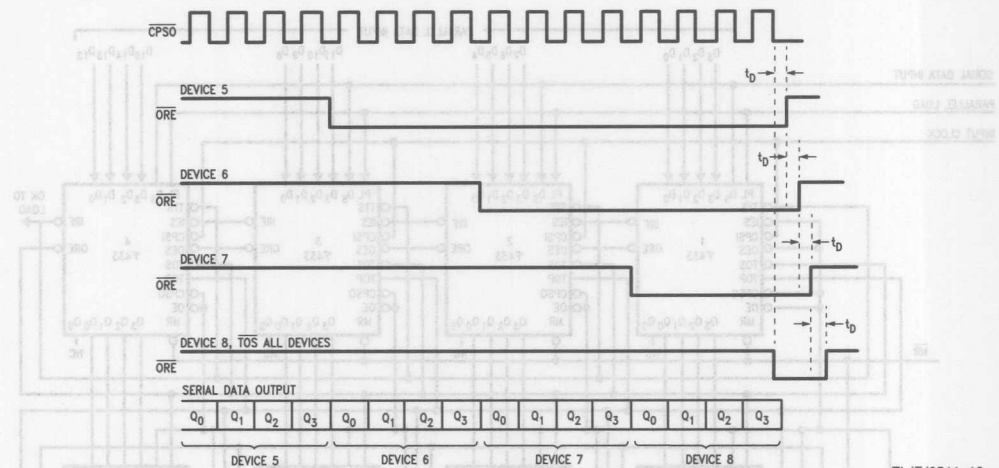
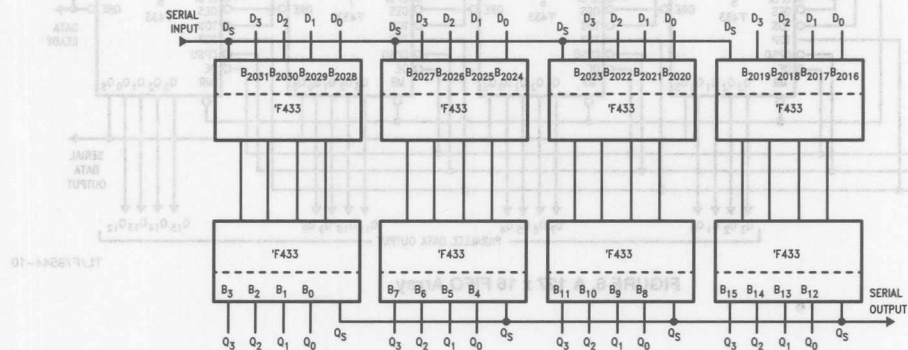


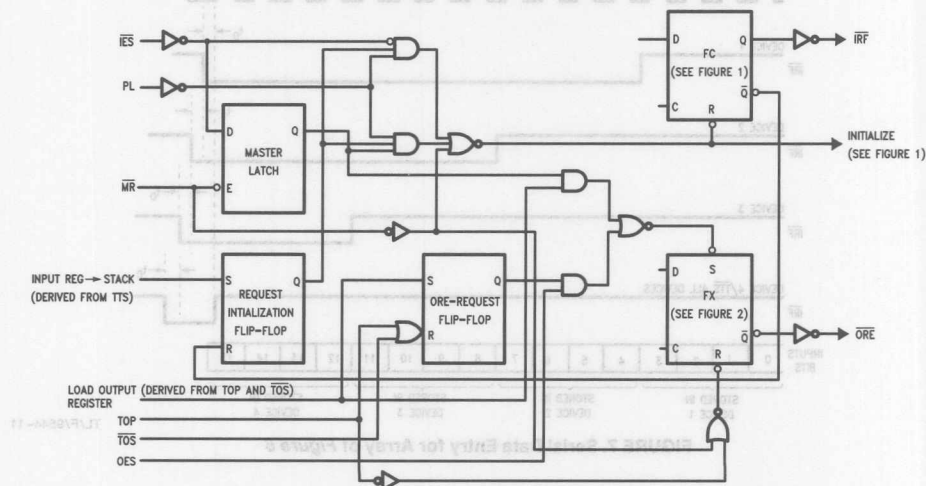
FIGURE 8. Serial Data Extraction for Array of Figure 6

TL/F/9544-12



TL/F/9544-13

FIGURE 9. Final Position of a 2032-Bit Serial Input



TL/F/9544-14

FIGURE 10. Conceptual Diagram, Interlocking Circuitry

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
---	----------------

Input Voltage (Note 2)	−0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	−30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
---	--------------------------

Standard Output	−0.5V to +5.5V
-----------------	----------------

TRI-STATE Output	−0.5V to +5.5V
------------------	----------------

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	−55°C to +125°C
Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.5	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.4		V	Min	I <sub>OH</sub> = 400 μA (ORE, IRF)
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = 5.7 mA (Q <sub>n</sub> , Q <sub>s</sub> )
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = 400 μA (ORE, IRF)
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = 5.7 mA (Q <sub>n</sub> , Q <sub>s</sub> )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = 400 μA (ORE, IRF)
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = 5.7 mA (Q <sub>n</sub> , Q <sub>s</sub> )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.50	V	Min	I <sub>OL</sub> = 8 mA (ORE, IRF)
		74F 10% V <sub>CC</sub>		0.50			I <sub>OL</sub> = 16 mA (Q <sub>n</sub> , Q <sub>s</sub> )
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.4	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V (Q <sub>n</sub> , Q <sub>s</sub> )
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V (Q <sub>n</sub> , Q <sub>s</sub> )
I <sub>OS</sub>	Output Short-Circuit Current		−20	−130	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		150	215	mA	Max	

		$C_L = 50 \text{ pF}$		$C_L = 50 \text{ pF}$		$C_L = 50 \text{ pF}$		Units	No.
		Min	Max	Min	Max	Min	Max		
$t_{PHL}$	Propagation Delay, Negative-Going CPSI to IRF Output	2.0	17.0			2.0	18.0	ns	433-a,b
$t_{PLH}$	Propagation Delay, Negative-Going TTS to IRF	9.0	34.0			8.0	38.0		
$t_{PLH}$ $t_{PHL}$	Propagation Delay, Negative-Going CPSO to Q <sub>S</sub> Output	4.0 5.0	25.0 20.0			3.0 5.0	27.0 21.0	ns	433-c,d
$t_{PLH}$ $t_{PHL}$	Propagation Delay, Positive-Going TOP to Q <sub>0</sub> -Q <sub>3</sub> Outputs	8.0 7.0	35.0 30.0			7.0 7.0	38.0 32.0	ns	433-e
$t_{PHL}$	Propagation Delay, Negative-Going CPSO to ORE	7.0	25.0			6.0	28.0	ns	433-c,d
$t_{PHL}$	Propagation Delay, Negative-Going TOP to ORE	6.0	26.0			6.0	28.0	ns	433-e
$t_{PLH}$	Propagation Delay, Positive-Going TOP to ORE	13.0	48.0			12.0	51.0		
$t_{PLH}$	Propagation Delay, Negative-Going TOS to Positive-Going ORE	13.0	45.0			12.0	50.0	ns	433-c,d
$t_{PHL}$	Propagation Delay, Positive-Going PL to Negative-Going IRF	4.0	22.0			4.0	23.0	ns	433-g,h
$t_{PLH}$	Propagation Delay, Negative-Going PL to Positive-Going IRF	7.0	31.0			6.0	35.0		
$t_{PLH}$	Propagation Delay, Positive-Going OES to ORE	9.0	38.0			8.0	44.0	ns	
$t_{PLH}$	Propagation Delay Positive-Going IES to Positive-Going	5.0	25.0			5.0	27.0	ns	433-h
$t_{PHL}$	Propagation Delay MR to ORE	7.0	28.0			7.0	31.0	ns	
$t_{PLH}$	Propagation Delay MR to IRF	5.0	27.0			5.0	30.0	ns	
$t_{PZH}$ $t_{PZL}$	Enable Time OE to Q <sub>0</sub> -Q <sub>3</sub>	1.0 1.0	16.0 14.0			1.0 1.0	18.0 16.0	ns	
$t_{PHZ}$ $t_{PLZ}$	Disable Time OE to Q <sub>0</sub> -Q <sub>3</sub>	1.0 1.0	10.0 23.0			1.0 1.0	12.0 30.0		
$t_{PZH}$ $t_{PZL}$	Enable Time Negative-Going OES to Q <sub>S</sub>	1.0 1.0	10.0 14.0			1.0 1.0	12.0 15.0	ns	
$t_{PHZ}$ $t_{PLZ}$	Disable Time Negative-Going OES to Q <sub>S</sub>	1.0 1.0	10.0 14.0			1.0 1.0	12.0 16.0		
$t_{PZH}$ $t_{PZL}$	Enable Time TOS to Q <sub>S</sub>	1.0 1.0	35.0 35.0			1.0 1.0	42.0 39.0	ns	
$t_{DFT}$	Fall-Through Time	0.2	0.9			0.2	1.0	ns	433-f
$t_{AP}$	Parallel Appearance Time ORE to Q <sub>0</sub> -Q <sub>3</sub>	-20.0	-2.0			-20.0	-2.0	ns	
$t_{AS}$	Serial Appearance Time ORE to Q <sub>S</sub>	-20.0	5.0			-20.0	5.0		

## AC Operating Requirements

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	7.0				7.0		ns	433-a,b
$t_s(\text{L})$	$D_S$ to Negative $\overline{\text{CPSI}}$	7.0				7.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0				2.0			
$t_h(\text{L})$	$D_S$ to $\overline{\text{CPSI}}$	2.0				2.0			
$t_s(\text{L})$	Setup Time, LOW $\overline{\text{TTS}}$ to $\overline{\text{IRF}}$ , Serial or Parallel Mode	0.0				0.0		ns	433-a,b,g,h
$t_s(\text{L})$	Setup Time, LOW Negative-Going $\overline{\text{ORE}}$ to Negative-Going $\overline{\text{TOS}}$	0.0				0.0		ns	433-c,d
$t_s(\text{L})$	Setup Time, LOW Negative-Going $\overline{\text{IES}}$ to $\overline{\text{CPSI}}$	8.0				9.0		ns	433-b
$t_s(\text{L})$	Setup Time, LOW Negative-Going $\overline{\text{TTS}}$ to $\overline{\text{CPSI}}$	30.0				33.0		ns	
$t_s(\text{H})$	Setup Time, HIGH or LOW	0.0				0.0		ns	
$t_s(\text{L})$	Parallel Inputs to PL	0.0				0.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	4.0				4.0			
$t_h(\text{L})$	Parallel Inputs to PL	4.0				4.0			
$t_w(\text{H})$	$\overline{\text{CPSI}}$ Pulse Width	10.0				11.0		ns	433-a,b
$t_w(\text{L})$	HIGH or LOW	5.0				6.0		ns	433-g,h
$t_w(\text{H})$	PL Pulse Width, HIGH	7.0				9.0		ns	
$t_w(\text{L})$	$\overline{\text{TTS}}$ Pulse Width, LOW Serial or Parallel Mode	7.0				9.0		ns	433-a,b,c,d
$t_w(\text{L})$	$\overline{\text{MR}}$ Pulse Width, LOW	7.0				9.0		ns	433-f
$t_w(\text{H})$	TOP Pulse Width	14.0				16.0		ns	433-e
$t_w(\text{L})$	HIGH or LOW	7.0				7.0		ns	
$t_w(\text{H})$	$\overline{\text{CPSO}}$ Pulse Width	14.0				16.0		ns	433-c,d
$t_w(\text{L})$	HIGH or LOW	7.0				7.0		ns	
$t_{\text{rec}}$	Recovery Time $\overline{\text{MR}}$ to Any Input	8.0				15.0		ns	433-f

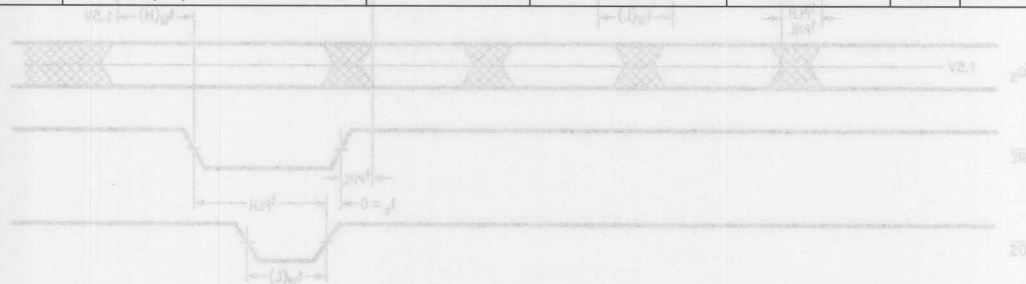
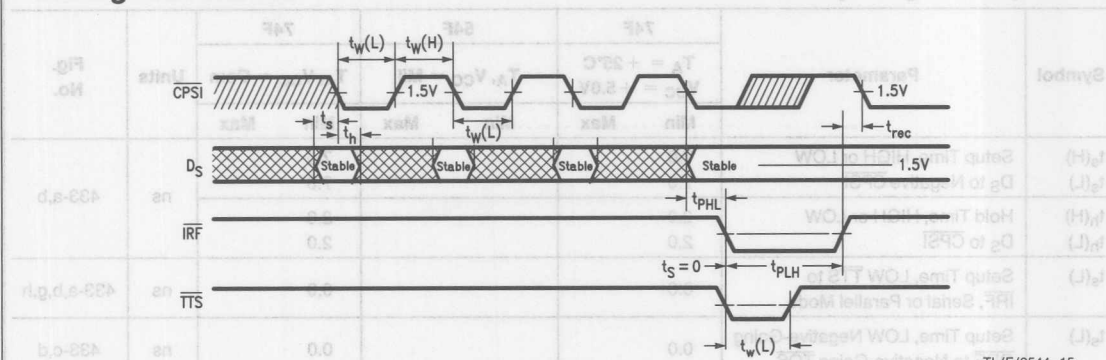
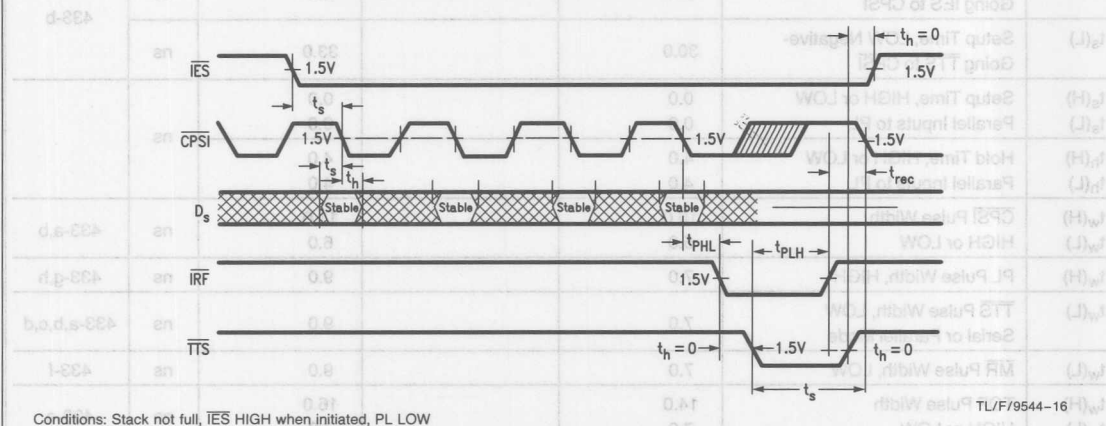


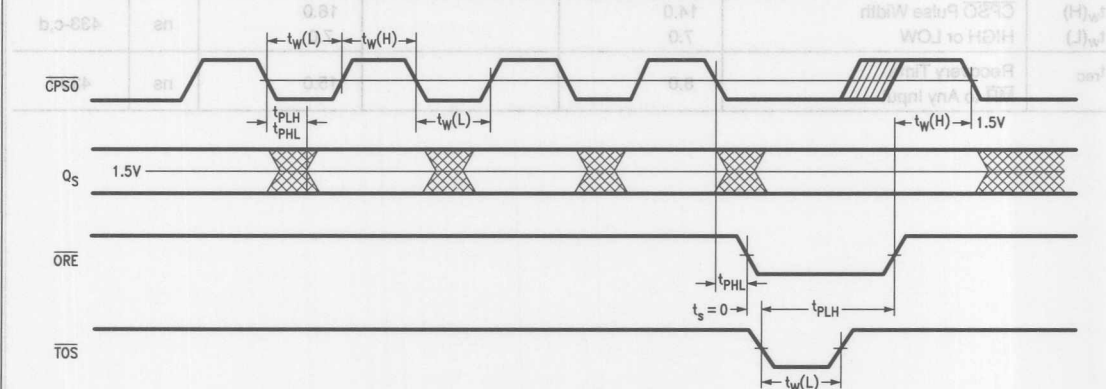
FIGURE 433-e Serial Output, Unexpanded or Master Operation  
Conditions: Data in stable, TOP HIGH, IES LOW when initiated, DES LOW



**FIGURE 433-a. Serial Input, Unexpanded or Master Operation**

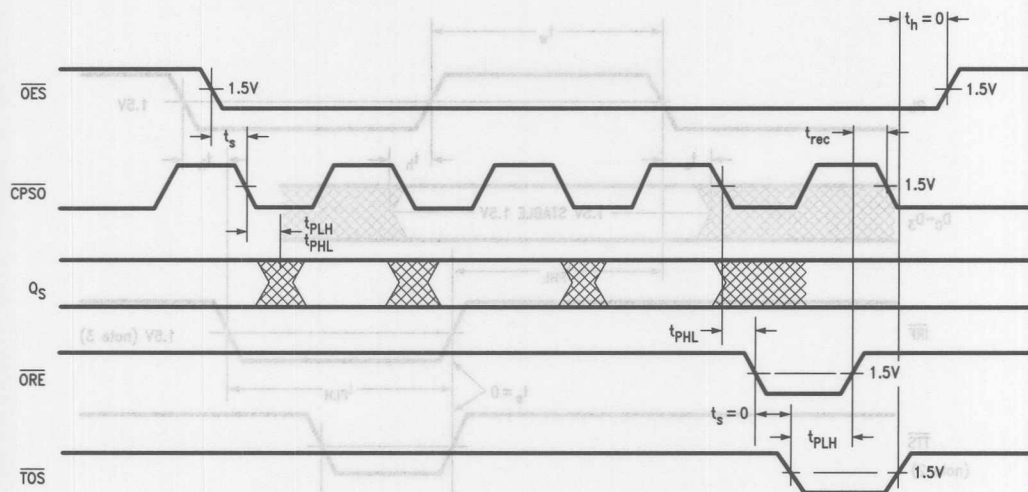


**FIGURE 433-b. Serial Input, Expanded Slave Operation**



**FIGURE 433-c. Serial Output, Unexpanded or Master Operation**

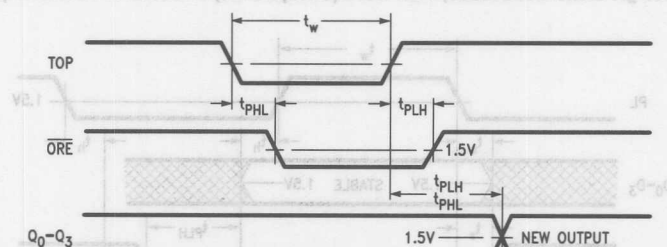
## Timing Waveforms (Continued)



Conditions: Data in stack, TOP HIGH,  $\overline{IES}$  HIGH when initiated

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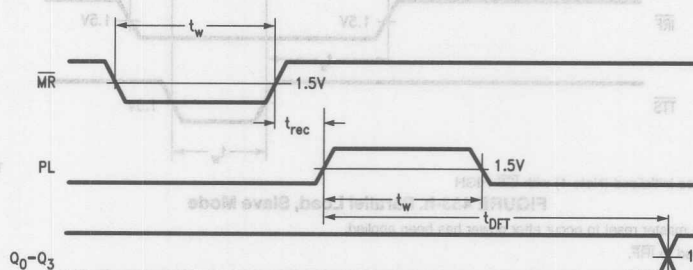
FIGURE 433-d. Serial Output, Slave Operation



Conditions:  $\overline{IES}$  LOW when initiated,  $\overline{OE}$ ,  $\overline{CPSO}$  LOW; data available in stack

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FIGURE 433-e. Parallel Output, 4-Bit Word or Master in Parallel Expansion



Conditions:  $\overline{TTS}$  connected to IRF,  $\overline{TOS}$  connected to  $\overline{ORE}$ ,  $\overline{IES}$ ,  $\overline{OES}$ ,  $\overline{OE}$ ,  $\overline{CPSO}$  LOW, TOP HIGH

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FIGURE 433-f. Fall Through Time



## Timing Waveforms (Continued)

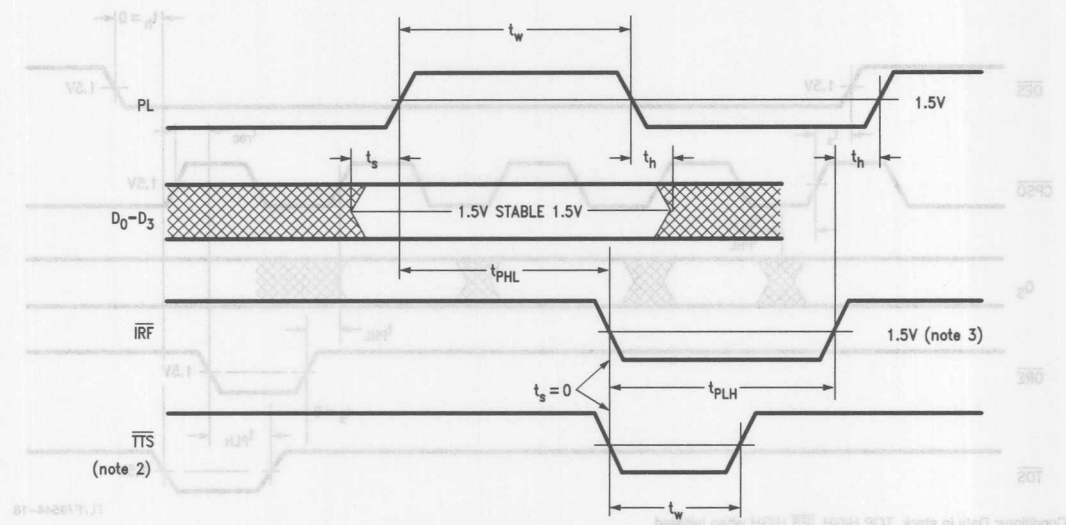


FIGURE 433-g. Parallel Load Mode, 4-Bit Word (Unexpanded) or Master in Parallel Expansion

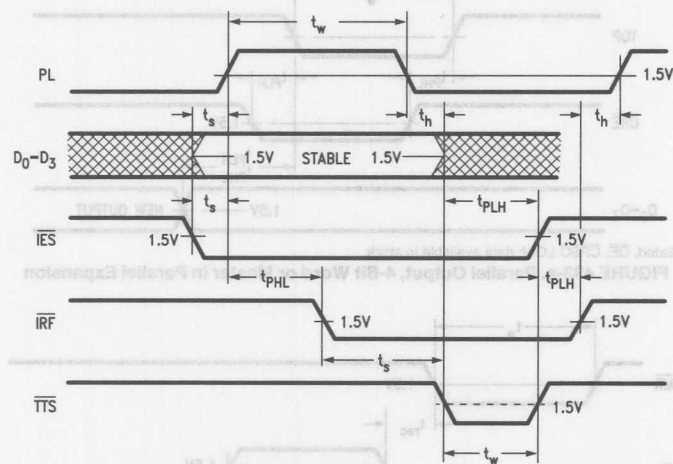


FIGURE 433-h. Parallel Load, Slave Mode

**Note 1:** Initialization requires a master reset to occur after power has been applied.

**Note 2:**  $\overline{TTS}$  normally connected to  $\overline{IRF}$ .

**Note 3:** If stack is full,  $\overline{IRF}$  will stay LOW.



## 54F/74F521 8-Bit Identity Comparator

### General Description

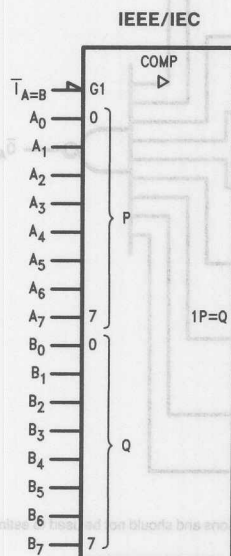
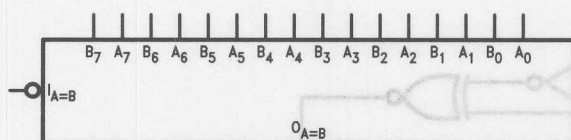
The 'F521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input  $\bar{I}_{A=B}$  also serves as an active LOW enable input.

### Features

- Compares two 8-bit words in 6.5 ns typ
- Expandable to any word length
- 20-pin package

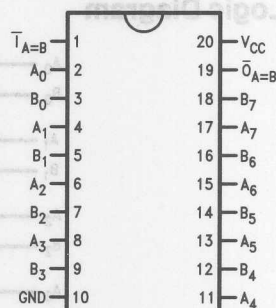
**Ordering Code:** See Section 5

### Logic Symbols

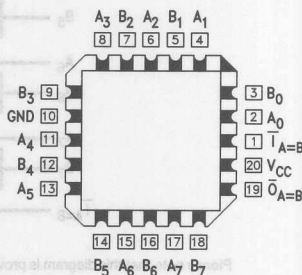


### Connection Diagrams

Pin Assignment  
for DIP, SOIC and Flatpak



Pin Assignment  
for LCC



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

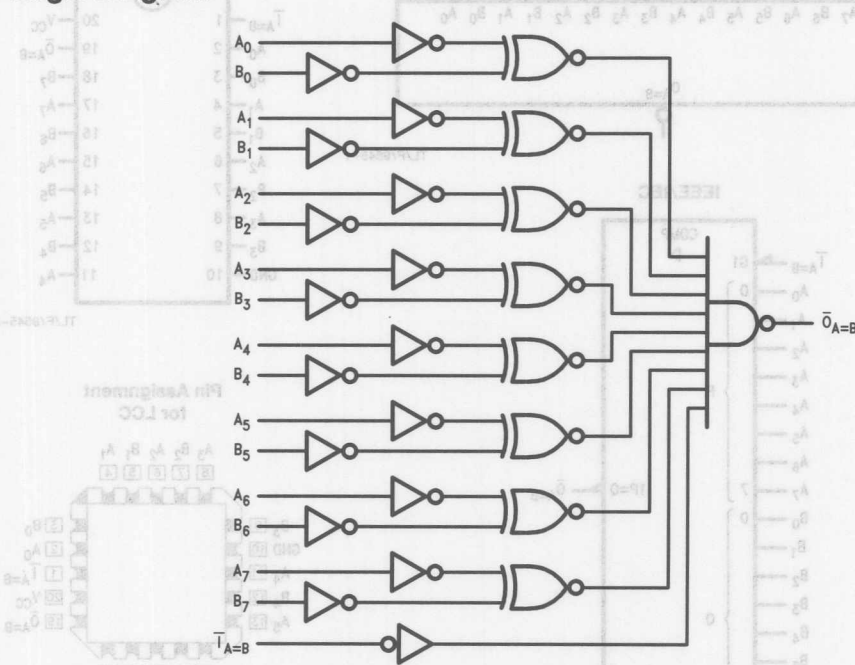
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_0-A_7$	Word A Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
$B_0-B_7$	Word B Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
$\bar{I}_A=B$	Expansion or Enable Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$\bar{O}_A=B$	Identity Output (Active LOW)	50/33.3	-1 mA/20 mA

**Truth Table**

Inputs		Output
$\bar{I}_A=B$	A, B	$\bar{O}_A=B$
L	$A=B^*$	L
L	$A \neq B$	H
H	$A=B^*$	H
H	$A \neq B$	H

H = HIGH Voltage Level

L = LOW Voltage Level

\* $A_0=B_0, A_1=B_1, A_2=B_2$ , etc.
**Logic Diagram**


TL/F/9545-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V

Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>

Standard Output TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	−55°C to +125°C
Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

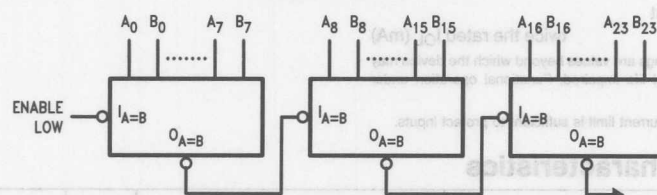
Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		21	32	mA	Max	V <sub>O</sub> = HIGH

# **AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{\text{PLH}}$	Propagation Delay	3.0	7.0	10.0	3.0	14.0	3.0	11.0	ns	2-3
$t_{\text{PHL}}$	$A_n$ or $B_n$ to $\overline{O}_{A=B}$	4.5	7.0	10.0	4.0	15.0	4.0	11.0		
$t_{\text{PLH}}$	Propagation Delay	3.0	5.0	6.5	3.0	8.5	3.0	7.5	ns	2-3
$t_{\text{PHL}}$	$\overline{I}_A = B$ to $\overline{O}_{A=B}$	3.5	6.5	9.0	3.5	13.5	3.5	10.0		

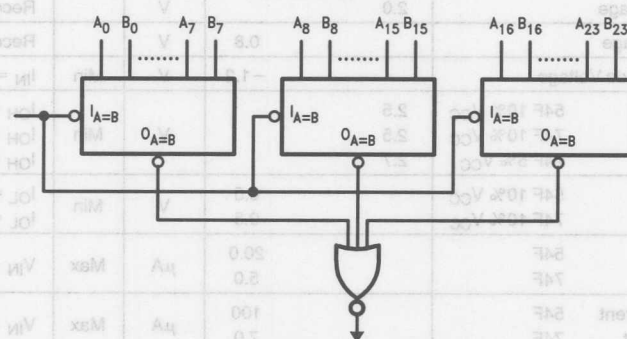
## **Applications**

### **Ripple Expansion**



TL/F/9545-6

### **Parallel Expansion**



TL/F/9545-7

## 54F/74F524 8-Bit Registered Comparator

### General Description

The 'F524 is an 8-bit bidirectional register with parallel input and output plus serial input and output progressing from LSB to MSB. All data inputs, serial and parallel, are loaded by the rising edge of the input clock. The device functions are controlled by two control lines ( $S_0$ ,  $S_1$ ) to execute shift, load, hold and read out.

An 8-bit comparator examines the data stored in the registers and on the data bus. Three true-HIGH, open-collector outputs representing 'register equal to bus', 'register greater than bus' and 'register less than bus' are provided. These outputs can be disabled to the OFF state by the use of Status Enable (SE). A mode control has also been provided

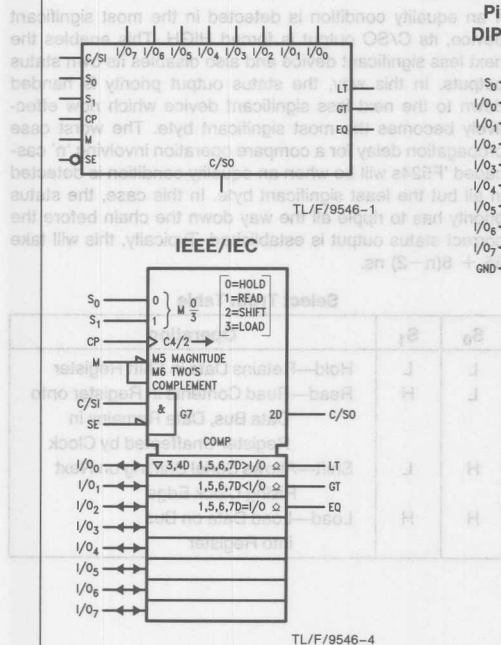
to allow two's complement as well as magnitude compare. Linking inputs are provided for expansion to longer words.

### Features

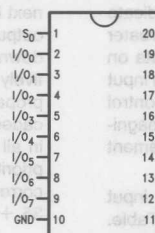
- 8-Bit bidirectional register with bus-oriented input-output
- Independent serial input-output to register
- Register bus comparator with 'equal to', 'greater than' and 'less than' outputs
- Cascadable in groups of eight bits
- Open-collector comparator outputs for AND-wired expansion
- Two's complement or magnitude compare

**Ordering Code:** See Section 5

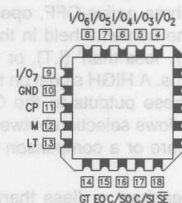
### Logic Symbols



### Pin Assignment for DIP, SOIC and Flatpak



### Pin Assignment for LCC





## Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$S_0, S_1$	Mode Select Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
C/SI	Status Priority or Serial Data Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{SE}$	Status Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
M	Compare Mode Select Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
$I/O_0-I/O_7$	Parallel Data Inputs or TRI-STATE® Parallel Data Outputs	3.5/1.083	70 $\mu$ A/ -0.65 mA
C/SO	Status Priority or Serial Data Output	150/40 (33.3)	-3 mA/24 mA (20 mA)
LT	Register Less Than Bus Output	50/33.3	-1 mA/20 mA
EQ	Register Equal Bus Output	OC*/33.3	OC*/20 mA
GT	Register Greater Than Bus Output	OC*/33.3	OC*/20 mA

\*OC = Open Collector

## Functional Description

The 'F524 contains eight D-type flip-flops connected as a shift register with provision for either parallel or serial loading. Parallel data may be read from or loaded into the registers via the data bus  $I/O_0-I/O_7$ . Serial data is entered from the C/SI input and may be shifted into the register and out through the C/SO output. Both parallel and serial data entry occur on the rising edge of the input clock (CP). The operation of the shift register is controlled by two signals  $S_0$  and  $S_1$  according to the Select Truth Table. The TRI-STATE parallel output buffers are enabled only in the Read mode.

One port of an 8-bit comparator is attached to the data bus while the other port is tied to the outputs of the internal register. Three active-OFF, open-collector outputs indicate whether the contents held in the shift register are 'greater than', (GT), 'less than' (LT), or 'equal to' (EQ) the data on the input bus. A HIGH signal on the Status Enable ( $\overline{SE}$ ) input disables these outputs to the OFF state. A mode control input (M) allows selection between a straightforward magnitude compare or a comparison between twos complement numbers.

For 'greater than' or 'less than' detection, the C/SI input must be held HIGH, as indicated in the Status Truth Table. The internal logic is arranged such that a LOW signal on the C/SI input disables the 'greater than' and 'less than' outputs. The C/SO output will be forced HIGH if the 'equal to' status condition exists, otherwise C/SO will be held LOW. These facilities enable the 'F524 to be cascaded for word length greater than eight bits.

Word length expansion (in groups of eight bits) can be achieved by connecting the C/SO output of the more significant byte to the C/SI input of the next less significant byte and also to its own  $\overline{SE}$  input (see Figure 1). The C/SI input of the most significant device is held HIGH while the  $\overline{SE}$  input of the least significant device is held LOW. The corresponding status outputs are AND-wired together. In the case of twos complement number compare, only the Mode input to the most significant device should be HIGH. The Mode inputs to all other cascaded devices are held LOW.

Suppose that an inequality condition is detected in the most significant device. Assuming that the byte stored in the register is greater than the byte on the data bus, the EQ and LT outputs will be pulled LOW and the GT output will float HIGH. Also the C/SO output of the most significant device will be forced LOW, disabling the subsequent devices but enabling its own status outputs. The correct status condition is thus indicated. The same applies if the registered byte is less than the data byte, only in this case the EQ and GT outputs go LOW and LT output floats HIGH.

If an equality condition is detected in the most significant device, its C/SO output is forced HIGH. This enables the next less significant device and also disables its own status outputs. In this way, the status output priority is handed down to the next less significant device which now effectively becomes the most significant byte. The worst case propagation delay for a compare operation involving 'n' cascaded 'F524s will be when an equality condition is detected in all but the least significant byte. In this case, the status priority has to ripple all the way down the chain before the correct status output is established. Typically, this will take  $35 + 6(n-2)$  ns.

Select Truth Table

$S_0$	$S_1$	Operation
L	L	Hold—Retains Data in Shift Register
L	H	Read—Read Contents in Register onto Data Bus, Data Remains in Register Unaffected by Clock
H	L	Shift—Allows Serial Shifting on Next Rising Clock Edge
H	H	Load—Load Data on Bus into Register

## Functional Description (Continued)

Number Representation Select Table

M	Operation
L	Magnitude Compare
H	Twos Complement Compare

Status Truth Table  
(Hold Mode)

Inputs			Outputs			
SE	C/SI	Data Comparison	EQ	GT	LT	C/SO
H	H	X	H	H	H	1
H	L	X	H	H	H	L
L	L	$O_A - O_H = 1/O_0 - 1/O_7$	L	H	H	L
L	L	$O_A - O_H = 1/O_0 - 1/O_7$	H	H	H	L
L	L	$O_A - O_H < 1/O_0 - 1/O_7$	L	H	H	L
L	H	$O_A - O_H > 1/O_0 - 1/O_7$	L	H	L	L
L	H	$O_A - O_H = 1/O_0 - 1/O_7$	H	L	L	H
L	H	$O_A - O_H < 1/O_0 - 1/O_7$	L	L	H	L

1 = HIGH if data are equal, otherwise LOW

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

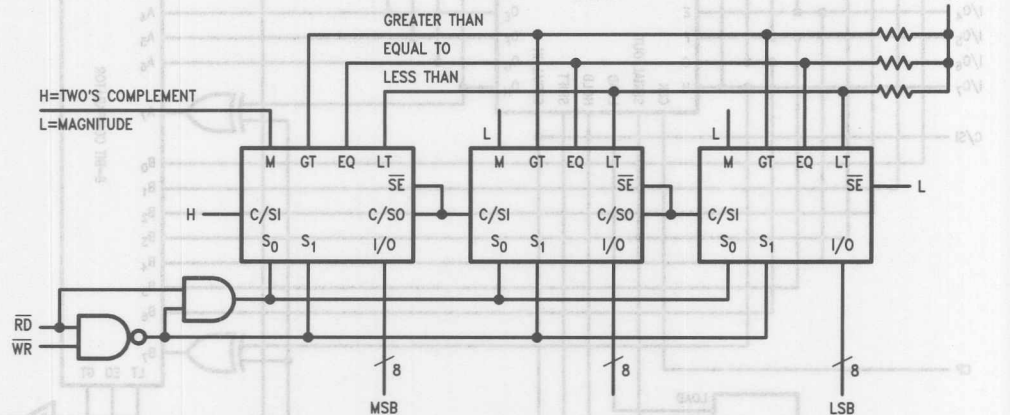
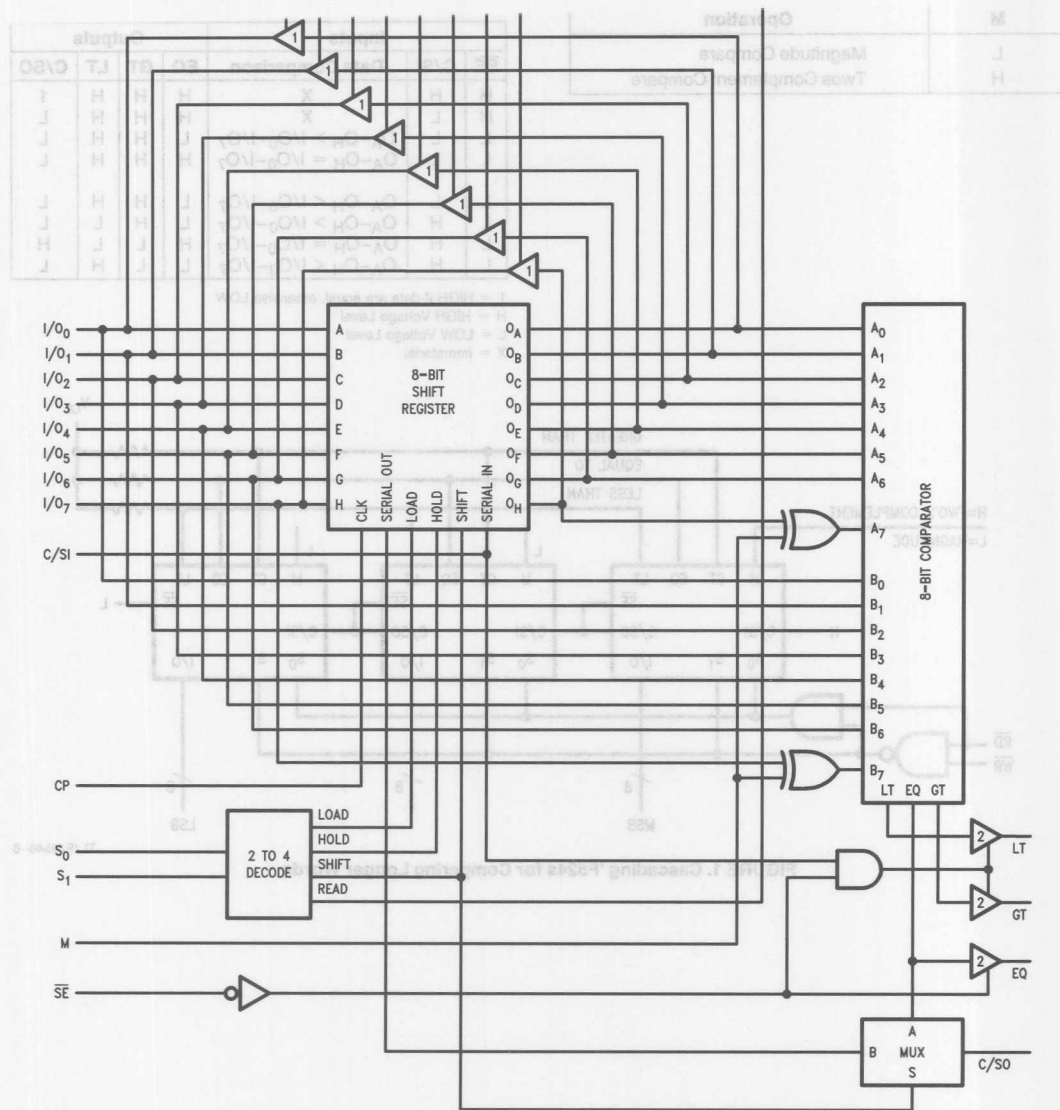


FIGURE 1. Cascading 7524s for Comparing Longer Words



**Notes:**

1. TRI-STATE Output
2. Open-Collector Output

TL/F/9546-5

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA

Voltage Applied to Output in HIGH State (with V<sub>CC</sub> = 0V)

Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA (I/O <sub>N</sub> )
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA (I/O <sub>N</sub> )
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA (LT, GT, EQ, C/SO)
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>I/O</sub> = 2.7V
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			−650	μA	Max	V <sub>I/O</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V

**DC Electrical Characteristics** (Continued)

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
I <sub>OHC</sub>	Open Collector, Output OFF Leakage Test			250	μA	Min	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>CC</sub> H	Power Supply Current		128	180	mA	Max	V <sub>O</sub> = HIGH
I <sub>CC</sub> L	Power Supply Current		128	180	mA	Max	V <sub>O</sub> = LOW
I <sub>CC</sub> Z	Power Supply Current		128	180	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f <sub>max</sub>	Maximum Shift Frequency	50	75				50		MHz	2-1
t <sub>PLH</sub>	Propagation Delay	9.0	16.5	20.0			9.0	21.0	ns	2-3
t <sub>PHL</sub>	I/O <sub>n</sub> to EQ	5.0	9.5	12.0			5.0	13.0		
t <sub>PLH</sub>	Propagation Delay	8.5	14.1	19.0			8.5	20.0		
t <sub>PHL</sub>	I/O <sub>n</sub> to GT	6.5	13.0	16.5			6.5	17.5		
t <sub>PLH</sub>	Propagation Delay	7.0	15.5	20.0			7.0	21.0	ns	2-3
t <sub>PHL</sub>	I/O <sub>n</sub> to LT	4.5	10.0	14.0			4.5	15.0		
t <sub>PLH</sub>	Propagation Delay	8.0	15.2	19.5			8.0	20.5		
t <sub>PHL</sub>	I/O <sub>n</sub> to C/SO	6.0	12.5	16.0			6.0	17.0		
t <sub>PLH</sub>	Propagation Delay	10.0	20.0	25.0			10.0	26.0	ns	2-3
t <sub>PHL</sub>	CP to EQ	4.0	8.5	16.5			4.0	17.5		
t <sub>PLH</sub>	Propagation Delay	10.0	16.5	21.0			10.0	22.0		
t <sub>PHL</sub>	CP to GT	8.5	17.0	22.0			8.5	23.0		
t <sub>PLH</sub>	Propagation Delay	9.0	20.0	25.0			9.0	26.0	ns	2-3
t <sub>PHL</sub>	CP to LT	5.5	13.5	17.0			5.5	18.0		
t <sub>PLH</sub>	Propagation Delay	8.5	16.5	21.0			8.5	22.0		
t <sub>PHL</sub>	CP to C/SO (Load)									
t <sub>PLH</sub>	Propagation Delay	5.0	10.0	13.0			5.0	14.0	ns	2-3
t <sub>PHL</sub>	CP to C/SO (Serial Shift)	4.5	9.0	11.5			4.5	12.5		
t <sub>PLH</sub>	Propagation Delay	9.0	15.0	19.0			9.0	20.0		
t <sub>PHL</sub>	C/SI to GT	3.0	6.5	8.5			3.0	9.5		
t <sub>PLH</sub>	Propagation Delay	8.0	15.5	20.0			8.0	21.0	ns	2-3
t <sub>PHL</sub>	C/SI to LT	3.5	6.5	8.5			3.5	9.5		
t <sub>PLH</sub>	Propagation Delay	6.5	11.5	14.5			6.5	15.5		
t <sub>PHL</sub>	S <sub>0</sub> , S <sub>1</sub> to C/SO	5.5	14.0	18.0			5.5	19.0		
t <sub>PLH</sub>	Propagation Delay	3.5	8.0	10.5			3.5	11.5	ns	2-3
t <sub>PHL</sub>	SE to EQ	2.5	6.0	8.0			2.5	9.0		
t <sub>PLH</sub>	Propagation Delay	6.5	12.5	16.0			6.5	17.0		
t <sub>PHL</sub>	SE to GT	3.5	6.0	8.0			3.5	9.0		
t <sub>PLH</sub>	Propagation Delay	5.0	10.5	13.5			5.0	14.5	ns	2-3
t <sub>PHL</sub>	SE to LT	3.5	6.0	8.0			3.5	9.0		
t <sub>PLH</sub>	Propagation Delay	4.0	8.5	11.0			4.0	12.0		
t <sub>PHL</sub>	C/SI to C/SO	4.0	8.5	11.0			4.0	12.0		

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay M to GT	8.0 6.0	15.0 12.0	19.5 15.5			8.0 6.0	20.5 16.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay M to LT	8.0 4.5	17.0 9.5	22.0 12.0			8.0 4.5	23.0 13.0		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_0, S_1$ to EQ	15.0 9.0	25.0 15.0	33.0 19.0			15.0 9.0	35.0 20.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_0, S_1$ to GT	10.5 10.5	18.0 18.0	23.0 23.0			10.5 10.5	24.0 24.0		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_0, S_1$ to LT	13.0 12.0	22.0 19.0	28.0 24.0			13.0 12.0	30.0 25.0		
$t_{PZH}$ $t_{PZL}$	Output Enable Time $S_0, S_1$ to I/O <sub>n</sub>	4.5 5.5	10.0 11.0	13.0 15.0			4.5 5.5	14.0 16.0	ns	2-5
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $S_0, S_1$ to I/O <sub>n</sub>	3.5 4.5	8.0 9.6	12.0 12.5			3.5 4.5	13.0 13.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW I/O <sub>n</sub> to CP	6.0 6.0				6.0 6.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW I/O <sub>n</sub> to CP	0 0				0 0			
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW S <sub>0</sub> or S <sub>1</sub> to CP	10.0 10.0				10.0 10.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW S <sub>0</sub> or S <sub>1</sub> to CP	0 0				0 0			
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW C/SI to CP	7.0 7.0				7.0 7.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW C/SI to CP	0 0				0 0			
$t_w(\text{H})$	Clock Pulse Width, HIGH	5.0				5.0		ns	2-4





## 54F/74F525 Programmable Counter

### General Description

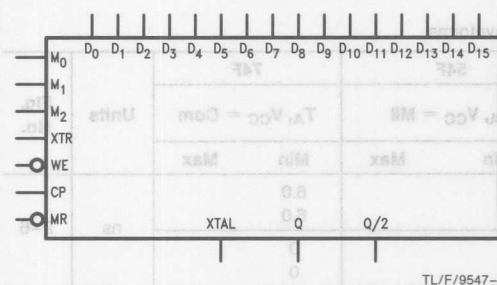
The 'F525 is a multi-function 28-pin device. It consists of a 16-bit count-down counter, logic to control the counter, logic to control the state of the outputs and a PLA to decode the particular function selected by the user. The list of high-speed timing applications include:

### Features

- Baud rate generator
- Digitally programmed monostable
- Variable system frequency generator
- Digital filter variable sampling rate
- 16-bit data path
- External trigger
- Extremely accurate one shot w/pulse widths from 50 ns to 3.27 ms @CP = 40 MHz

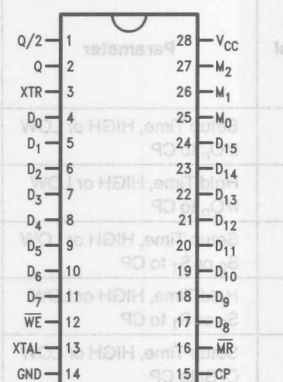
**Ordering Code:** See Section 5

### Logic Symbol

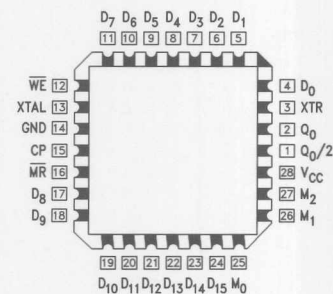


### Connection Diagrams

#### Pin Assignment DIP, SOIC and Flatpak



#### Pin Assignment for LCC and PCC



## Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
Q	Output (Primarily indicates when the counter has reached zero)	50/33.3	-1 mA/20 mA
Q/2	Output (Divides Q by 2)	50/33.3	-1 mA/20 mA
$M_0$ - $M_2$	Status Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
MR	Master Reset	1.0/1.0	20 $\mu$ A/-0.6 mA
CP	Clock Pulse	1.0/2.0	20 $\mu$ A/-1.2 mA
$D_0$ - $D_{15}$	Data Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
WE	Write Enable Input	1.0/1.0	20 $\mu$ A/-0.6 mA
XTR	External Trigger Input	1.0/3.0	20 $\mu$ A/-1.8 mA
XTAL	Crystal Output	1.0/1.0	20 $\mu$ A/-0.6 mA

## Functional Description

The multi-function aspect of the device consists of eight different modes of operation. An explanation of the operation of the device in each of the modes follows. However, there is one operation that is independent of the selected mode: the loading of data. Data is latched into a set of data latches when  $\overline{WE}$  is brought from a LOW to a HIGH state. The latches are transparent when  $\overline{WE}$  is held LOW.

### Operation Notes:

1. Device should be reset before operation.
2. The XTR input acts as a select line for the clock.
3. With XTR low, the clock goes into the counter.
4. With XTR high, the clock loads the counter.
5. In mode 4 and 5, during counting, the counter cannot be reloaded. XTR high freezes the count.
6. Mode 7 is the only auto-reload mode, all other modes require and XTR pulse to begin.
7. Loading 0 into the latches idles the device.

### MODE 0: Interval Timer with Level Output

While XTR is HIGH, the data in the data latches is loaded into the counter upon the next positive edge of CP. The negative edge of XTR enables the count-down to begin with the next positive edge of CP. When the count reaches zero, Q, normally LOW, is brought HIGH and Q/2 toggles state. Taking XTR HIGH at any time enables the data in the data latches to be loaded into the counter on the rising edge of CP and clears Q. See Figure 1.

### MODE 1: Interval Timer with Inverted Level Output

The operation is exactly the same as in Mode 0 except that Q is normally HIGH and goes LOW when the count reaches zero. Q/2 toggles on the negative-edge of Q. See Figure 1.

### MODE 2: Interval Timer with Pulse Output

While XTR is HIGH, the data in the data latches is loaded into the counter upon the next positive edge of CP. The negative edge of XTR enables the count-down to begin with the next positive edge of CP. When the count reaches

zero, Q, normally LOW, is brought HIGH for a single period of CP. Q/2 toggles state on the positive edge of Q. Taking XTR HIGH at any time causes the data in the data latches to be loaded into the counter on the rising edge of CP and clears Q. See Figure 2.

### MODE 3: Interval Timer with Inverted Pulse Output

The operation is exactly the same as in Mode 2 except that Q is normally HIGH and goes LOW for a single period of CP. Q/2 toggles on the negative edge of Q. See Figure 2.

Function Table

$M_2$	$M_1$	$M_0$	Function
0	0	0	Mode 0
0	0	1	Mode 1
0	1	0	Mode 2
0	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5
1	1	0	Mode 6
1	1	1	Mode 7

### MODE 4: Interval Timer, Pulse Output with Count Hold

While XTR is HIGH, the data in the data latches is loaded into the counter upon the next positive edge of CP. The negative edge of XTR enables the count-down to begin with the next positive edge of CP. When the count reaches zero, Q, normally low, is brought HIGH for a single period of CP. Q/2 toggles state on the positive edge of Q. Taking XTR HIGH before the counters reach zero, stops the count-down from the point where it was held. Data cannot be reloaded into the counter until a count of zero is reached. See Figure 3.

### MODE 5: Interval Timer, Inverted Pulse Output with Count Hold

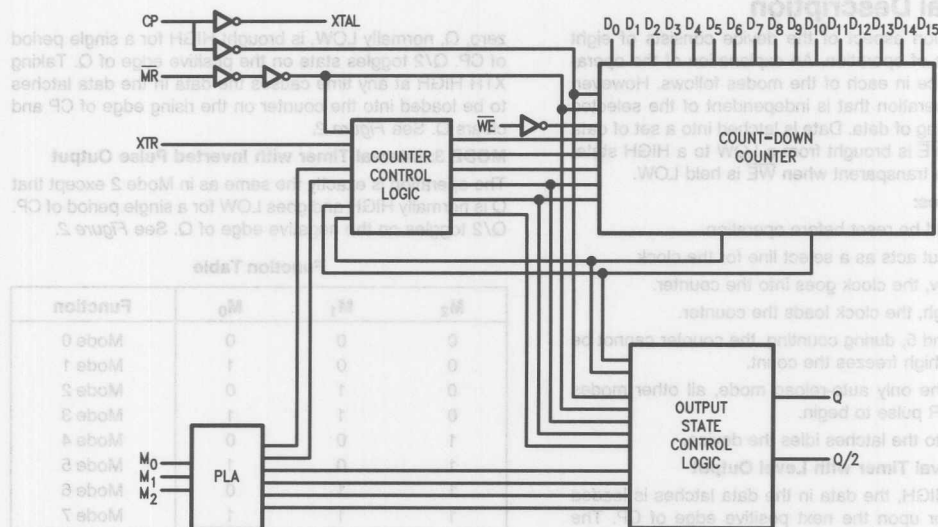
The operation is exactly the same as Mode 4 except that Q is normally HIGH and goes LOW for a single period of CP. Q/2 toggles on the negative-edge of Q. See Figure 3.

## Functional Description (Continued)

### MODE 6: Retriggerable Synchronous One-Shot

When XTR is HIGH, the data in the data latches is loaded into the counter upon the positive edge of CP. The negative edge of XTR enables the count-down to begin with the next positive edge of CP, where Q, normally LOW, is then brought HIGH and the counter is decremented when the count reaches zero, Q is brought LOW, and Q/2 is toggled. Bringing XTR HIGH during the count-down will allow the data in the data latches to be loaded into the counter with the next positive edge of CP, but will not affect Q. See Figure 4. NOTE that the pulse width of Q will be N-1 clock cycles, where N is the number loaded into the counter. N=1 should not be used as this may cause unpredictable results.

### Block Diagram



MODE 6: Interval Timer, Pulse Output with Count Hold  
While XTR is HIGH, the data in the data latches is loaded into the counter upon the next positive edge of CP. The negative edge of XTR enables the count-down to begin with the next positive edge of CP. When the count reaches zero, Q, normally LOW, is brought HIGH for a single period of CP. Q/2 toggles on the positive edge of CP. Taking XTR HIGH before the counters reach zero, stops the count-down from the point where it was held. Data cannot be reloaded into the counter until a count of zero is reached. See Figure 3.

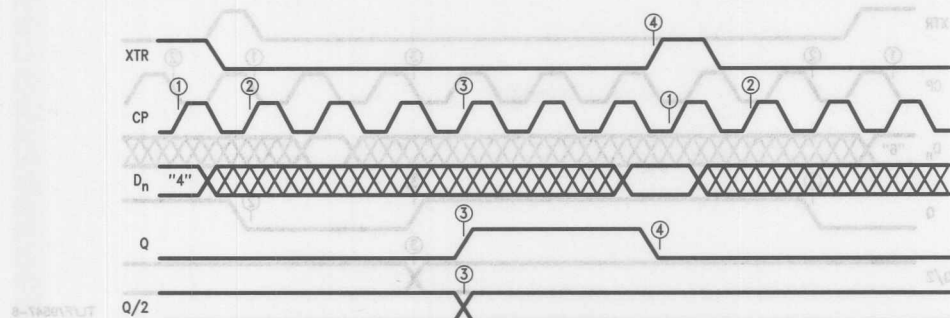
MODE 5: Interval Timer, Inverted Pulse Output with Count Hold  
The operation is exactly the same as Mode 4 except that Q is normally HIGH and goes LOW for a single period of CP. Q/2 toggles on the negative edge of CP. See Figure 2.

### MODE 7: Frequency Generator

When XTR is HIGH, the data in the data latches is loaded into the counter upon the positive edge of CP. The negative edge of XTR enables the count-down to begin with the next positive edge of CP. When the count reaches zero, Q, normally LOW, is brought HIGH for a single period of CP and Q/2 is toggled. The same clock edge that brings Q HIGH, also loads the data in the data latches into the counter. The counter will start to count on the next positive edge of CP. This mode will run continuously after an initial XTR until stopped by MR. Taking XTR HIGH at any time causes the data in the data latches to be loaded into the counter and Q output to be cleared with the next positive edge of CP. See Figure 5.

## Timing Diagrams

Timing Diagrams (Continued)



TL/F/9547-5

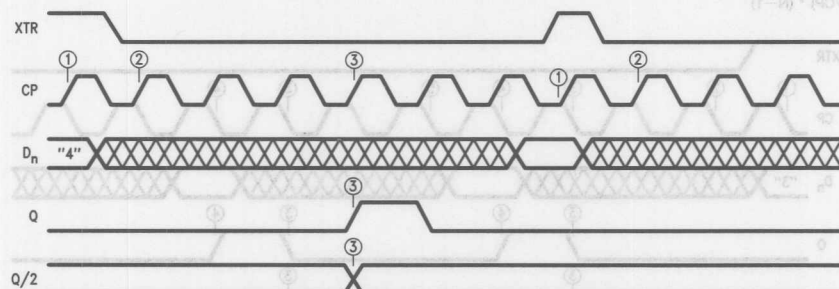
① With XTR HIGH, the rising edge of CP loads data from the latches to the counter.

② With XTR LOW, the rising edge of CP begins count-down cycle.

③ When the count reaches zero, Q goes HIGH, and Q/2 toggles state.

④ The next occurrence of XTR clears Q.

FIGURE 1. MODE 0 and MODE 1 (Inverse Output of Mode 0)

 $\bar{M}_n = 000, 001$ 

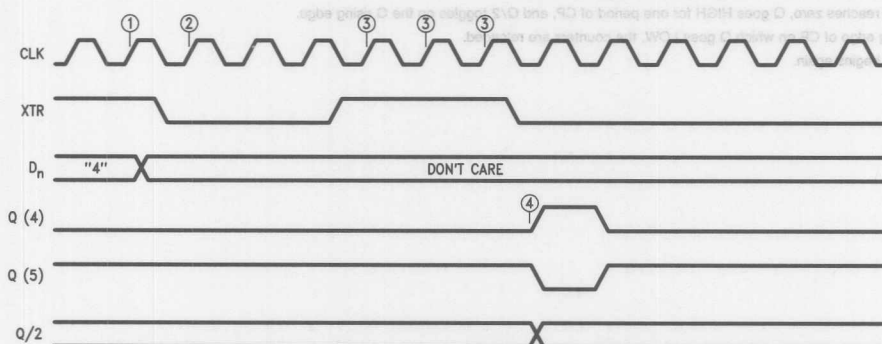
TL/F/9547-6

① With XTR HIGH, the rising edge of CP loads data from the latches to the counter.

② With XTR LOW, the rising edge of CP begins the count-down cycle.

③ When the count reaches zero, Q goes HIGH for one period of CP, and Q/2 toggles state.

FIGURE 2. MODE 2 and MODE 3 (Inverse Output of Mode 2)

 $\bar{M}_n = 010, 011$ 

TL/F/9547-7

FIGURE 3. MODE 4 and MODE 5

 $\bar{M}_n = 100, 101$ 

① With XTR HIGH, the rising edge of CP loads data from the latches into the counter.

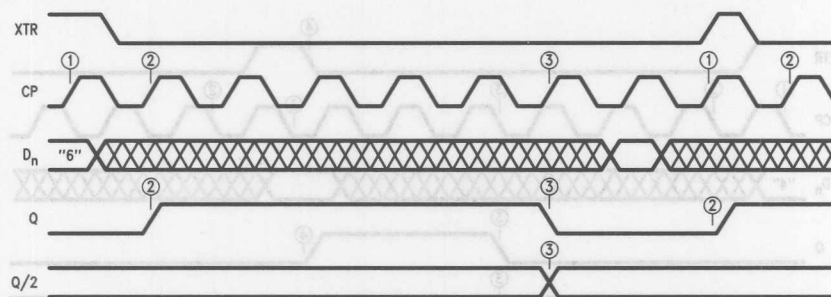
② With XTR LOW, the rising edge of CP begins the count-down.

③ With XTR HIGH, during count-down, the rising edge of CP does nothing.

④ When the count reaches zero, Q goes HIGH for one clock cycle and Q/2 toggles state.

**Note:** Once the count reaches zero, the counter can be reloaded with XTR HIGH.

## Timing Diagrams (Continued)



TL/F/9547-8

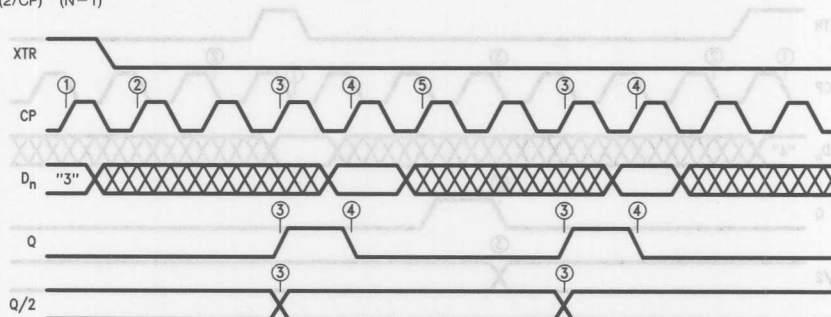
FIGURE 4. MODE 6

 $\bar{M}_n = 110$ 

- ① With XTR HIGH, the rising edge of CP loads data from the latches to the counter.
- ② With XTR LOW, the rising edge of CP begins the count, and Q goes HIGH.
- ③ When the count reaches zero, Q goes LOW, and Q/2 toggles state. Bringing XTR HIGH before count reaches zero will reload the counter, but not affect Q.

**Notes:**

Loading N=0 halts counter; loading N=1 will result in undefined operation.

Pulse width =  $(2/CP) * (N-1)$ 

TL/F/9547-9

FIGURE 5. MODE 7

 $\bar{M}_n = 111$ 

- ① With XTR HIGH, the rising edge of CP, loads data from the latches to the counter.
- ② On the falling edge of XTR, the rising edge of CP begins count-down.
- ③ When count reaches zero, Q goes HIGH for one period of CP, and Q/2 toggles on the Q rising edge.
- ④ On the rising edge of CP on which Q goes LOW, the counters are reloaded.
- ⑤ Count-down begins again.

**Office/Distributors for availability and specifications.**Storage Temperature  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ Ambient Temperature under Bias  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ Junction Temperature under Bias  $-55^{\circ}\text{C}$  to  $+175^{\circ}\text{C}$ **Free Air Ambient Temperature**

Military

Commercial

 $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ **Supply Voltage**

Military

Commercial

 $+4.5\text{V}$  to  $+5.5\text{V}$  $+4.5\text{V}$  to  $+5.5\text{V}$  $V_{\text{CC}}$  Pin Potential to

Ground Pin

 $-0.5\text{V}$  to  $+7.0\text{V}$ 

Input Voltage (Note 2)

 $-0.5\text{V}$  to  $+7.0\text{V}$ 

Input Current (Note 2)

 $-30\text{ mA}$  to  $+5.0\text{ mA}$ 

Voltage Applied to Output

in HIGH State (with  $V_{\text{CC}} = 0\text{V}$ )

Standard Output

 $-0.5\text{V}$  to  $V_{\text{CC}}$ 

TRI-STATE® Output

 $-0.5\text{V}$  to  $+5.5\text{V}$ 

Current Applied to Output

in LOW State (Max)

twice the rated  $I_{\text{OL}}$  (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	$V_{\text{CC}}$	Conditions
		Min	Typ	Max			
$V_{\text{IH}}$	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
$V_{\text{IL}}$	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
$V_{\text{CD}}$	Input Clamp Diode Voltage			-1.2	V	Min	$I_{\text{IN}} = -18\text{ mA}$
$V_{\text{OH}}$	Output HIGH Voltage	54F 10% $V_{\text{CC}}$	2.5		V	Min	$I_{\text{OH}} = -1\text{ mA}$
		74F 10% $V_{\text{CC}}$	2.5				$I_{\text{OH}} = -1\text{ mA}$
		74F 5% $V_{\text{CC}}$	2.7				$I_{\text{OH}} = -1\text{ mA}$
$V_{\text{OL}}$	Output LOW Voltage	54F 10% $V_{\text{CC}}$		0.5	V	Min	$I_{\text{OL}} = 20\text{ mA}$
		74F 10% $V_{\text{CC}}$		0.5			$I_{\text{OL}} = 20\text{ mA}$
$I_{\text{IH}}$	Input HIGH Current	54F		20.0	$\mu\text{A}$	Max	$V_{\text{IN}} = 2.7\text{V}$
		74F		5.0			
$I_{\text{BVI}}$	Input HIGH Current Breakdown Test	54F		100	$\mu\text{A}$	Max	$V_{\text{IN}} = 7.0\text{V}$
		74F		7.0			
$I_{\text{CEX}}$	Output HIGH Leakage Current	54F		250	$\mu\text{A}$	Max	$V_{\text{OUT}} = V_{\text{CC}}$
		74F		50			
$V_{\text{ID}}$	Input Leakage Test	74F	4.75		V	0.0	$I_{\text{ID}} = 1.9\text{ }\mu\text{A}$ All Other Pins Grounded
$I_{\text{OD}}$	Output Leakage Circuit Current	74F		3.75	$\mu\text{A}$	0.0	$V_{\text{IOD}} = 150\text{ mV}$ All Other Pins Grounded
$I_{\text{IL}}$	Input LOW Current			-0.6	mA	Max	$V_{\text{IN}} = 0.5\text{V}$
$I_{\text{OS}}$	Output Short-Circuit Current	-60		-150	mA	Max	$V_{\text{OUT}} = 0\text{V}$
$I_{\text{CCH}}$	Power Supply Current		106	160	mA	Max	$V_{\text{O}} = \text{HIGH}$
$I_{\text{CCL}}$	Power Supply Current		106	160	mA	Max	$V_{\text{O}} = \text{LOW}$



# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	50	60				40		MHz	2-1
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to Q	9.0 8.0	16.0 12.0	20.5 15.5			8.0 7.0	22.5 17.5	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to Q/2	9.0 10.0	15.5 15.5	20.0 20.0			8.0 9.0	22.0 22.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay XTR to Q	8.5 6.0	12.0 10.5	15.5 13.5			7.5 5.0	17.5 15.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay MR to Q	11.5 9.0	16.5 12.5	21.0 16.0			10.5 8.0	23.0 18.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay MR to Q/2	8.0 7.0	14.0 10.5	17.5 13.5			7.0 6.0	19.5 15.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay M <sub>n</sub> to Q	10.0 10.5	15.0 17.0	19.0 21.5			9.0 9.5	21.0 23.5	ns	2-3

## AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $D_n$ to $\overline{\text{WE}}$	2.0 4.0				2.5 4.5		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $D_n$ to $\overline{\text{WE}}$	0 2.0				0 2.5		ns	2-6
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $D_n$ to CP	9.0 10.5				10.0 12.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $D_n$ to CP	0 0				0 0		ns	2-6
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW XTR to CP	7.0 8.0				8.0 9.0		ns	2-6
$t_h(\text{H})$	Hold Time, HIGH or LOW XTR to CP	0				0		ns	2-6
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW Mode to CP	33.5 33.5				35.5 35.5		ns	2-6
$t_w(\text{H})$	XTR Pulse Width, HIGH	11.5				13.0		ns	2-4
$t_w(\text{L})$	$\overline{\text{MR}}$ Pulse Width, LOW	7.0				8.0		ns	2-4
$t_w(\text{L})$	$\overline{\text{WE}}$ Pulse Width, LOW	4.5				5.0		ns	2-4
$t_w(\text{H})$ $t_w(\text{L})$	CP Pulse Width HIGH or LOW	3.5 9.5				4.0 10.5		ns	2-4
$t_{\text{rec}}$	Recovery Time $\overline{\text{MR}}$ to CP	5.0				6.0		ns	2-6
$t_{\text{rec}}$	Recovery Time Mode to CP	30.0				32.0		ns	2-6



54F/74F533

## Octal Transparent Latch with TRI-STATE® Outputs

### General Description

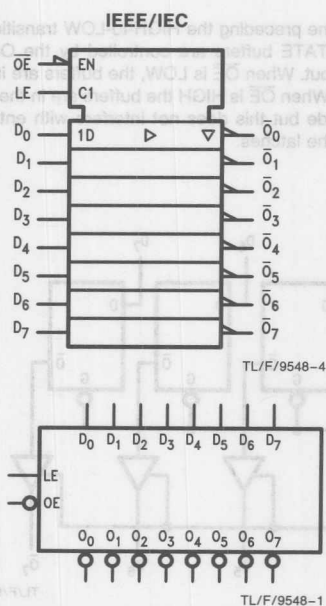
The 'F533 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH the bus output is in the high impedance state. The 'F533 is the same as the 'F373, except that the outputs are inverted.

### Features

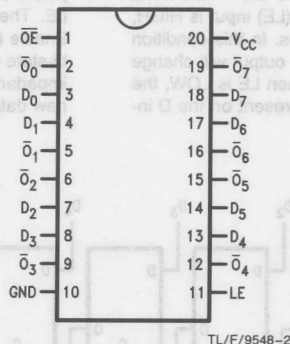
- Eight latches in a single package
- TRI-STATE outputs for bus interfacing
- Inverted version of the 'F373
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

### Logic Symbols

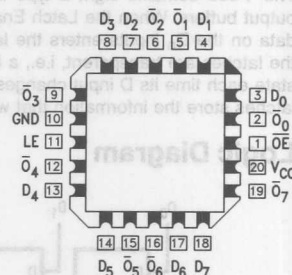


### Pin Assignment for DIP, SOIC and Flatpak



### Connection Diagrams

### Pin Assignment for LCC



# Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$D_0-D_7$	Data Inputs	1.0/1.0	$20\ \mu\text{A}/-0.6\ \text{mA}$
LE	Latch Enable Input (Active HIGH)	1.0/1.0	$20\ \mu\text{A}/-0.6\ \text{mA}$
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/1.0	$20\ \mu\text{A}/-0.6\ \text{mA}$
$\overline{O}_0-\overline{O}_7$	Complementary TRI-STATE Outputs	150/40 (33.3)	$-3\ \text{mA}/24\ \text{mA}$ (20 mA)

Function Table

Inputs			Output
LE	$\overline{OE}$	D	$\overline{O}$
H	L	H	L
H	L	L	H
L	L	X	$\overline{O}_0$
X	H	X	Z

H = HIGH Voltage Level

L = LOW Voltage Level

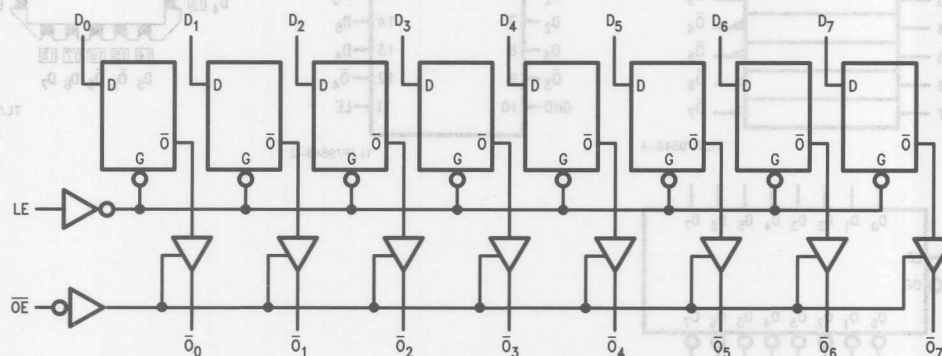
X = Immaterial

## Functional Description

The 'F533 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D in-

puts a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the buffers are in the bi-state mode. When  $\overline{OE}$  is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

## Logic Diagram



TL/F/9548-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
---	----------------

Input Voltage (Note 2)	−0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	−30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

ESD Last Passing Voltage (Min)	4000V
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**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)	54F		1.0	mA	Max	V <sub>IN</sub> = 5.5V
		74F		0.5			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCZ</sub>	Power Supply Current		41	61	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	4.0	6.7	9.0	4.0	12.0	4.0	10.0	ns	2-3
t <sub>PHL</sub>	D <sub>n</sub> to $\bar{O}_n$	2.5	4.4	7.0	2.5	9.0	2.5	8.0		
t <sub>PLH</sub>	Propagation Delay	5.0	7.1	11.0	5.0	14.0	5.0	13.0	ns	2-3
t <sub>PHL</sub>	LE to $\bar{O}_n$	3.0	4.7	7.0	3.0	9.0	3.0	8.0		
t <sub>PZH</sub>	Output Enable Time	2.0	5.9	10.0	2.0	12.5	2.0	11.0	ns	2-5
t <sub>PZL</sub>		2.0	5.6	7.5	2.0	10.5	2.0	8.5		
t <sub>PHZ</sub>	Output Disable Time	1.5	3.4	6.5	1.5	8.5	1.5	7.0	ns	2-5
t <sub>PLZ</sub>		1.5	2.7	5.5	1.5	7.5	1.5	6.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> , V <sub>CC</sub> = Mil		T <sub>A</sub> , V <sub>CC</sub> = Com			
		Min	Max	Min	Max	Min	Max		
t <sub>s</sub> (H)	Setup Time, HIGH or LOW D <sub>n</sub> to LE	2.0		2.0		2.0		ns	2-6
t <sub>s</sub> (L)		2.0		2.0		2.0			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW D <sub>n</sub> to LE	3.0		3.0		3.0		ns	2-6
t <sub>h</sub> (L)		3.0		3.0		3.0			
t <sub>w</sub> (H)	LE Pulse Width, HIGH	6.0		6.0		6.0		ns	2-4

# 54F/74F534

## Octal D-Type Flip-Flop with TRI-STATE® Outputs

### General Description

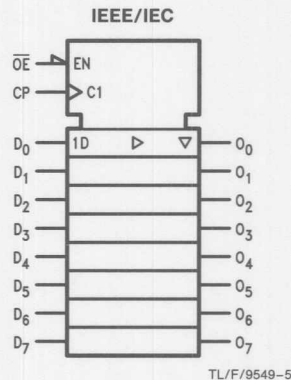
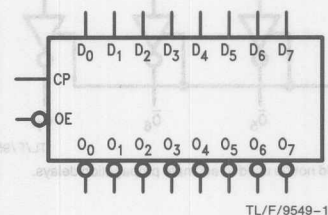
The 'F534 is a high speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ( $\overline{OE}$ ) are common to all flip-flops. The 'F534 is the same as the 'F374 except that the outputs are inverted.

### Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Guaranteed 4000V minimum ESD protection

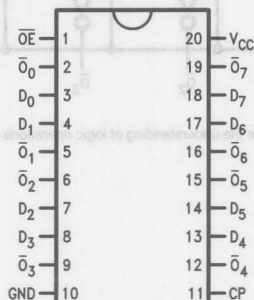
### Ordering Code: See Section 5

### Logic Symbols

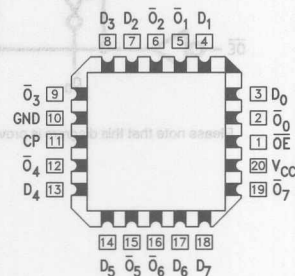


### Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



Pin Assignment for LCC



### Unit Loading/Fan Out: See Section 2 for U.L. Definitions



Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$D_0$ - $D_7$	Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{O}_0$ - $\overline{O}_7$	Complementary TRI-STATE Outputs	150/40(33.3)	-3 mA/24 mA (20 mA)



## Functional Description

The 'F534 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

Function Table

Inputs			Output
CP	OE	D	$\overline{O}$
	L	H	L
	L	L	H
L	L	X	$\overline{O}_0$
X	H	X	Z

H = HIGH Voltage Level

L = LOW Voltage Level

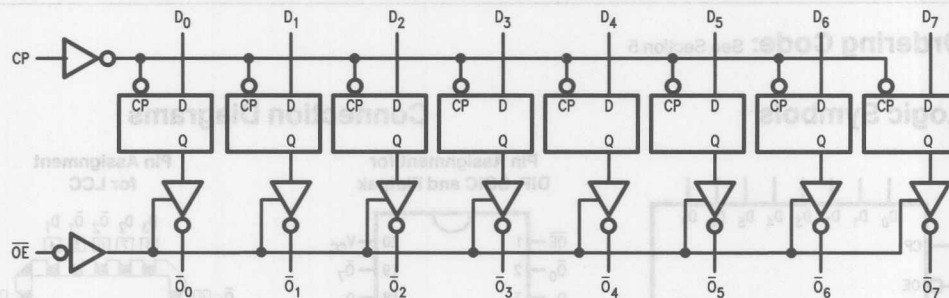
X = Immaterial

 = LOW-to-HIGH Clock Transition

Z = High Impedance

$\overline{O}_0$  = Value stored from previous clock cycle

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
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Input Voltage (Note 2)	−0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	−30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
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Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
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ESD Last Passing Voltage (Min)	4000V
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**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.4 2.5 2.4 2.7 2.7			V	Min	I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>			0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F			20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F			100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F			250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F			3.75	μA	0.0	V <sub>IOD</sub> = 1.50 μA All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current				−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current				50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current				−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60		−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test				500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCZ</sub>	Power Supply Current			55	86	mA	Max	V <sub>O</sub> = HIGH Z

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	100			60		70		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	4.0	6.5	8.5	4.0	10.5	4.0	10.0	ns	2-3
$t_{\text{PHL}}$	CP to $\bar{O}_n$	4.0	6.5	8.5	4.0	11.0	4.0	10.0		
$t_{\text{PZH}}$	Output Enable Time	2.0	9.0	11.5	2.0	14.0	2.0	12.5	ns	2-5
$t_{\text{PZL}}$		2.0	5.8	7.5	2.0	10.0	2.0	8.5		
$t_{\text{PHZ}}$	Output Disable Time	1.5	5.3	7.0	1.5	8.0	1.5	8.0		
$t_{\text{PLZ}}$		1.5	4.3	5.5	1.5	7.5	1.5	6.5		

# AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	2.0		2.0		2.0		ns	2-6
$t_s(\text{L})$	$D_n$ to CP	2.0		2.5		2.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0		2.0		2.0			
$t_h(\text{L})$	$D_n$ to CP	2.0		2.5		2.0		ns	2-4
$t_w(\text{H})$	CP Pulse Width	7.0		7.0		7.0			
$t_w(\text{L})$	HIGH or LOW	6.0		6.0		6.0			

$V_{OH}$	Output HIGH Voltage	Min	V	2.7		2.7			
$V_{OL}$	Output LOW Voltage	Min	V	0.5		0.5			
$I_{IH}$	Input HIGH Current	Max	$\mu\text{A}$	20.0		20.0			
$I_{IL}$	Input LOW Current	Max	$\mu\text{A}$	100		100			
$I_{OZ}$	Output HIGH Leakage Current	Max	$\mu\text{A}$	250		250			
$V_{IP}$	Input Leakage Test	0.0	V	4.75		4.75			
$I_{OP}$	Output Leakage Current	0.0	$\mu\text{A}$	3.75		3.75			
$I_{IL}$	Input LOW Current	Max	$\mu\text{A}$	80		80			
$I_{OZ}$	Output Leakage Current	Max	$\mu\text{A}$	50		50			
$I_{OS}$	Output Short-Circuit Current	Max	$\text{mA}$	150		150			
$I_{ZZ}$	Bus Drainage Test	0.0V	$\mu\text{A}$	500		500			
$I_{OZ}$	Power Supply Current	Max	$\text{mA}$	85		85			

# 54F/74F537

## 1-of-10 Decoder with TRI-STATE® Outputs

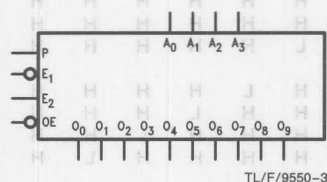
### General Description

The 'F537 is one-of-ten decoder/demultiplexer with four active HIGH BCD inputs and ten mutually exclusive outputs. A polarity control input determines whether the outputs are active LOW or active HIGH. The 'F537 has TRI-STATE outputs, and a HIGH signal on the Output Enable ( $\overline{OE}$ ) input forces all outputs to the high impedance state. Two input

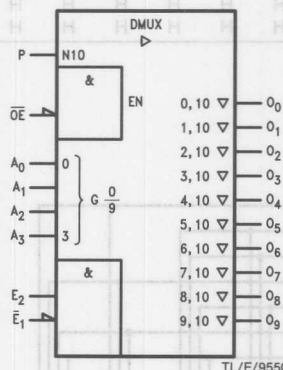
enables, active HIGH  $E_2$  and active LOW  $\overline{E}_1$ , are available for demultiplexing data to the selected output in either non-inverted or inverted form. Input codes greater than BCD nine cause all outputs to go to the inactive state (i.e., same polarity as the P input).

**Ordering Code:** See Section 5

### Logic Symbols

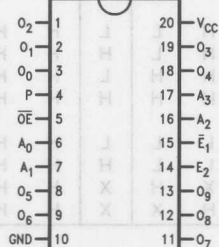


IEEE/IEC



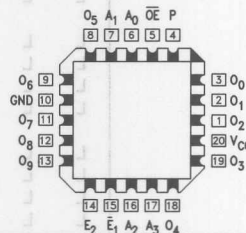
### Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak



TL/F/9550-1

Pin Assignment  
for LCC



TL/F/9550-2

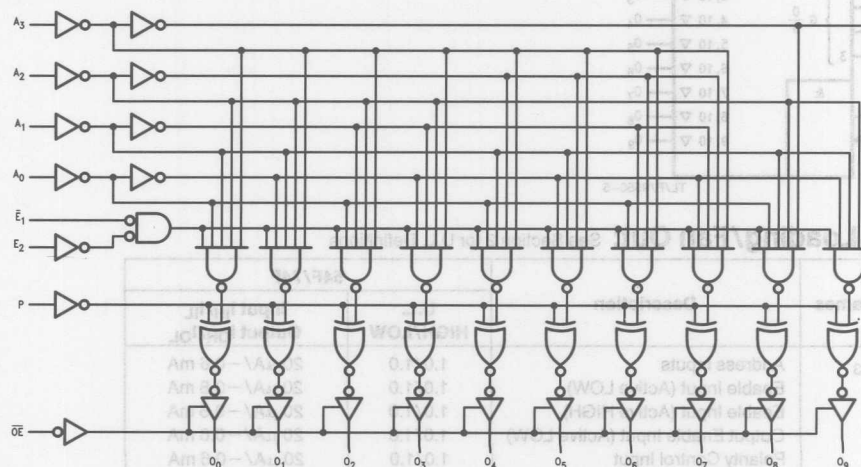
**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_0-A_3$	Address Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{E}_1$	Enable Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$E_2$	Enable Input (Active HIGH)	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
P	Polarity Control Input	1.0/1.0	20 $\mu A$ / -0.6 mA
$O_0-O_9$	TRI-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

	OE	E <sub>1</sub>	E <sub>2</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	O <sub>0</sub>	O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>	O <sub>4</sub>	O <sub>5</sub>	O <sub>6</sub>	O <sub>7</sub>	O <sub>8</sub>	O <sub>9</sub>
High Impedance	H	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	H	X	X	X	X	X	Outputs Equal P Input									
Active HIGH Output (P = L)	L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L
	L	L	H	L	L	L	H	L	H	L	L	L	L	L	L	L	L
	L	L	H	L	L	L	H	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	L	H	H	L	L	H	L	L	L	L	L	L	L
Active LOW Output (P = H)	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	L	L	H	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	L	H	H	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	L	H	H	L	L	L	L	L	L	L	L	L	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
---	----------------

Input Voltage (Note 2)	−0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	−30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
---	--

Standard Output	−0.5V to V <sub>CC</sub>
-----------------	--------------------------

TRI-STATE Output	−0.5V to +5.5V
------------------	----------------

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military −55°C to +125°C

Commercial 0°C to +70°C

Supply Voltage

Military +4.5V to +5.5V

Commercial +4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.4 2.5 2.4 2.7 2.7			V	Min	I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>			0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F			20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F			100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F			250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current				−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current				50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current				−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60		−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test				500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current				56	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCZ</sub>	Power Supply Current			44	66	mA	Max	V <sub>O</sub> = HIGH Z



# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	6.0	11.0	16.0			6.0	17.0	ns	2-3
$t_{PHL}$	$A_n$ to $O_n$	4.0	7.5	11.0			4.0	12.0		
$t_{PLH}$	Propagation Delay	5.0	8.5	14.5			5.0	15.5	ns	2-3
$t_{PHL}$	$\bar{E}_1$ to $O_n$	4.0	6.5	9.0			4.0	10.0		
$t_{PLH}$	Propagation Delay	6.0	11.0	16.0			6.0	17.0	ns	2-3
$t_{PHL}$	$E_2$ to $O_n$	5.0	10.0	14.0			5.0	15.0		
$t_{PLH}$	Propagation Delay	6.0	11.5	18.0			6.0	20.0	ns	2-5
$t_{PHL}$	P to $O_n$	6.0	11.0	16.0			6.0	17.0		
$t_{PZH}$	Output Enable Time	3.0	5.5	10.5			3.0	11.5	ns	2-5
$t_{PZL}$	$\overline{OE}$ to $O_n$	5.0	9.0	13.0			5.0	14.0		
$t_{PHZ}$	Output Disable Time	2.0	4.0	6.0			2.0	7.0	ns	2-5
$t_{PLZ}$	$\overline{OE}$ to $O_n$	3.0	5.0	7.0			3.0	8.0		

Symbol	Parameter	74F74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage	0.8			V		Recognized as a LOW Signal
V <sub>IO</sub>	Input Clamp Diode Voltage	-1.2			V	Min	I <sub>IH</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7			V	Min	I <sub>OH</sub> = -1 mA
		2.7					I <sub>OH</sub> = -3 mA
		2.7					I <sub>OH</sub> = -1 mA
		2.7					I <sub>OH</sub> = -3 mA
		2.7					I <sub>OH</sub> = -1 mA
		2.7					I <sub>OH</sub> = -3 mA
V <sub>OL</sub>	Output LOW Voltage	0.5			V	Min	I <sub>OL</sub> = 20 mA
		0.5					I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	2.0			μA	Max	V <sub>IH</sub> = 2.7V
		2.0					
I <sub>IHL</sub>	Input HIGH Current Breakdown Test	100			μA	Max	V <sub>IH</sub> = 7.0V
		100					
I <sub>OZH</sub>	Output HIGH Leakage Current	250			μA	Max	V <sub>OH</sub> = V <sub>CC</sub>
		250					
V <sub>IO</sub>	Input Leakage Test	4.75			V	0.0	I <sub>IO</sub> = 1.9 μA All Other Pins Grounded
I <sub>OOL</sub>	Output Leakage Circuit Current	2.75			μA	0.0	V <sub>OD</sub> = 180 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current	-0.8			mA	Max	V <sub>IH</sub> = 0.8V
I <sub>OZH</sub>	Output Leakage Current	80			μA	Max	V <sub>OH</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current	-80			μA	Max	V <sub>OH</sub> = 0.8V
I <sub>OS</sub>	Output Short-Circuit Current	-80			mA	Max	V <sub>OH</sub> = 0V
I <sub>DS</sub>	Bus Discharge Test	800			μA	0.0V	V <sub>OH</sub> = 2.58V
I <sub>OCH</sub>	Power Supply Current	88			mA	Max	V <sub>O</sub> = HIGH
I <sub>OCL</sub>	Power Supply Current	88	44		mA	Max	V <sub>O</sub> = HIGH

# 54F/74F538

## 1-of-8 Decoder with TRI-STATE® Outputs

### General Description

The 'F538 decoder/demultiplexer accepts three Address ( $A_0$ – $A_2$ ) input signals and decodes them to select one of eight mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active LOW or active HIGH. A HIGH Signal on either of the active LOW Output Enable ( $\overline{OE}$ ) inputs forces all outputs to the high impedance state. Two active HIGH and two active LOW input enables are available for easy expansion to 1-of 32 decoding with

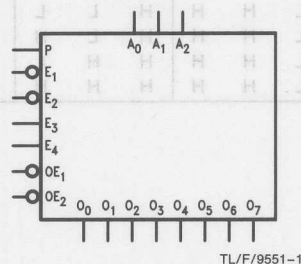
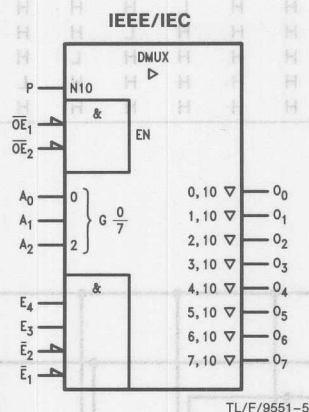
four packages, or for data demultiplexing to 1-of-8 or 1-of-16 destinations.

### Features

- Output polarity control
- Data demultiplexing capability
- Multiple enables for expansion
- TRI-STATE outputs

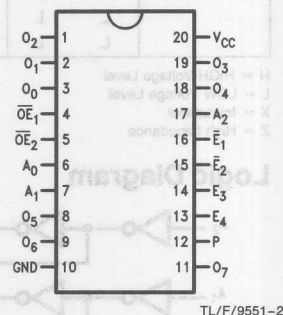
**Ordering Code:** See Section 5

### Logic Symbols

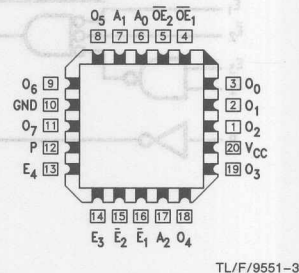


### Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



Pin Assignment for LCC



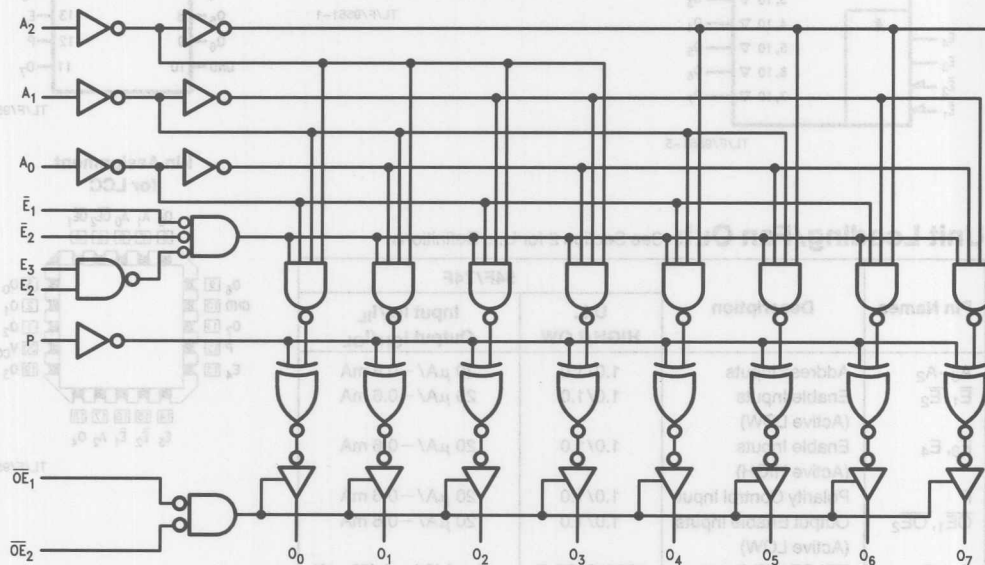
**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_0$ – $A_2$	Address Inputs	1.0/1.0	20 $\mu$ A/–0.6 mA
$\overline{E}_1, \overline{E}_2$	Enable Inputs (Active LOW)	1.0/1.0	20 $\mu$ A/–0.6 mA
$E_3, E_4$	Enable Inputs (Active HIGH)	1.0/1.0	20 $\mu$ A/–0.6 mA
P	Polarity Control Input	1.0/1.0	20 $\mu$ A/–0.6 mA
$\overline{OE}_1, \overline{OE}_2$	Output Enable Inputs (Active LOW)	1.0/1.0	20 $\mu$ A/–0.6 mA
$O_0$ – $O_7$	TRI-STATE Outputs	150/40 (33.3)	–3 mA/24 mA (20 mA)

	-1	-2	-1	-2	-3	-4	-2	-1	-0	0	1	2	3	4	5	6	7
High Impedance	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	L	H	X	X	X	X	X	X	Outputs Equal P Input							
Active HIGH Output (P = L)	L	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L	L
Active LOW Output (P = H)	L	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

TL/F/9551-4

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	−55°C to +125°C
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current		31	45	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		37	56	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		37	56	mA	Max	V <sub>O</sub> = HIGH Z

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	6.0	11.0	16.0			6.0	17.0		
$t_{PHL}$	$A_n$ to $O_n$	4.0	7.5	11.0			4.0	12.0	ns	2-3
$t_{PLH}$	Propagation Delay	5.0	8.5	15.0			5.0	16.0		
$t_{PHL}$	$E_1$ or $E_2$ to $O_n$	4.0	6.5	9.0			4.0	10.0		
$t_{PLH}$	Propagation Delay	6.0	11.0	16.0			6.0	17.0		
$t_{PHL}$	$E_3$ or $E_4$ to $O_n$	5.0	10.0	14.0			5.0	15.0	ns	2-3
$t_{PLH}$	Propagation Delay	6.0	11.5	18.0			6.0	20.0		
$t_{PHL}$	$P$ to $O_n$	6.0	11.0	16.0			6.0	17.0		
$t_{PZH}$	Output Enable Time	3.0	5.5	10.0			3.0	11.0		
$t_{PZL}$	$\overline{OE}_1$ or $\overline{OE}_2$ to $O_n$	5.0	9.0	13.0			5.0	14.0	ns	2-5
$t_{PHZ}$	Output Disable Time	2.0	4.0	6.0			2.0	7.0		
$t_{PLZ}$	$\overline{OE}_1$ or $\overline{OE}_2$ to $O_n$	3.0	5.0	8.0			3.0	9.0		

Symbol	Parameter	Units	Min	Typ	Max	Conditions
$V_{IH}$	Input HIGH Voltage	V	2.0			Recognized as a HIGH signal
$V_{IL}$	Input LOW Voltage	V	0.8			Recognized as a LOW signal
$V_{OD}$	Input Clamp Diode Voltage	V	-1.2			$I_{in} = -18\text{ mA}$
$V_{OH}$	Output HIGH Voltage	V				$I_{OH} = -1\text{ mA}$ $I_{OH} = -3\text{ mA}$ $I_{OH} = -1\text{ mA}$ $I_{OH} = -3\text{ mA}$ $I_{OH} = -1\text{ mA}$ $I_{OH} = -3\text{ mA}$
$V_{OL}$	Output LOW Voltage	V				$I_{OL} = 20\text{ mA}$ $I_{OL} = 20\text{ mA}$
$I_{IH}$	Input HIGH Current	$\mu\text{A}$	20.0			$V_{IH} = 2.7\text{V}$
$I_{BI}$	Input HIGH Current Breakdown Test	$\mu\text{A}$	100			$V_{IH} = 7.0\text{V}$
$I_{OZH}$	Output HIGH Leakage Current	$\mu\text{A}$	250			$V_{OH} = V_{CC}$
$V_{IO}$	Input Leakage Test	V				$I_D = 1.8\text{ }\mu\text{A}$ All Other Pins Grounded
$I_{OO}$	Output Leakage Current	$\mu\text{A}$	2.5			$V_{OD} = 150\text{ mV}$ All Other Pins Grounded
$I_{IL}$	Input LOW Current	$\text{mA}$	-0.8			$V_{IL} = 0.5\text{V}$
$I_{OZH}$	Output Leakage Current	$\mu\text{A}$	50			$V_{OH} = 2.7\text{V}$
$I_{OLZ}$	Output Leakage Current	$\mu\text{A}$	-50			$V_{OL} = 0.5\text{V}$
$I_{OS}$	Output Short-Circuit Current	$\text{mA}$	-150			$V_{OH} = 0\text{V}$
$I_{SZ}$	Bus Discharge Test	$\mu\text{A}$	500			$V_{OH} = 0.5\text{V}$
$I_{OH}$	Power Supply Current	$\text{mA}$	31			$V_O = \text{HIGH}$
$I_{OL}$	Power Supply Current	$\text{mA}$	37			$V_O = \text{LOW}$
$I_{OZ}$	Power Supply Current	$\text{mA}$	37			$V_O = \text{HIGH-Z}$

## 54F/74F539

# Dual 1-of-4 Decoder with TRI-STATE® Outputs

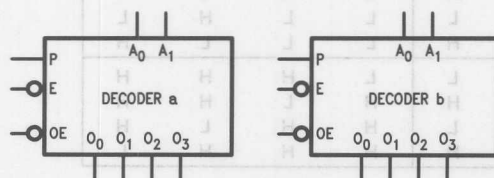
## General Description

The 'F539 contains two independent decoders. Each accepts two Address ( $A_0$ ,  $A_1$ ) input signals and decodes them to select one of four mutually exclusive outputs. A polarity control input ( $P$ ) determines whether the outputs are active HIGH ( $P = L$ ) or active LOW ( $P = H$ ). An active LOW

input Enable ( $\bar{E}$ ) is available for data demultiplexing; data is routed to the selected output in non-inverted form in the active LOW mode or in inverted form in the active HIGH mode. A HIGH signal on the active LOW Output Enable ( $\bar{OE}$ ) input forces the TRI-STATE outputs to the high impedance state.

**Ordering Code:** See Section 5

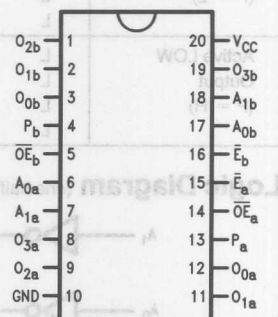
## Logic Symbols



TL/F/9552-1

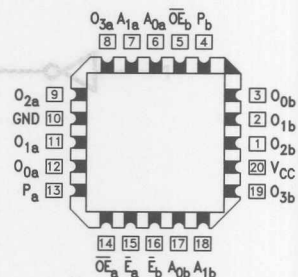
## Connection Diagrams

**Pin Assignment  
for DIP, SOIC and Flatpak**

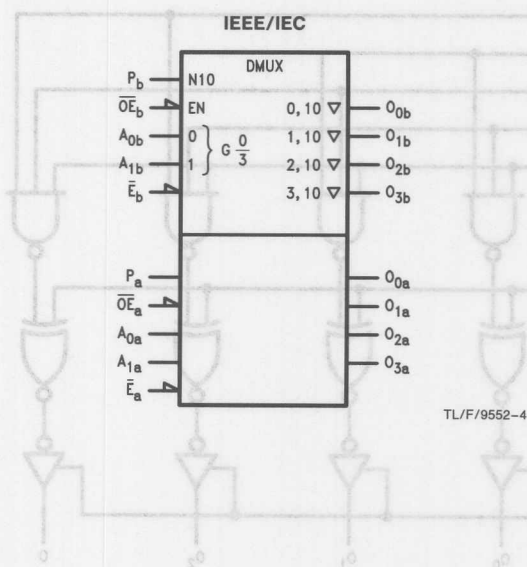


TL/F/9552-2

**Pin Assignment  
for LCC**



TL/F/9552-3



TL/F/9552-4



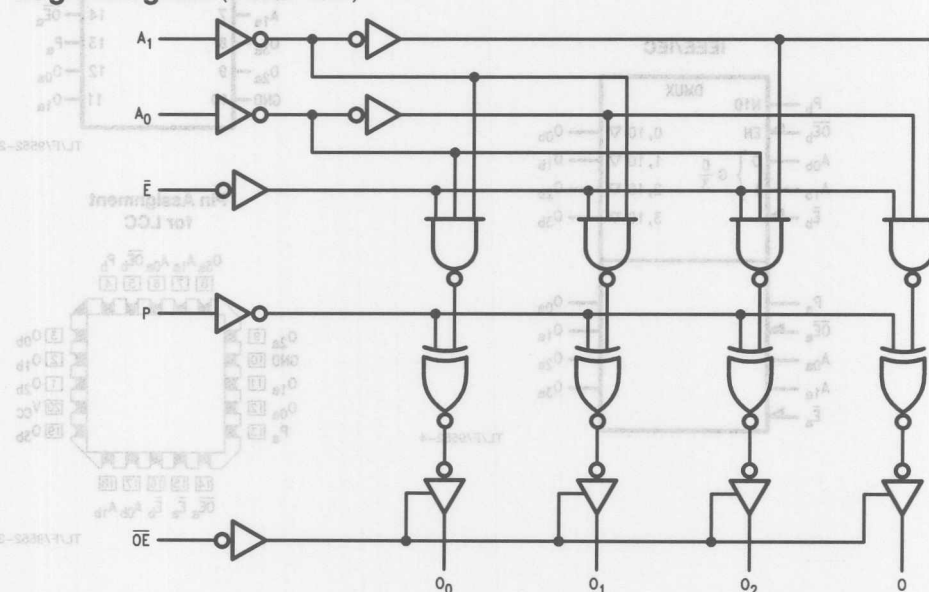
A <sub>0a</sub> -A <sub>1a</sub>	Side A Address Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
A <sub>0b</sub> -A <sub>1b</sub>	Side B Address Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\bar{E}_a, \bar{E}_b$	Enable Inputs (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\bar{OE}_a, \bar{OE}_b$	Output Enable Inputs (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
P <sub>a</sub> , P <sub>b</sub>	Polarity Control Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
O <sub>0a</sub> -O <sub>3a</sub>	Side A TRI-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)
O <sub>0b</sub> -O <sub>3b</sub>	Side B TRI-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

**Truth Table** (each half)

Function	Inputs				Outputs			
	$\bar{OE}$	$\bar{E}$	A <sub>1</sub>	A <sub>0</sub>	O <sub>0</sub>	O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>
High Impedance	H	X	X	X	Z	Z	Z	Z
Disable	L	H	X	X	O <sub>n</sub> = P			
Active HIGH Output (P = L)	L	L	L	L	H	L	L	L
	L	L	L	H	L	H	L	L
	L	L	H	L	L	L	H	L
	L	L	H	H	L	L	L	H
Active LOW Output (P = H)	L	L	L	L	L	H	H	H
	L	L	L	H	H	L	H	H
	L	L	H	L	H	H	L	H
	L	L	H	H	H	H	H	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

**Logic Diagram** (one half shown)



TL/F/9552-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
---	----------------

Input Voltage (Note 2)	−0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	−30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
---	--

Standard Output	−0.5V to V <sub>CC</sub>
-----------------	--------------------------

TRI-STATE Output	−0.5V to +5.5V
------------------	----------------

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military

Commercial

−55°C to +125°C

0°C to +70°C

Supply Voltage

Military

Commercial

+4.5V to +5.5V

+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>ID</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current		28	45	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		40	60	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		40	60	mA	Max	V <sub>O</sub> = HIGH Z

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	4.0	14.5	18.5			3.5	19.5	ns	2-3
t <sub>PHL</sub>	A <sub>n</sub> to O <sub>n</sub>	4.0	9.5	12.0			4.0	13.0		
t <sub>PLH</sub>	Propagation Delay	5.0	12.0	16.0			5.5	17.0	ns	2-3
t <sub>PHL</sub>	E to O <sub>n</sub>	4.0	7.5	9.5			4.0	10.5		
t <sub>PLH</sub>	Propagation Delay	7.5	14.5	21.5			4.5	22.5	ns	2-3
t <sub>PHL</sub>	P to O <sub>n</sub>	5.0	11.0	16.5			4.5	17.5		
t <sub>pZH</sub>	Output Enable Time	4.5	8.0	10.5			4.0	11.5	ns	2-5
t <sub>pZL</sub>	O <sub>E</sub> to O <sub>n</sub>	5.5	10.0	13.0			5.0	14.0		
t <sub>PHZ</sub>	Output Disable Time	2.0	4.5	6.5			2.0	7.0		
t <sub>PLZ</sub>	O <sub>E</sub> to O <sub>n</sub>	3.0	6.5	8.5			3.0	9.5		

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter	74F		Units	V <sub>CC</sub>	Conditions
		Min	Typ			
V <sub>IH</sub>	Input HIGH Voltage	2.0		V		Recognized as a HIGH signal
V <sub>IL</sub>	Input LOW Voltage	0.8		V		Recognized as a LOW signal
V <sub>CC</sub>	Input Clamp Diode Voltage	-1.5		V	Min	I <sub>IN</sub> = -10 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	2.7	V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA
V <sub>OL</sub>	Output LOW Voltage	0.2	0.2	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	24	20.0	μA	Max	V <sub>IH</sub> = 2.7V
I <sub>IL</sub>	Input LOW Current	24	100	μA	Max	V <sub>IH</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	24	280	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	24	4.75	V	0.0	I <sub>ID</sub> = 1.0 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	24	3.75	μA	0.0	V <sub>OD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current		-0.8	μA	Max	V <sub>IH</sub> = 0.5V
I <sub>OH</sub>	Output Leakage Current		80	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OL</sub>	Output Leakage Current		-50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test		500	μA	0.0V	V <sub>OUT</sub> = 2.5V
I <sub>CC</sub>	Power Supply Current	28	48	mA	Max	V <sub>O</sub> = HIGH
I <sub>CC</sub>	Power Supply Current	40	80	mA	Max	V <sub>O</sub> = LOW
I <sub>CC</sub>	Power Supply Current	40	80	mA	Max	V <sub>O</sub> = HIGH $\Sigma$



## 54F/74F540 • 54F/74F541 Octal Buffer/Line Driver with TRI-STATE® Outputs

### General Description

The 'F540 and 'F541 are similar in function to the 'F240 and 'F244 respectively, except that the inputs and outputs are on opposite sides of the package (see Connection Diagrams). This pinout arrangement makes these devices especially useful as output ports for microprocessors, allowing ease of layout and greater PC board density.

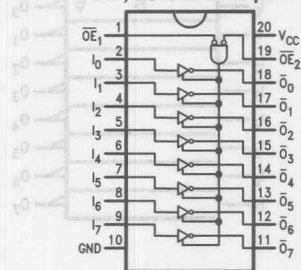
### Features

- TRI-STATE outputs drive bus lines
- Inputs and outputs opposite side of package, allowing easier interface to microprocessors

**Ordering Code:** See Section 5

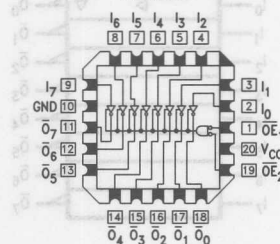
### Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak

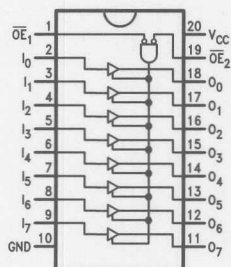


TL/F/9553-1

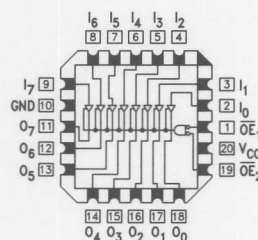
Pin Assignment  
for LCC



TL/F/9553-2



TL/F/9553-4



TL/F/9553-5

**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{OE}_1, \overline{OE}_2$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$I_n$	Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$O_n, \overline{O}_n$	Outputs	600/106.6 (80)	-12 mA/64 mA (48 mA)

Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	I	'F540	'F541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

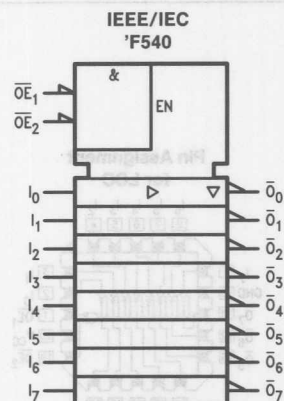
H = HIGH Voltage Level

L = LOW Voltage Level

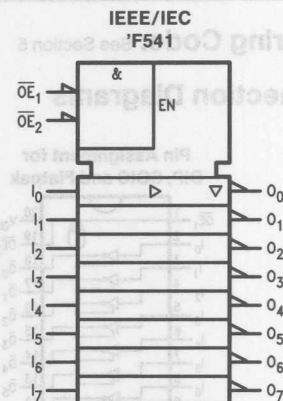
X = Immaterial

Z = High Impedance

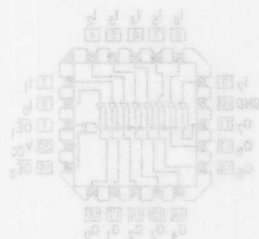
## Logic Diagrams



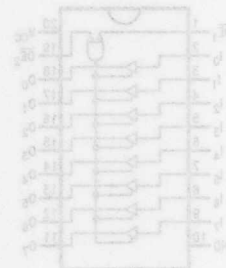
TL/F/9553-3



TL/F/9553-6



TL/F/9553-3



TL/F/9553-6

Pin Name	Description	U.I.	54F174F
$\overline{OE}_1, \overline{OE}_2$	TRI-STATE Output Enable Input (Active LOW)	HIGH/LOW	Input 14/15 Output 10/11
$I_n$	Inputs	1.0/1.0	20 mA/-0.8 mA
$O_n$	Outputs	1.0/1.0	20 mA/-0.8 mA
		600/100 (80)	-15 mA/18 mA (48 mA)

Unit Loading/Fan Out: See Section 2 for U.I. Definitions

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA

Voltage Applied to Output  
in HIGH State (with V<sub>CC</sub> = 0V)  
Standard Output

–0.5V to V<sub>CC</sub>

TRI-STATE Output

–0.5V to +5.5V

Current Applied to Output  
in LOW State (Max)

twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military –55°C to +125°C

Commercial 0°C to +70°C

Supply Voltage

Military +4.5V to +5.5V

Commercial +4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			–1.2	V	Min	I <sub>IN</sub> = –18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.4			Min	I <sub>OH</sub> = –3 mA
		54F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = –12 mA
		74F 10% V <sub>CC</sub>	2.4		V		I <sub>OH</sub> = –3 mA
		74F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = –15 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = –3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.55	V	Min	I <sub>OL</sub> = 48 mA
		74F 10% V <sub>CC</sub>		0.55			I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			–0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			–50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		–100	–225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V



**DC Electrical Characteristics** (Continued)

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
I <sub>CCH</sub>	Power Supply Current ('F540)		11	20	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current ('F540)		53	75	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current ('F540)		31	45	mA	Max	V <sub>O</sub> = HIGH Z
I <sub>CCH</sub>	Power Supply Current ('F541)		26	35	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current ('F541)		55	75	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current ('F541)		31	55	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	1.5	3.0	5.0	1.0	6.0	1.0	5.5	ns	2-3
t <sub>PHL</sub>	Data to Output ('F540)	1.0	2.0	4.0	1.0	4.5	1.0	4.0		
t <sub>PZH</sub>	Output Enable Time ('F540)	2.5	4.9	8.0	2.5	9.0	2.5	8.5	ns	2-5
t <sub>PZL</sub>		3.5	5.8	10.0	3.5	11.0	3.5	10.5		
t <sub>PHZ</sub>	Output Disable Time ('F540)	1.5	3.4	6.0	1.5	7.0	1.5	6.5	ns	2-3
t <sub>PLZ</sub>		1.0	2.5	5.5	1.0	7.5	1.0	6.0		
t <sub>PLH</sub>	Propagation Delay	1.5	3.3	5.5			1.5	6.0	ns	2-3
t <sub>PHL</sub>	Data to Output ('F541)	1.5	2.7	5.5			1.5	6.0		
t <sub>PZH</sub>	Output Enable Time ('F541)	3.0	5.8	8.0			2.5	9.5	ns	2-5
t <sub>PZL</sub>		3.5	6.1	8.5			3.0	9.5		
t <sub>PHZ</sub>	Output Disable Time ('F541)	1.5	3.4	6.0			1.5	6.5	ns	2-5
t <sub>PLZ</sub>		1.5	2.9	5.5			1.5	6.0		



## 54F/74F543 Octal Registered Transceiver

### General Description

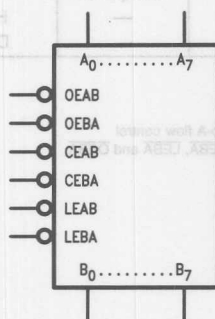
The 'F543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The A outputs are guaranteed to sink 24 mA (20 mA Mil) while the B outputs are rated for 64 mA (48 mA Mil).

### Features

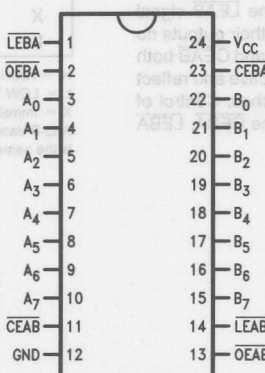
- 8-bit octal transceiver
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- A outputs sink 24 mA (20 mA Mil)
- B outputs sink 64 mA (48 mA Mil)
- 300 mil slim package

**Ordering Code:** See Section 5

### Logic Symbols

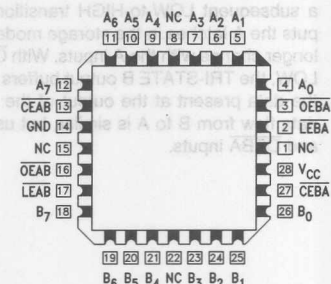


Pin Assignment for  
DIP, SOIC and Flatpak



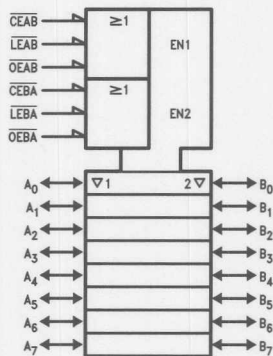
TL/F/9554-2

Pin Assignment  
for LCC



TL/F/9554-3

### IEEE/IEC



TL/F/9554-5

# Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)	1.0/2.0	20 $\mu A$ / -1.2 mA
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)	1.0/2.0	20 $\mu A$ / -1.2 mA
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$A_0-A_7$	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs	3.5/1.083	70 $\mu A$ / -650 $\mu A$ -3 mA/24 mA (20 mA)
$B_0-B_7$	B-to-A Data Inputs or A-to-B TRI-STATE Outputs	3.5/1.083	70 $\mu A$ / -650 $\mu A$ -12 mA/64 mA (48 mA)
		600/106.6 (80)	

## Functional Description

The 'F543 contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ( $\overline{CEAB}$ ) input must be LOW in order to enter data from  $A_0-A_7$  or take data from  $B_0-B_7$ , as indicated in the Data I/O Control Table. With  $\overline{CEAB}$  LOW, a LOW signal on the A-to-B Latch Enable ( $\overline{LEAB}$ ) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the  $\overline{LEAB}$  signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With  $\overline{CEAB}$  and  $\overline{OEAB}$  both LOW, the TRI-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the  $\overline{CEBA}$ ,  $\overline{LEBA}$  and  $\overline{OEBA}$  inputs.

Data I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = HIGH Voltage Level

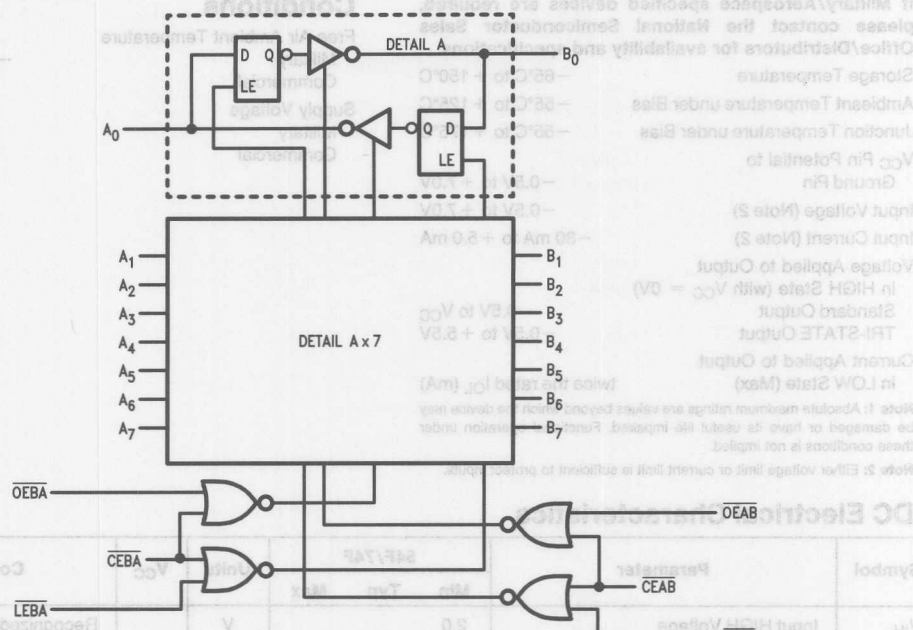
L = LOW Voltage Level

X = Immaterial

A-to-B data flow shown; B-to-A flow control is the same, except using  $\overline{CEBA}$ ,  $\overline{LEBA}$  and  $\overline{OEBA}$

## Logic Diagram

$-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
 $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$   
 $+4.5\text{V}$  to  $+5.5\text{V}$   
 $+4.5\text{V}$  to  $+5.5\text{V}$



Symbol	Parameter	Min	Typ	Max	Conditions
$V_{IH}$	Input HIGH Voltage	2.0			Recognized as a HIGH signal
$V_{IL}$	Input LOW Voltage	0.8			Recognized as a LOW signal
$V_{DD}$	Input Clamp Diode Voltage	-1.5			$I_{IN} = -18\text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.7	2.8	2.9	$I_{OH} = -1\text{ mA (A}_n\text{)}$ $I_{OH} = -3\text{ mA (A}_n\text{, B}_n\text{)}$ $I_{OH} = -12\text{ mA (B}_n\text{)}$ $I_{OH} = -1\text{ mA (A}_n\text{)}$ $I_{OH} = -3\text{ mA (A}_n\text{, B}_n\text{)}$ $I_{OH} = -12\text{ mA (B}_n\text{)}$ $I_{OH} = -1\text{ mA (A}_n\text{)}$ $I_{OH} = -3\text{ mA (A}_n\text{, B}_n\text{)}$ $I_{OH} = -12\text{ mA (B}_n\text{)}$
$V_{OL}$	Output LOW Voltage	0.25	0.3	0.4	$I_{OL} = 20\text{ mA (A}_n\text{)}$ $I_{OL} = 48\text{ mA (B}_n\text{)}$ $I_{OL} = 24\text{ mA (A}_n\text{)}$ $I_{OL} = 84\text{ mA (B}_n\text{)}$
$I_{IH}$	Input HIGH Current	25	50	75	$V_{IN} = 2.7\text{V}$
$I_{BI}$	Input HIGH Current Breakdown Test	25	100	150	$V_{IN} = 7.0\text{V}$ (OEAB, OEBA, CEAB, LEBA, CEBA, CEBA)
$I_{OVI}$	Input HIGH Current Breakdown (V <sub>O</sub> )	25	10	15	$V_{IN} = 5.5\text{V (A}_n\text{, B}_n\text{)}$
$I_{OEX}$	Output HIGH Leakage Current	25	250	50	$V_{OUT} = V_{CC}$
$V_{IO}$	Input Leakage Test	25	4.75		$I_{IP} = 1.8\text{ mA}$ All Other Pins Grounded
$I_{OCC}$	Output Leakage Circuit Current	25	3.75		$V_{I/O} = 150\text{ mV}$ All Other Pins Grounded

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	-0.5V to V <sub>CC</sub>
Standard Output	-0.5V to +5.5V
TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	-55°C to +125°C
Military	0°C to +70°C
Commercial	
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	

## DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5			V	Min	I <sub>OH</sub> = -1 mA (A <sub>n</sub> )
		54F 10% V <sub>CC</sub>	2.4					I <sub>OH</sub> = -3 mA (A <sub>n</sub> , B <sub>n</sub> )
		54F 10% V <sub>CC</sub>	2.0					I <sub>OH</sub> = -12 mA (B <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.5					I <sub>OH</sub> = -1 mA (A <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.4					I <sub>OH</sub> = -3 mA (A <sub>n</sub> , B <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.0					I <sub>OH</sub> = -12 mA (B <sub>n</sub> )
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = -1 mA (A <sub>n</sub> )
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = -3 mA (A <sub>n</sub> , B <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>			0.5	V	Min	I <sub>OL</sub> = 20 mA (A <sub>n</sub> )
		54F 10% V <sub>CC</sub>			0.55			I <sub>OL</sub> = 48 mA (B <sub>n</sub> )
		74F 10% V <sub>CC</sub>			0.5			I <sub>OL</sub> = 24 mA (A <sub>n</sub> )
		74F 10% V <sub>CC</sub>			0.55			I <sub>OL</sub> = 64 mA (B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current	54F			20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F			5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F			100	μA	Max	V <sub>IN</sub> = 7.0V (OEAB, OEBA, LEAB, LEBA, CEAB, CEBA)
		74F			7.0			
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)	54F			1.0	mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
		74F			0.5			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F			50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded

**DC Electrical Characteristics** (Continued)

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
I <sub>IL</sub>	Input LOW Current			-0.6 -1.2	mA	Max	V <sub>IN</sub> = 0.5V (OEAB, OEBA) V <sub>IN</sub> = 0.5V (CEAB, CEBA)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			-650	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current	-60 -100		-150 -225	mA	Max	V <sub>OUT</sub> = 0V (A <sub>n</sub> ) V <sub>OUT</sub> = 0V (B <sub>n</sub> )
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CCH</sub>	Power Supply Current		67	100	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		83	125	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		83	125	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Transparent Mode A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	3.0 3.0	5.5 5.0	7.5 6.5			3.0 3.0	8.5 7.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEBA to A <sub>n</sub>	4.5 4.5	8.5 8.5	11.0 11.0			4.5 4.5	12.5 12.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEAB to B <sub>n</sub>	4.5 4.5	8.5 8.5	11.0 11.0			4.5 4.5	12.5 12.5	ns	2-3
t <sub>pZH</sub> t <sub>pZL</sub>	Output Enable Time OEBA or OEAB to A <sub>n</sub> or B <sub>n</sub> CEBA or CEAB to A <sub>n</sub> or B <sub>n</sub>	3.0 4.0	7.0 7.5	9.0 10.5			3.0 4.0	10.0 12.0	ns	2-5
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OEBA or OEAB to A <sub>n</sub> or B <sub>n</sub> CEBA or CEAB to A <sub>n</sub> or B <sub>n</sub>	1.0 2.5	6.0 5.5	8.0 10.5			1.0 2.5	9.0 11.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> , V <sub>CC</sub> = Mil		T <sub>A</sub> , V <sub>CC</sub> = Com			
		Min	Max	Min	Max	Min	Max		
t <sub>s</sub> (H)	Setup Time, HIGH or LOW	3.0				3.5		ns	2-6
t <sub>s</sub> (L)	A <sub>n</sub> or B <sub>n</sub> to $\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$	3.0				3.5			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	3.0				3.5			
t <sub>h</sub> (L)	A <sub>n</sub> or B <sub>n</sub> to $\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$	3.0				3.5			
t <sub>w</sub> (L)	Latch Enable, B to A Pulse Width, LOW	8.0				9.0		ns	2-4





## 54F/74F544 Octal Registered Transceiver

### General Description

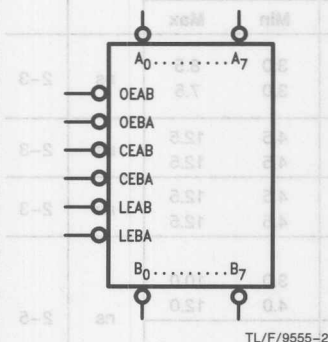
The 'F544 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The A outputs are guaranteed to sink 24 mA (20 mA Mil) while the B outputs are rated for 64 mA (48 mA Mil). The 'F544 inverts data in both directions.

### Features

- 8-bit octal transceiver
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- A outputs sink 24 mA (20 mA Mil), B outputs sink 64 mA (48 mA Mil)
- 300 mil slim PDIP

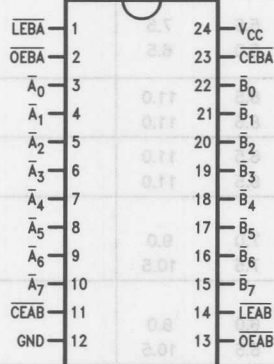
**Ordering Code:** See Section 5

### Logic Symbols

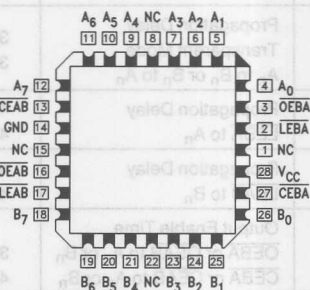


### Connection Diagrams

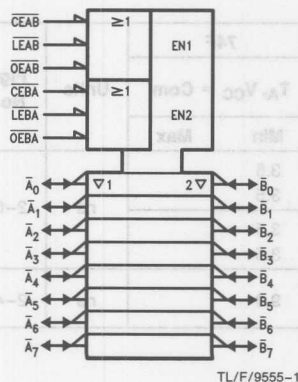
Pin Assignment for  
DIP, SOIC and Flatpak



Pin Assignment  
for LCC



IEEE/IEC



TL/F/9555-3

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)	1.0/2.0	20 $\mu A$ / -1.2 mA
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)	1.0/2.0	20 $\mu A$ / -1.2 mA
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{A_0}-\overline{A_7}$	A-to-B Data Inputs or B-to-A TRI-STATE Outputs	3.5/1.083	70 $\mu A$ / -650 $\mu A$ -3 mA/24 mA (20 mA)
$\overline{B_0}-\overline{B_7}$	B-to-A Data Inputs or A-to-B TRI-STATE Outputs	3.5/1.083	70 $\mu A$ / -650 $\mu A$ -12 mA/64 mA (48 mA)

**Functional Description**

The 'F544 contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ( $\overline{CEAB}$ ) input must be LOW in order to enter data from  $\overline{A_0}-\overline{A_7}$  or take data from  $\overline{B_0}-\overline{B_7}$ , as indicated in the Data I/O Control Table. With  $\overline{CEAB}$  LOW, a LOW signal on the A-to-B Latch Enable ( $\overline{LEAB}$ ) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the  $\overline{LEAB}$  signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With  $\overline{CEAB}$  and  $\overline{OEAB}$  both LOW, the TRI-STATE® B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the  $\overline{CEBA}$ ,  $\overline{LEBA}$  and  $\overline{OEBA}$  inputs.

**Data I/O Control Table**

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

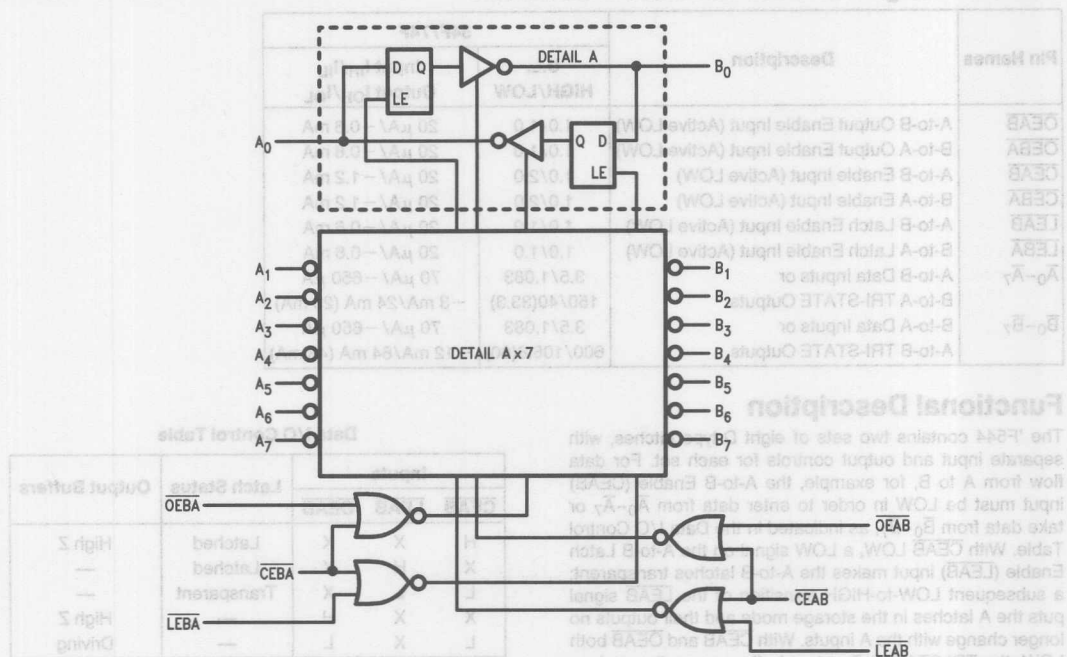
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

A-to-B data flow shown; B-to-A flow control is the same, except using  $\overline{CEBA}$ ,  $\overline{LEBA}$  and  $\overline{OEBA}$

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
---	----------------

Input Voltage (Note 2)	−0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	−30 mA to +5.0 mA
------------------------	-------------------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

Voltage Applied to Output in HIGH State (with V<sub>CC</sub> = 0V)

Standard Output −0.5V to V<sub>CC</sub>

TRI-STATE Output −0.5V to +5.5V

Current Applied to Output

in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military −55°C to +125°C

Commercial 0°C to +70°C

Supply Voltage

Military +4.5V to +5.5V

Commercial +4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA, (except $\bar{A}_n, \bar{B}_n$ )
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA ( $\bar{A}_n$ )
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA ( $\bar{A}_n, \bar{B}_n$ )
		54F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = −12 mA ( $\bar{B}_n$ )
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA ( $\bar{A}_n$ )
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA ( $\bar{A}_n, \bar{B}_n$ )
		74F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = −15 mA ( $\bar{B}_n$ )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA ( $\bar{A}_n$ )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA ( $\bar{A}_n$ )
		54F 10% V <sub>CC</sub>		0.55			I <sub>OL</sub> = 48 mA ( $\bar{B}_n$ )
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA ( $\bar{A}_n$ )
		74F 10% V <sub>CC</sub>		0.55			I <sub>OL</sub> = 64 mA ( $\bar{B}_n$ )
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V (except $\bar{A}_n, \bar{B}_n$ )
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V (except $\bar{A}_n, \bar{B}_n$ )
		74F		7.0			
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)	54F		1.0	mA	Max	V <sub>IN</sub> = 5.5V ( $\bar{A}_n, \bar{B}_n$ )
		74F		0.5			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub> ( $\bar{A}_n, \bar{B}_n$ )
		74F		250			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V ( $\bar{O}E\bar{A}\bar{B}, \bar{O}E\bar{B}\bar{A}$ )
				−1.2			V <sub>IN</sub> = 0.5V ( $\bar{C}E\bar{A}\bar{B}, \bar{C}E\bar{B}\bar{A}$ )
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V ( $\bar{A}_n, \bar{B}_n$ )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			−650	μA	Max	V <sub>OUT</sub> = 0.5V ( $\bar{A}_n, \bar{B}_n$ )

**DC Electrical Characteristics** (Continued)

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
I <sub>OS</sub>	Output Short-Circuit Current	-60 -100		-150 -225	mA	Max	V <sub>OUT</sub> = 0V ( $\bar{A}_n$ ) V <sub>OUT</sub> = 0V ( $\bar{B}_n$ )
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V ( $\bar{A}_n$ , $\bar{B}_n$ )
I <sub>CCH</sub>	Power Supply Current		70	105	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		85	130	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		83	125	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig No
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Transparent Mode A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	3.0 3.0	7.0 5.0	9.5 6.5	3.0 2.5	12.0 8.5	3.0 3.0	10.5 7.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEBA to A <sub>n</sub>	6.0 4.0	10.0 7.0	13.0 9.5	6.0 4.0	18.0 11.5	6.0 4.0	14.5 10.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEAB to B <sub>n</sub>	6.0 4.0	10.0 7.0	13.0 9.5	6.0 4.0	18.0 11.5	6.0 4.0	14.5 10.5	ns	2-3
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OEBA or OEAB to A <sub>n</sub> or B <sub>n</sub> CEBA or CEAB to A <sub>n</sub> or B <sub>n</sub>	3.0 4.0	7.0 7.5	9.0 10.5	3.0 4.0	11.0 13.0	3.0 4.0	10.0 12.0	ns	2-5
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OEBA or OEAB to A <sub>n</sub> or B <sub>n</sub> CEBA or CEAB to A <sub>n</sub> or B <sub>n</sub>	1.0 2.5	6.0 5.5	8.0 10.5	2.0 2.0	10.0 9.5	1.0 2.5	9.0 11.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig No
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> , V <sub>CC</sub> = Mil		T <sub>A</sub> , V <sub>CC</sub> = Com			
		Min	Max	Min	Max	Min	Max		
t <sub>s</sub> (H)	Setup Time, HIGH or LOW	3.0		3.0		3.0		ns	2-6
t <sub>s</sub> (L)	$\bar{A}_n$ or $\bar{B}_n$ to $\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$	3.0		3.0		3.0			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	3.0		3.0		3.0			
t <sub>h</sub> (L)	$\bar{A}_n$ or $\bar{B}_n$ to $\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$	3.0		3.0		3.0		ns	2-4
t <sub>w</sub> (L)	Latch Enable, B to A Pulse Width, LOW	6.0		9.0		7.5			
I <sub>OP</sub>	Output Leakage Current	0.0	2.75						
I <sub>IL</sub>	Input LOW Current	Max	-0.6						
I <sub>OH</sub>	Output Leakage Current	Max	70						
I <sub>OL</sub>	Output Leakage Current	Max	-650						

# 54F/74F545 Octal Bidirectional Transceiver with TRI-STATE® Outputs

## General Description

The 'F545 is an 8-bit, TRI-STATE, high-speed transceiver. It provides bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24 mA (20 mA Mil) bus drive capability on the A ports and 64 mA (48 mA Mil) bus drive capability on the B ports.

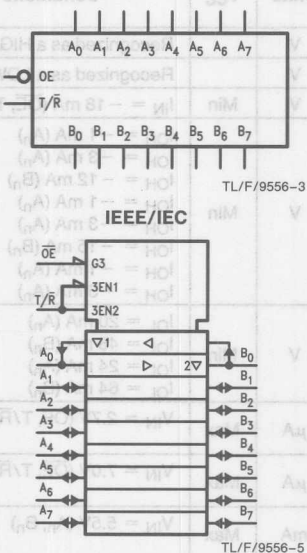
One input, Transmit/Receive (T/R) determines the direction of logic signals through the bidirectional transceiver. Transmit enables data from A ports to B ports; Receive enables data from B ports to A ports. The Output Enable input disables both A and B ports by placing them in a TRI-STATE condition.

## Features

- Higher drive than 8304
- 8-bit bidirectional data flow reduces system package count
- TRI-STATE inputs/outputs for interfacing with bus-oriented systems
- 24 mA (20 mA Mil) and 64 mA (48 mA Mil) bus drive capability on A and B ports, respectively
- Transmit/Receive and Output Enable simplify control logic
- Guaranteed 4000V minimum ESD protection
- Pin for Pin compatible with Intel 8286

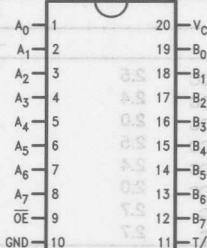
**Ordering Code:** See Section 5

## Logic Symbols

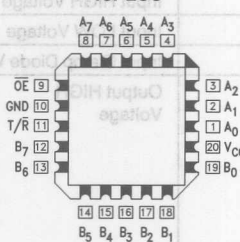


## Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



Pin Assignment for LCC



Truth Table

Inputs		Outputs
OE	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
OE	Output Enable Input (Active LOW)	1.0/2.0	20 $\mu$ A / -1.2 mA
T/R	Transmit/Receive Input	1.0/2.0	20 $\mu$ A / -1.2 mA
A <sub>0</sub> -A <sub>7</sub>	Side A TRI-STATE Inputs or TRI-STATE Outputs	3.5/1.083 150/40 (33.3)	70 $\mu$ A / -650 $\mu$ A -3 mA/24 mA (20 mA)
B <sub>0</sub> -B <sub>7</sub>	Side B TRI-STATE Inputs or TRI-STATE Outputs	3.5/1.083 600/106.6 (80)	70 $\mu$ A / -650 $\mu$ A -12 mA/64 mA (48 mA)



**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	-0.5V to V <sub>CC</sub>
Standard Output TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	-55°C to +125°C
Military	0°C to +70°C
Commercial	
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	

**DC Electrical Characteristics**

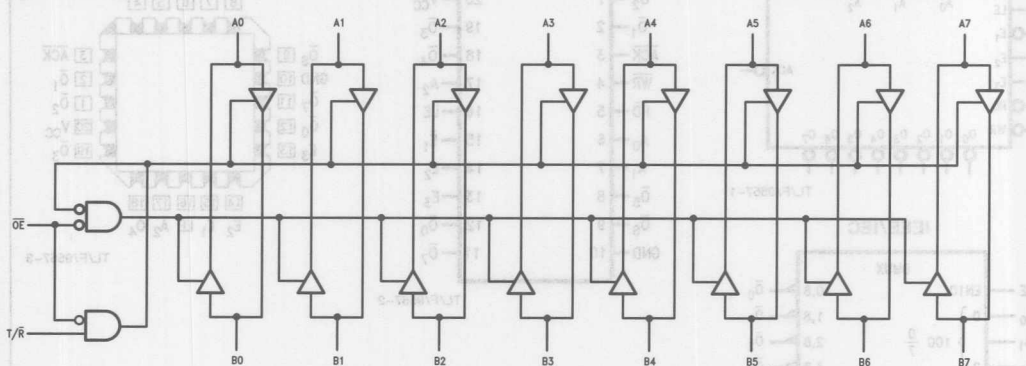
Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA (OE, T/ $\bar{R}$ )
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.4 2.0 2.5 2.4 2.0 2.7 2.7		V	Min	I <sub>OH</sub> = -1 mA (A <sub>n</sub> ) I <sub>OH</sub> = -3 mA (A <sub>n</sub> ) I <sub>OH</sub> = -12 mA (B <sub>n</sub> ) I <sub>OH</sub> = -1 mA (A <sub>n</sub> ) I <sub>OH</sub> = -3 mA (A <sub>n</sub> ) I <sub>OH</sub> = -15 mA (B <sub>n</sub> ) I <sub>OH</sub> = -1 mA (A <sub>n</sub> ) I <sub>OH</sub> = -3 mA (A <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.55 0.5 0.55	V	Min	I <sub>OL</sub> = 20 mA (A <sub>n</sub> ) I <sub>OL</sub> = 48 mA (B <sub>n</sub> ) I <sub>OL</sub> = 24 mA (A <sub>n</sub> ) I <sub>OL</sub> = 64 mA (B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V (OE, T/ $\bar{R}$ )
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V (OE, T/ $\bar{R}$ )
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)	54F 74F		1.0 0.5	mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-1.2	mA	Max	V <sub>IN</sub> = 0.5V (OE, T/ $\bar{R}$ )
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			-650	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current			-60 -100	mA	Max	V <sub>OUT</sub> = 0V (A <sub>n</sub> ) V <sub>OUT</sub> = 0V (B <sub>n</sub> )

**DC Electrical Characteristics** (Continued)

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current		70	90	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		95	120	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		85	110	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	2.5	4.2	6.0	2.0	7.5	2.5	7.0	ns	2-3
t <sub>PHL</sub>	A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	2.5	4.6	6.0	2.0	7.5	2.5	7.0		
t <sub>pZH</sub>	Output Enable Time	3.0	5.3	7.0	2.5	9.0	3.0	8.0	ns	2-5
t <sub>pZL</sub>		3.5	6.0	8.0	3.0	10.0	3.5	9.0		
t <sub>PHZ</sub>	Output Disable Time	3.0	5.0	6.5	2.5	9.0	3.0	7.5		
t <sub>PLZ</sub>		2.0	5.0	6.5	2.0	10.0	2.0	7.5		

**Logic Diagram**

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.


**54F/74F547**

## Octal Decoder/Demultiplexer with Address Latches and Acknowledge

### General Description

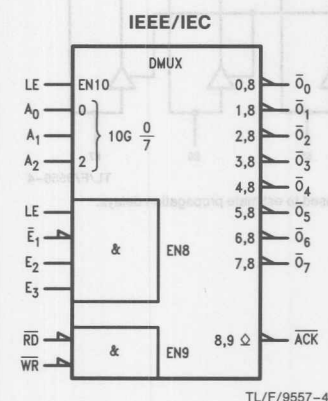
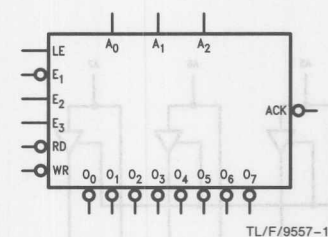
The 'F547 is a 3-to-8 line address decoder with latches for address storage. Designed primarily to simplify multiple chip selection in a microprocessor system, it contains one active LOW and two active HIGH Enables to conserve address space. Also included is an active LOW Acknowledge output that responds to either a Read or Write input signal when the Enables are active.

### Features

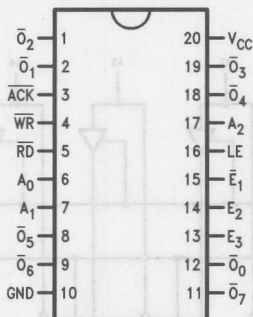
- 3-to-8 line address decoder
- Address storage latches
- Multiple enables for address extension
- Open collector acknowledge output

**Ordering Code:** See Section 5

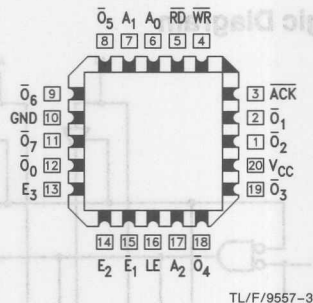
### Logic Symbols



Pin Assignment  
for DIP, SOIC and Flatpak



Pin Assignment  
for LCC



# Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_0$ – $A_2$	Address Select Inputs	1.0/1.0	20 $\mu$ A/–0.6 mA
$\bar{E}_1$	Chip Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/–0.6 mA
$E_2, E_3$	Chip Enable Inputs	1.0/1.0	20 $\mu$ A/–0.6 mA
LE	Latch Enable Input	1.0/1.0	20 $\mu$ A/–0.6 mA
$\bar{RD}$	Read Acknowledge Input (Active LOW)	1.0/1.0	20 $\mu$ A/–0.6 mA
$\bar{WR}$	Write Acknowledge Input (Active LOW)	1.0/1.0	20 $\mu$ A/–0.6 mA
ACK	Open Collector Acknowledge Output (Active LOW)	*OC/33.3	*OC/20 mA
$\bar{O}_0$ – $\bar{O}_7$	Decoded Outputs (Active LOW)	50/33.3	–1 mA/20 mA

\*OC = Open Collector

## Functional Description

When enabled, the 'F547 accepts the  $A_0$ – $A_2$  Address inputs and decodes them to select one of eight active LOW, mutually exclusive outputs, as shown in the Decoder Truth Table. With LE HIGH, the Address latches are transparent and the output selection changes each time the  $A_0$ – $A_2$  address changes. When LE is LOW, the latches store the last valid address preceding the HIGH-to-LOW transition of the LE input signal. For applications in which the separation of latch enable and chip enable functions is not required, LE and  $\bar{E}_1$  can be tied together, such that when HIGH the outputs are OFF and the latches are transparent, and when LOW the latches are storing and the selected output is enabled.

The open collector Acknowledge ( $\bar{ACK}$ ) output is normally HIGH (i.e., OFF) and goes LOW when  $\bar{E}_1$ ,  $E_2$  and  $E_3$  are all active and either the Read ( $\bar{RD}$ ) or Write ( $\bar{WR}$ ) input is LOW, as indicated in the Acknowledge Truth Table.

Acknowledge Truth Table

Inputs					Output
$\bar{E}_1$	$E_2$	$E_3$	$\bar{RD}$	$\bar{WR}$	ACK
H	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
L	H	H	H	H	H
L	H	H	L	X	L
L	H	H	X	L	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Latch Status Table

Input LE	Latch Status
H	Transparent
L	Storing

Output Status Table

Inputs			Decoder Outputs
$\bar{E}_1$	$E_2$	$E_3$	
L	H	H	$\bar{O}_n$ = LOW†
H	X	X	$O_0$ – $O_7$ = HIGH
X	L	X	$O_0$ – $O_7$ = HIGH
X	X	L	$O_0$ – $O_7$ = HIGH

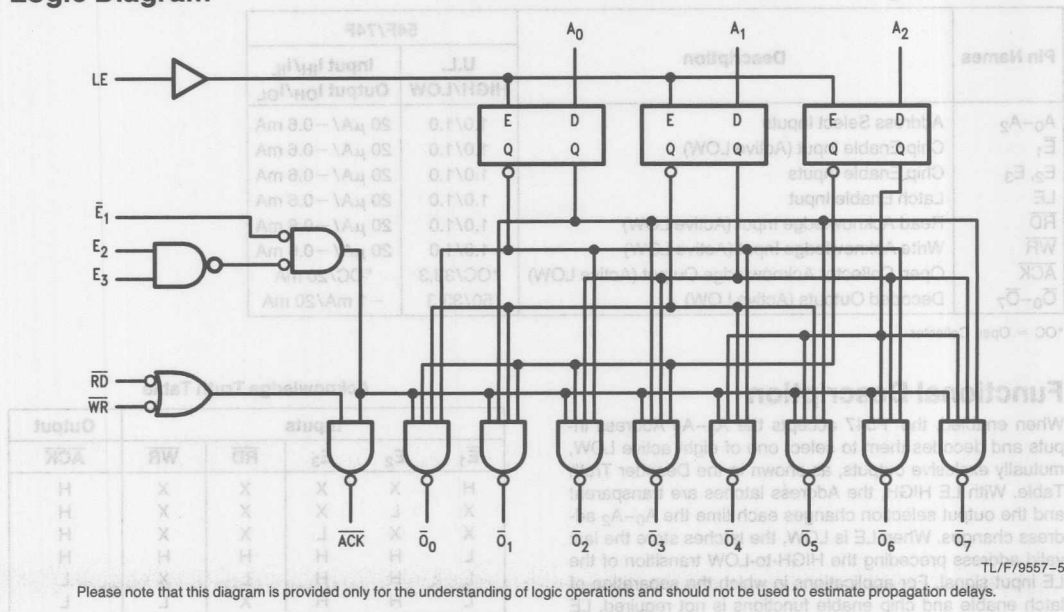
†See Decoder Truth Table

Decoder Truth Table\*

Inputs			Outputs							
$A_2$	$A_1$	$A_0$	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$	$\bar{O}_4$	$\bar{O}_5$	$\bar{O}_6$	$\bar{O}_7$
L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H
L	H	L	H	H	L	H	H	H	H	H
L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	H	H	H	L	H	H	H
H	L	H	H	H	H	H	H	L	H	H
H	H	L	H	H	H	H	H	H	L	H
H	H	H	H	H	H	H	H	H	H	L

\*Assuming  $\bar{E}_1$ , LOW;  $E_2$  and  $E_3$ , HIGH

## Logic Diagram



TL/F/9557-5

The open collector Acknowledge (ACK) output is normally HIGH (i.e., OFF) and goes LOW when E<sub>1</sub>, E<sub>2</sub> and E<sub>3</sub> are all active and either the Read (RD) or Write (WR) input is LOW, as indicated in the Acknowledge Truth Table.

LOW the latches are storing and the selected output is enabled.

LE input enables the output of the selected latch. The output of the selected latch is not enabled if the LE input is HIGH. The output of the selected latch is not enabled if the LE input is LOW and the latches are transparent, and when the output of the selected latch is not enabled.

When enabled, the output of the selected latch is HIGH or LOW, depending on the state of the selected latch. The output of the selected latch is not enabled if the LE input is HIGH. The output of the selected latch is not enabled if the LE input is LOW and the latches are transparent, and when the output of the selected latch is not enabled.

When enabled, the output of the selected latch is HIGH or LOW, depending on the state of the selected latch. The output of the selected latch is not enabled if the LE input is HIGH. The output of the selected latch is not enabled if the LE input is LOW and the latches are transparent, and when the output of the selected latch is not enabled.

Output Status Table

Inputs	Outputs
E <sub>0</sub> E <sub>1</sub> E <sub>2</sub> E <sub>3</sub>	Q <sub>0</sub> Q <sub>1</sub> Q <sub>2</sub> Q <sub>3</sub> Q <sub>4</sub> Q <sub>5</sub> Q <sub>6</sub> Q <sub>7</sub>
0 0 0 0	0 0 0 0 0 0 0 0
0 0 0 1	0 0 0 0 0 0 0 1
0 0 1 0	0 0 0 0 0 0 1 0
0 0 1 1	0 0 0 0 0 0 1 1
0 1 0 0	0 0 0 0 0 1 0 0
0 1 0 1	0 0 0 0 0 1 0 1
0 1 1 0	0 0 0 0 0 1 1 0
0 1 1 1	0 0 0 0 0 1 1 1
1 0 0 0	0 0 0 0 0 1 1 0
1 0 0 1	0 0 0 0 0 1 1 1
1 0 1 0	0 0 0 0 0 1 1 0
1 0 1 1	0 0 0 0 0 1 1 1
1 1 0 0	0 0 0 0 0 1 1 0
1 1 0 1	0 0 0 0 0 1 1 1
1 1 1 0	0 0 0 0 0 1 1 0
1 1 1 1	0 0 0 0 0 1 1 1

Decoder Truth Table

Inputs	Outputs
A <sub>0</sub> A <sub>1</sub> A <sub>2</sub>	Q <sub>0</sub> Q <sub>1</sub> Q <sub>2</sub> Q <sub>3</sub> Q <sub>4</sub> Q <sub>5</sub> Q <sub>6</sub> Q <sub>7</sub>
0 0 0	0 0 0 0 0 0 0 0
0 0 1	0 0 0 0 0 0 0 1
0 1 0	0 0 0 0 0 0 1 0
0 1 1	0 0 0 0 0 0 1 1
1 0 0	0 0 0 0 0 1 0 0
1 0 1	0 0 0 0 0 1 0 1
1 1 0	0 0 0 0 0 1 1 0
1 1 1	0 0 0 0 0 1 1 1

\* Assuming E<sub>0</sub>, E<sub>1</sub> and E<sub>2</sub> are HIGH

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	-0.5V to V <sub>CC</sub>
Standard Output TRI-STATE® Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	-55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA ( $\overline{O}_N$ )
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA ( $\overline{O}_N$ )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA ( $\overline{O}_N$ )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA ( $\overline{ACK}$ , $\overline{O}_N$ )
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA ( $\overline{ACK}$ , $\overline{O}_N$ )
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub> ( $\overline{O}_N$ )
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V ( $\overline{O}_N$ )
I <sub>OHC</sub>	Open Collector, Output OFF Leakage Test			250	μA	Min	V <sub>OUT</sub> = V <sub>CC</sub> ( $\overline{ACK}$ )
I <sub>CC</sub>	Power Supply Current		17	30	mA	Max	



Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	2.0	7.0	9.0	3.0	10.5	1.5	10.0	ns	2-3
t <sub>PHL</sub>	A <sub>n</sub> to $\bar{O}_n$	4.5	9.0	12.0	5.0	13.5	4.0	13.0		
t <sub>PLH</sub>	Propagation Delay	2.5	6.5	8.5	3.0	10.0	2.0	9.5	ns	2-3
t <sub>PHL</sub>	$\bar{E}_1$ to $\bar{O}_n$	3.0	6.5	8.5	3.5	10.0	3.0	9.5		
t <sub>PLH</sub>	Propagation Delay	3.5	7.5	10.0	4.0	11.5	3.0	11.0	ns	2-3
t <sub>PHL</sub>	LE to $\bar{O}_n$	5.0	14.5	14.0	5.0	20.0	5.0	15.0		
t <sub>PLH</sub>	Propagation Delay	4.0	8.5	10.0	4.5	12.5	3.0	11.0	ns	2-3
t <sub>PHL</sub>	E <sub>2</sub> or E <sub>3</sub> to $\bar{O}_n$	4.0	8.5	10.0	4.5	12.5	4.0	11.0		
t <sub>PLH</sub>	Propagation Delay	6.5	11.0	13.0	6.5	16.0	6.5	14.0	ns	2-3
t <sub>PHL</sub>	$\bar{E}_1$ , RD or WR to ACK	3.5	7.5	9.5	3.5	11.0	3.0	10.5		
t <sub>PLH</sub>	Propagation Delay	7.5	13.0	14.0	8.0	18.5	7.0	15.0	ns	2-3
t <sub>PHL</sub>	E <sub>2</sub> or E <sub>3</sub> to ACK	4.5	8.5	12.0	5.0	12.5	4.0	11.0		

### AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> , V <sub>CC</sub> = Mil		T <sub>A</sub> , V <sub>CC</sub> = Com			
		Min	Max	Min	Max	Min	Max		
t <sub>s</sub> (H)	Setup Time, HIGH or LOW	5.0		5.0		5.0		ns	2-6
t <sub>s</sub> (L)	A <sub>n</sub> to LE	5.0		5.0		5.0			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	6.0		6.0		6.0			
t <sub>h</sub> (L)	A <sub>n</sub> to LE	6.0		6.0		6.0		ns	2-4
t <sub>w</sub> (H)	LE Pulse Width, HIGH	6.0		6.0		6.0			



**54F/74F548**

## Octal Decoder/Demultiplexer with Acknowledge

### General Description

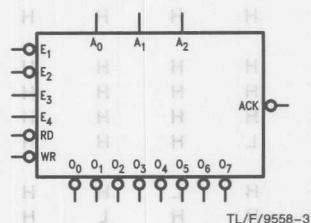
The 'F548 is a 3-to-8 line address decoder with four Enable inputs. Two of the Enables are Active LOW and two are Active HIGH for maximum addressing versatility. Also provided is an Active LOW Acknowledge output that responds to either a Read or Write input signal when the Enables are active.

### Features

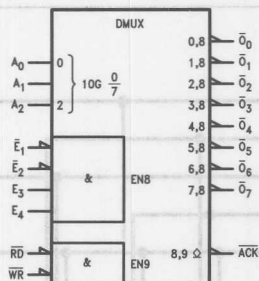
- 3-to-8 line address decoder
- Multiple enables for address extension
- Open collector acknowledge output
- Active LOW decoder outputs

**Ordering Code:** See Section 5

### Logic Symbols



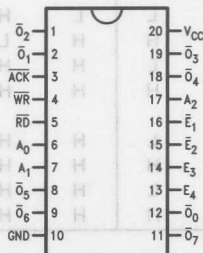
IEEE/IEC



TL/F/9558-5

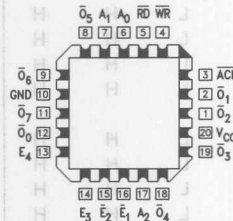
### Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak



TL/F/9558-1

Pin Assignment  
for LCC



TL/F/9558-2

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I <sub>IH</sub> /I <sub>IL</sub> Output I <sub>OH</sub> /I <sub>OL</sub>
A <sub>0</sub> -A <sub>2</sub>	Output Select Address Inputs	1.0/1.0	20 μA/-0.6 mA
E <sub>1</sub> , E <sub>2</sub>	Chip Enable Inputs (Active LOW)	1.0/1.0	20 μA/-0.6 mA
E <sub>3</sub> , E <sub>4</sub>	Chip Enable Inputs	1.0/1.0	20 μA/-0.6 mA
RD	Read Acknowledge Input (Active LOW)	1.0/1.0	20 μA/-0.6 mA
WR	Write Acknowledge Input (Active LOW)	1.0/1.0	20 μA/-0.6 mA
ACK	Open Collector Acknowledge Output (Active LOW)	OC*/33.3	* /20 mA
O <sub>0</sub> -O <sub>7</sub>	Decoded Outputs (Active LOW)	50/33.3	-1 mA/20 mA

\*OC = Open Collector

## Functional Description

When enabled, the 'F548 accepts the  $A_0$ – $A_2$  Address inputs and decodes them to select one of eight active LOW, mutually exclusive outputs, as shown in the Decoder Truth Table. When one or more Enables is inactive, all decoder outputs are HIGH. Thus, the 'F548 can be used as a demultiplexer by applying data to one of the Enables.

The open collector Acknowledge (ACK) output is normally HIGH (i.e., OFF) and goes LOW when the Enables are all active and either the Read ( $\overline{RD}$ ) or Write ( $\overline{WR}$ ) input is LOW, as indicated in the Acknowledge Truth Table.

### Acknowledge Truth Table

Inputs						Output
$\overline{E}_1$	$\overline{E}_2$	$E_3$	$E_4$	$\overline{RD}$	$\overline{WR}$	ACK
H	X	X	X	X	X	H
X	H	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
X	X	X	X	L	X	H
X	X	X	X	X	L	H
L	L	H	H	H	H	L
L	L	H	H	L	X	L
L	L	H	H	X	L	L

H = HIGH Voltage Level

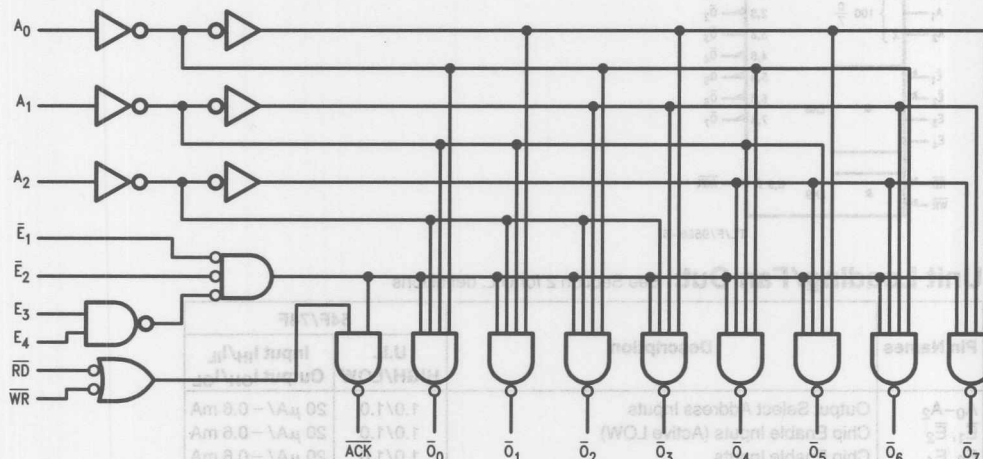
L = LOW Voltage Level

X = Immaterial

### Decoder Truth Table

Inputs							Outputs							
$\overline{E}_1$	$\overline{E}_2$	$E_3$	$E_4$	$A_2$	$A_1$	$A_0$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	X	H	H	H	H	H	H	H	H
X	X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	L	H	H	H	H	H
L	L	L	H	H	L	L	H	H	H	L	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	L	H	H	H
L	L	L	H	H	H	L	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	L

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

TL/F/9558-4

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
---	----------------

Input Voltage (Note 2)	−0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	−30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
---	--------------------------

Standard Output TRI-STATE® Output	−0.5V to +5.5V
-----------------------------------	----------------

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military

Commercial

Supply Voltage

Military

Commercial

−55°C to +125°C

0°C to +70°C

+4.5V to +5.5V

+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA ( $\overline{O}_0$ – $\overline{O}_7$ )
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA ( $\overline{O}_0$ – $\overline{O}_7$ )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA ( $\overline{O}_0$ – $\overline{O}_7$ )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V ( $\overline{O}_0$ – $\overline{O}_7$ )
I <sub>OHC</sub>	Open Collector, Output OFF Leakage Test			250	μA	Min	V <sub>OUT</sub> = V <sub>CC</sub> ( $\overline{ACK}$ )
I <sub>CCH</sub>	Power Supply Current		14	21	mA	Max	V <sub>O</sub> = HIGH

# **AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n$ to $\overline{O}_n$	2.0 4.0	5.5 8.0	8.0 9.5	3.0 4.0	10.0 12.0	1.5 4.0	9.0 10.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	2.5 3.5	6.5 6.5	8.5 8.5	3.0 3.5	10.0 10.0	2.0 3.0	9.5 9.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $E_3$ or $E_4$ to $\overline{O}_n$	4.0 4.0	8.5 8.5	9.5 9.5	5.0 4.0	13.0 12.5	3.0 3.5	10.5 10.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{ACK}$	6.5 3.0	11.0 7.5	12.5 9.5	6.5 3.0	16.5 11.0	6.5 3.0	13.0 10.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $E_3$ or $E_4$ to $\overline{ACK}$	8.0 4.0	13.0 8.5	14.0 10.0	8.0 4.0	19.5 13.0	8.0 4.0	15.0 11.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{RD}$ or $\overline{WR}$ to $\overline{ACK}$	5.5 2.5	10.0 5.0	12.0 8.0	5.5 2.5	16.5 8.5	5.5 2.5	12.5 8.5	ns	2-3

Symbol	Parameter	74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
$V_{IH}$	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
$V_{IL}$	Input LOW Voltage	0.8			V		Recognized as a LOW Signal
$V_{CC}$	Input Clamp Diode Voltage	-1.2			V	Min	$I_{IH} = -18\text{mA}$
$V_{OH}$	Output HIGH Voltage	2.7			V	Min	$I_{OH} = -1\text{mA}$ ( $\bar{O}_n$ - $\bar{O}_n$ ) $I_{OH} = -1\text{mA}$ ( $\bar{O}_n$ - $\bar{O}_n$ ) $I_{OH} = -1\text{mA}$ ( $\bar{O}_n$ - $\bar{O}_n$ )
$V_{OL}$	Output LOW Voltage	0.5			V	Min	$I_{OL} = 20\text{mA}$ $I_{OL} = 20\text{mA}$
$I_{IH}$	Input HIGH Current	2.0			$\mu\text{A}$	Max	$V_{IH} = 2.7\text{V}$
$I_{OH}$	Input HIGH Current	100			$\mu\text{A}$	Max	$V_{IH} = 7.0\text{V}$
$I_{OH}$	Output HIGH Current	250			$\mu\text{A}$	Max	$V_{OH} = V_{CC}$
$I_{OL}$	Output LOW Current	20			$\mu\text{A}$	Max	$I_{OH} = 1.3\text{mA}$ All Other Pins Grounded
$I_{OH}$	Output Leakage Current	3.75			$\mu\text{A}$	0.0	$V_{CC} = 180\text{mV}$ All Other Pins Grounded
$I_{IL}$	Input LOW Current	-0.8			$\text{mA}$	Max	$V_{IH} = 0.5\text{V}$
$I_{OS}$	Output Short-Circuit Current	-80			$\text{mA}$	Max	$V_{OH} = 0\text{V}$ ( $\bar{O}_n$ - $\bar{O}_n$ )
$I_{OH}$	Open Collector Output OFF Leakage Test	250			$\mu\text{A}$	Min	$V_{OH} = V_{CC}$ (ACK)
$I_{OH}$	Power Supply Current	14			$\text{mA}$	Max	$V_O = \text{HIGH}$



## 54F/74F550 • 54F/74F551

### Octal Registered Transceiver with Status Flags

#### General Description

The 'F550 and 'F551 octal transceivers each contain two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock pulse and clock enable inputs, as well as a flag flip-flop that is set automatically as the register is loaded. Each flag flip-flop is provided with a clear input, and each register has a separate output enable control for its TRI-STATE® buffers. The separate clocks, flags and enables provide considerable flexibility as I/O ports for demand-response data transfer. The 'F550 is non-inverting; the 'F551 inverts data in both directions.

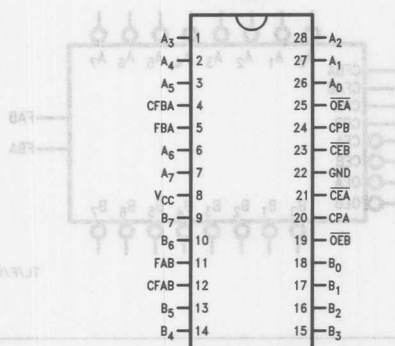
#### Features

- 8-bit bidirectional I/O port with handshake
- Back-to-back registers for storage
- Register status flag flip-flops
- Separate edge-detecting clears for flags
- Inverting and non-inverting versions
- B outputs sink 64 mA (48 mA Mil)

**Ordering Code:** See Section 5

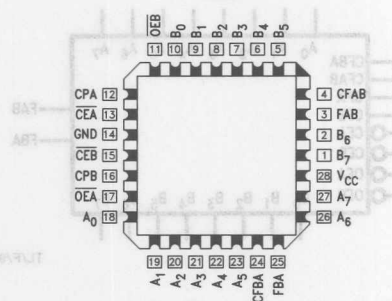
#### Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak  
'F550



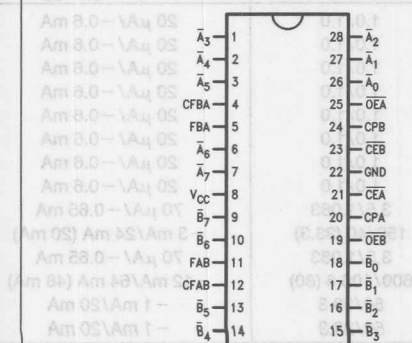
TL/F/9559-1

Pin Assignment  
for LCC  
'F550



TL/F/9559-2

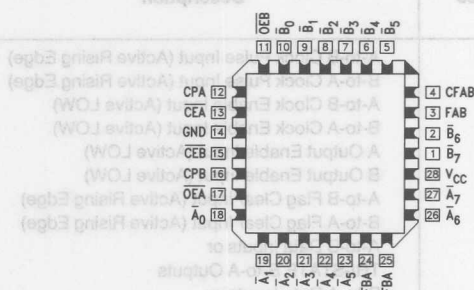
'F551



TL/F/9559-8

IEEE/IEC

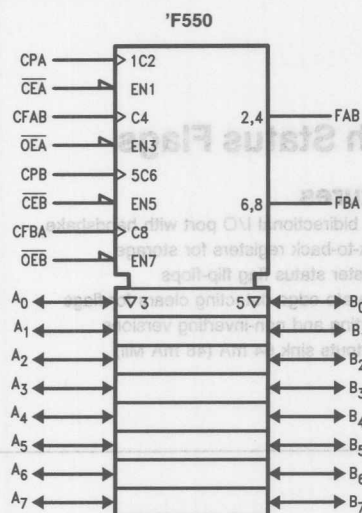
'F551



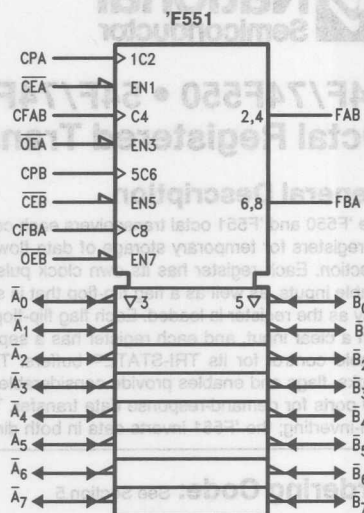
TL/F/9559-9



## Connection Diagrams (Continued)

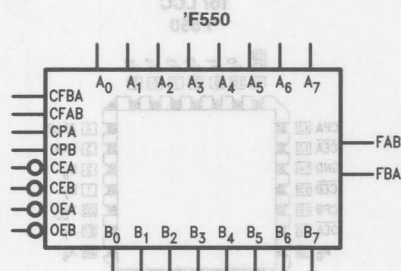


TL/F/9559-10

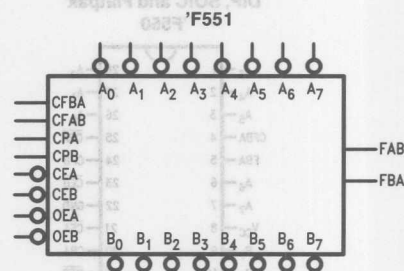


TL/F/9559-11

## Logic Symbols



TL/F/9559-3



TL/F/9559-7

## Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
CPA	A-to-B Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu\text{A}$ / -0.6 mA
CPB	B-to-A Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu\text{A}$ / -0.6 mA
$\overline{\text{CEA}}$	A-to-B Clock Enable Input (Active LOW)	1.0/1.0	20 $\mu\text{A}$ / -0.6 mA
$\overline{\text{CEB}}$	B-to-A Clock Enable Input (Active LOW)	1.0/1.0	20 $\mu\text{A}$ / -0.6 mA
$\overline{\text{OEA}}$	A Output Enable Input (Active LOW)	1.0/1.0	20 $\mu\text{A}$ / -0.6 mA
$\overline{\text{OEB}}$	B Output Enable Input (Active LOW)	1.0/1.0	20 $\mu\text{A}$ / -0.6 mA
CFAB	A-to-B Flag Clear Input (Active Rising Edge)	1.0/1.0	20 $\mu\text{A}$ / -0.6 mA
CFBA	B-to-A Flag Clear Input (Active Rising Edge)	1.0/1.0	20 $\mu\text{A}$ / -0.6 mA
$\text{A}_0$ - $\text{A}_7$	A-to-B Data Inputs or TRI-STATE B-to-A Outputs	3.5/1.083 150/40 (33.3)	70 $\mu\text{A}$ / -0.65 mA -3 mA/24 mA (20 mA)
$\text{B}_0$ - $\text{B}_7$	B-to-A Data Inputs or TRI-STATE A-to-B Outputs	3.5/1.083 600/106.6 (80)	70 $\mu\text{A}$ / -0.65 mA -12 mA/64 mA (48 mA)
FAB	A-to-B Status Flag Output (Active HIGH)	50/33.3	-1 mA/20 mA
FBA	B-to-A Status Flag Output (Active HIGH)	50/33.3	-1 mA/20 mA

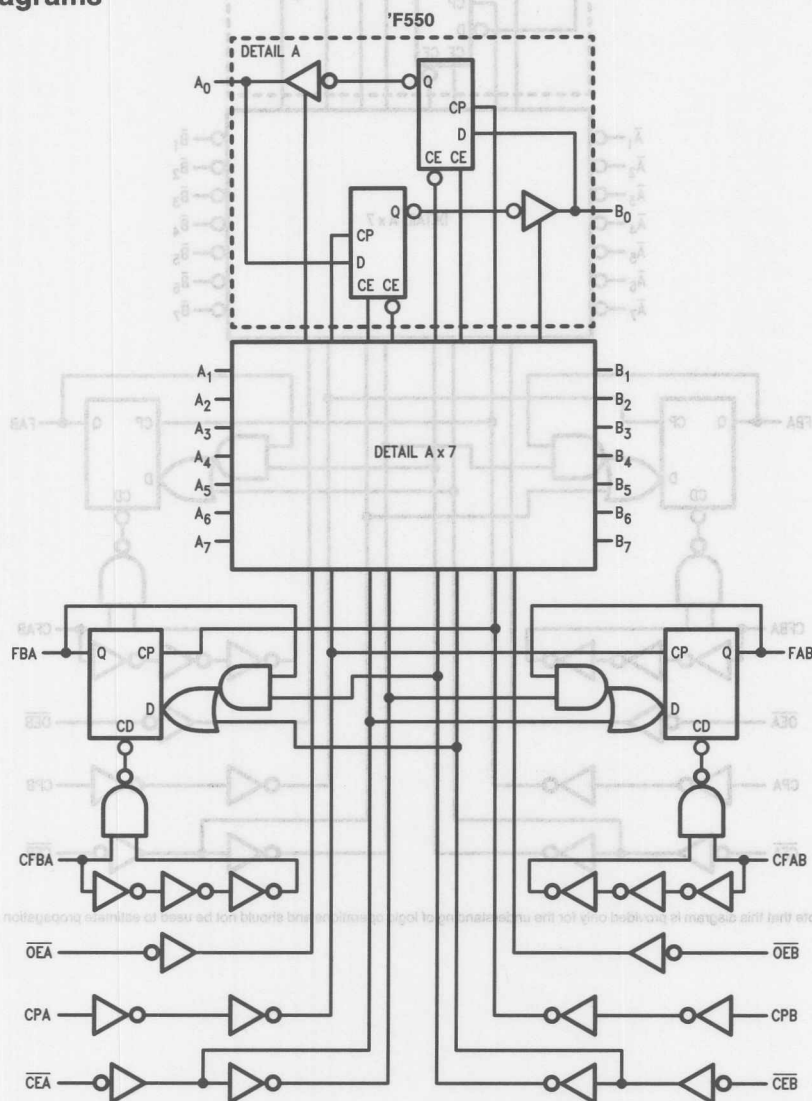
## Functional Description

Data applied to the A inputs is entered and stored on the rising edge of the A Clock Pulse (CPA), provided that the A Clock Enable ( $\overline{\text{CEA}}$ ) is LOW; simultaneously, the status flip-flop is set and the A-to-B flag (FAB) output goes HIGH. Data thus entered from the A inputs is present at the inputs to the B output buffers, but only appears on the B I/O pins when the B Output Enable ( $\overline{\text{OEB}}$ ) signal is made LOW. After the B output data is assimilated, the receiving system clears the A-to-B flag flip-flop by applying a LOW-to-HIGH tran-

sition to the CFAB input. Optionally, the  $\overline{\text{OEB}}$  and CFAB pins can be tied together and operated by one function from the receiving system.

Data flow from B-to-A proceeds in the same manner described for A-to-B flow. Inputs  $\overline{\text{CEB}}$  and CPB enter the B input data and set the B-to-A flag (FBA) output HIGH. A LOW signal on  $\overline{\text{OEA}}$  enables the A output buffers and a LOW-to-HIGH transition on CFBA clears the FBA flag.

## Logic Diagrams



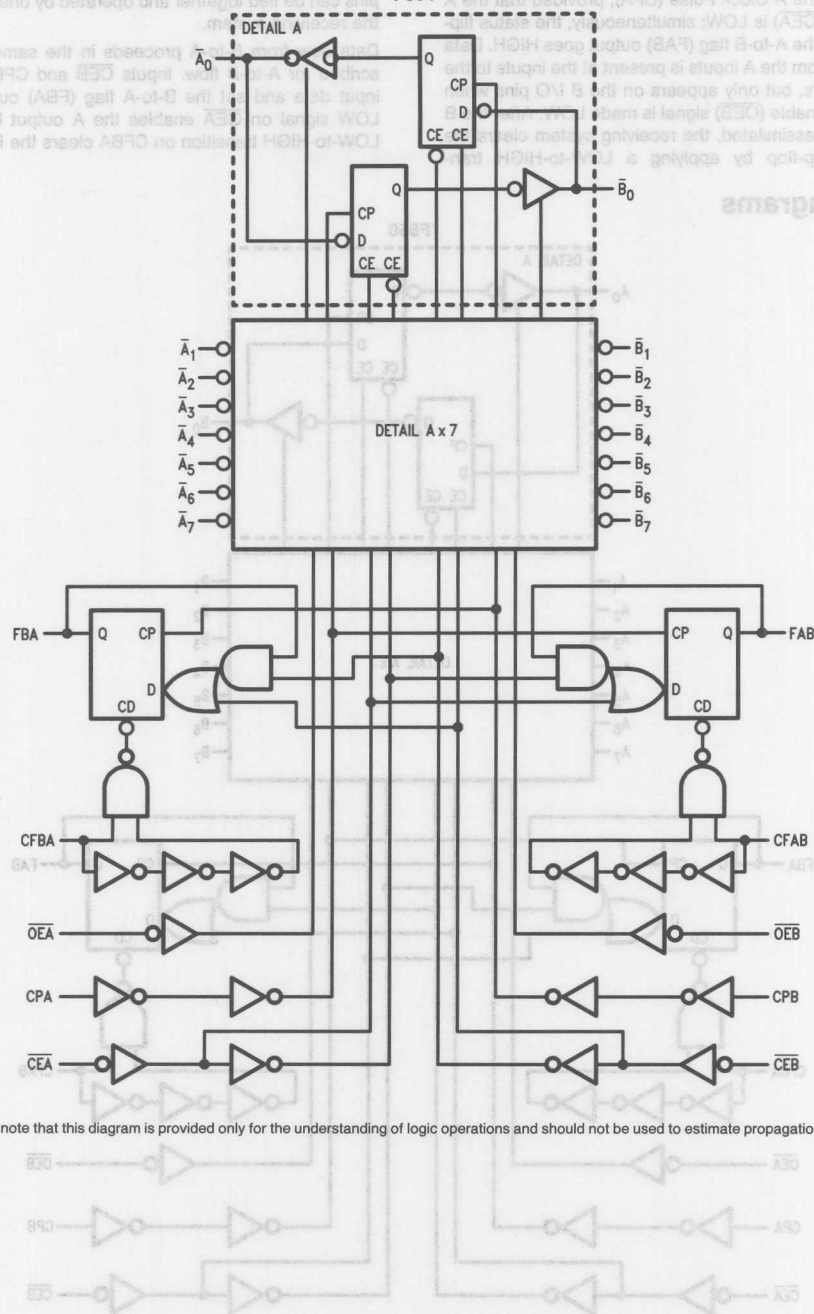
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

TL/F/9559-4

# Logic Diagrams (Continued)

Functional Description

Data applied to the A inputs is entered and stored on the rising edge of the A Clock Pulse (CPA), provided that the A Clock Enable (CEA) is LOW; simultaneously, the status flip-flop is set and the A-to-B flag (FAB) output goes HIGH. This flip-flop is reset and the A-to-B flag (FAB) output goes LOW when the B output buffer, but only appears on the 5 V<sub>IO</sub> pin, the B Output Enable (OEB) signal is made LOW. The receiving system clears the output data is assimilated, the receiving system clears the A-to-B flag flip-flop by applying a LOW-to-HIGH transition on the B Clock Pulse (CPB), provided that the B Clock Enable (CEB) is LOW.



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA (A <sub>0</sub> –A <sub>7</sub> )
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA (A <sub>0</sub> –A <sub>7</sub> )
		54F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = −12 mA (B <sub>0</sub> –B <sub>7</sub> )
		74F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA (A <sub>0</sub> –A <sub>7</sub> )
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA (A <sub>0</sub> –A <sub>7</sub> )
		74F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = −15 mA (B <sub>0</sub> –B <sub>7</sub> )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA (A <sub>0</sub> –A <sub>7</sub> )
V <sub>OL</sub>	Output Low Voltage	54F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA (A <sub>0</sub> –A <sub>7</sub> )
		54F 10% V <sub>CC</sub>		0.55	V	Min	I <sub>OL</sub> = 48 mA (B <sub>0</sub> –B <sub>7</sub> )
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA (A <sub>0</sub> –A <sub>7</sub> )
		74F 10% V <sub>CC</sub>		0.55			I <sub>OL</sub> = 64 mA (B <sub>0</sub> –B <sub>7</sub> )
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V (Non I/O Inputs)
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V (Non I/O Inputs)
		74F		7.0			
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)	54F		1.0	mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
		74F		0.5			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V (Non I/O Inputs)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>0</sub> –A <sub>7</sub> , B <sub>0</sub> –B <sub>7</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			−650	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>0</sub> –A <sub>7</sub> , B <sub>0</sub> –B <sub>7</sub> )

**DC Electrical Characteristics** (Continued)

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
I <sub>OS</sub>	Output Short-Circuit Current	-60 -100		-150 -225	mA mA	Max Max	V <sub>OUT</sub> = 0V (A <sub>0</sub> -A <sub>7</sub> ) V <sub>OUT</sub> = 0V (B <sub>0</sub> -B <sub>7</sub> )
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CC</sub> H	Power Supply Current		84	140	mA	Max	V <sub>O</sub> = HIGH
I <sub>CC</sub> L	Power Supply Current		105	140	mA	Max	V <sub>O</sub> = LOW
I <sub>CC</sub> Z	Power Supply Current		102	140	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	3.0	5.5	7.5			2.5	8.5	ns	2-3
t <sub>PHL</sub>	CPA or CPB to B <sub>n</sub> or A <sub>n</sub>	4.0	7.0	9.0			3.5	10.0		
t <sub>PLH</sub>	Propagation Delay	3.5	6.0	8.0			3.0	9.0	ns	2-3
	CPA or CPB to FBA or FAB									
t <sub>PHL</sub>	Propagation Delay	5.0	9.0	11.5			4.5	13.0	ns	2-3
	CFAB or CFBA to FAB or FBA									
t <sub>PZH</sub>	Output Enable Time	2.5	5.5	7.5			2.0	8.5	ns	2-5
t <sub>PZL</sub>	OEA or OEB to A <sub>n</sub> or B <sub>n</sub>	3.5	7.0	9.5			3.0	10.5		
t <sub>PHZ</sub>	Output Disable Time	3.0	6.5	9.0			2.5	10.0		
t <sub>PLZ</sub>	OEA or OEB to A <sub>n</sub> or B <sub>n</sub>	2.5	5.5	7.5			2.0	8.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> , V <sub>CC</sub> = Mil		T <sub>A</sub> , V <sub>CC</sub> = Com			
		Min	Max	Min	Max	Min	Max		
t <sub>s</sub> (H)	Setup Time, HIGH or LOW	4.0				4.5		ns	2-6
t <sub>s</sub> (L)	A <sub>n</sub> , B <sub>n</sub> to CPA, CPB	4.0				4.5			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	2.0				2.5			
t <sub>h</sub> (L)	A <sub>n</sub> , B <sub>n</sub> to CPA, CPB	2.0				2.5			
t <sub>s</sub> (H)	Setup Time, HIGH or LOW	1.0				1.5		ns	2-6
t <sub>s</sub> (L)	CEA, CEB to CPA, CPB	4.0				4.5			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	2.0				2.5			
t <sub>h</sub> (L)	CEA, CEB to CPA, CPB	2.0				2.5			
t <sub>w</sub> (H)	Pulse Width, HIGH or LOW	3.0				3.5		ns	2-4
t <sub>w</sub> (L)	CPA or CPB	3.0				3.5			
t <sub>w</sub> (H)	Pulse Width, HIGH	3.0				3.5		ns	2-4
	CFAB or CFBA								
t <sub>rec</sub>	Recovery Time	9.0				10.0		ns	2-6
	CFAB, CFBA to CPA, CPB								

## 54F/74F552

# Octal Registered Transceiver with Parity and Flags

## General Description

The 'F552 octal transceiver contains two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock pulse and clock enable input as well as a flag flip-flop that is set automatically as the register is loaded. The flag output will be reset when the output enable returns to HIGH after reading the output port. Each register has a separate output enable control for its TRI-STATE® buffer. The separate Clocks, Flags, and Enables provide considerable flexibility as I/O ports for demand-response data transfer. When data is transferred from the A-port to the B-port, a parity bit is generated. On the

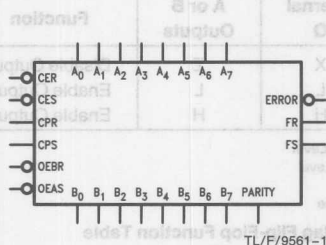
other hand, when data is transferred from the B-port to the A-port, the parity of input data on B<sub>0</sub>-B<sub>7</sub> is checked.

## Features

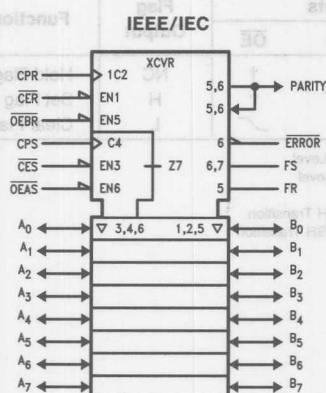
- 8-Bit bidirectional I/O Port with handshake
- Register status flag flip-flops
- Separate clock enable and output enable
- Parity generation and parity check
- B-outputs sink 64 mA
- TRI-STATE outputs

**Ordering Code:** See Section 5

## Logic Symbols

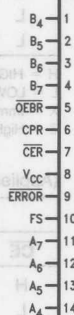


TL/F/9561-1



TL/F/9561-5

## Pin Assignment for DIP, SOIC and Flatpak



## Connection Diagrams

### Pin Assignment for LCC and PCC



TL/F/9561-3

TL/F/9561-2

## Register Function Table

(Applies to R or S Register)

Function	Internal	CP	CE
Hold Data	NC	X	X
Load Data	L	L	L
Keep Old Data	NC	L	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Indeterminate  
~ = LOW-to-HIGH Transition  
↑ = First LOW-to-HIGH Transition  
NC = No Change



# Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
A <sub>0</sub> –A <sub>7</sub>	A-to-B Port Data Inputs or B-to-A TRI-STATE	3.5/1.083 150/40 (33.3)	70 $\mu$ A/–0.65 mA –3 mA/24 mA (20 mA)
B <sub>0</sub> –B <sub>7</sub>	B-to-A Transceiver Inputs or A-to-B TRI-STATE Output	3.5/1.083 600/106.6 (80)	70 $\mu$ A/–0.65 mA –12 mA/64 mA (48 mA)
FR	B Port Flag Output	50/33.3	–1 mA/20 mA
FS	A Port Flag Output	50/33.3	–1 mA/20 mA
PARITY	Parity Bit Transceiver Input or Output	3.5/1.083 600/106.6 (50)	70 $\mu$ A/–0.65 mA –12 mA/64 mA (48 mA)
ERROR	Parity Check Output (Active LOW)	50/33.3	–1 mA/20 mA
CER	R Registers Clock Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/–0.6 mA
CES	S Registers Clock Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/–0.6 mA
CPR	R Registers Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/–0.6 mA
CPS	S Registers Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/–0.6 mA
OE $\overline{B}$ R	B Port and PARITY Output Enable (Active LOW) and Clear FR Input (Active Rising Edge)	1.0/2.0	20 $\mu$ A/–1.2 mA
OE $\overline{A}$ S	A Port Output Enable (Active LOW) and Clear FS Input (Active Rising Edge)	1.0/2.0	20 $\mu$ A/–1.2 mA

## Functional Description

Data applied to the A-inputs are entered and stored in the R register on the rising edge of the CPR Clock Pulse, provided that the Clock Enable ( $\overline{CER}$ ) is LOW; simultaneously, the status flip-flop is set and the flag (FR) output goes HIGH. As the Clock Enable ( $\overline{CER}$ ) returns to HIGH, the data will be held in the R register. These data entered from the A-inputs will appear at the B-port I/O pins after the Output Enable ( $\overline{OEBR}$ ) has gone LOW. When  $\overline{OEBR}$  is LOW, a parity bit appears at the PARITY pin, which will be set HIGH when there is an even number of 1s or all 0s at the Q outputs of the R register. After the data is assimilated, the receiving system clears the flag FR by changing the signal at the  $\overline{OEBR}$  pin from LOW to HIGH.

Data flow from B-to-A proceeds in the same manner described for A-to-B flow. A LOW at the  $\overline{CES}$  pin and a LOW-to-HIGH transition at CPS pin enters the B-input data and the parity-input data into the S registers and the parity register respectively and set the flag output FS to HIGH. A LOW signal at the  $\overline{OEAS}$  pin enables the A-port I/O pins and a LOW-to-HIGH transition of the  $\overline{OEAS}$  signal clears the FS flag. When  $\overline{OEAS}$  is LOW, the parity check output ERROR will be HIGH if there is an odd number of 1s at the Q outputs of the S registers and the parity register. The flag FS can be cleared by a LOW-to-HIGH transition of the  $\overline{OEAS}$  signal.

### Register Function Table

(Applies to R or S Register)

Inputs			Internal Q	Function
D	CP	$\overline{CE}$		
X	X	H	NC	Hold Data
L	—	L	L	Load Data
H	—	L	H	Load Data
X	†	L	NC	Keep Old Data

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
— = LOW-to-HIGH Transition  
† = Not LOW-to-HIGH Transition  
NC = No Change

### Output Control

$\overline{OE}$	Internal Q	A or B Outputs	Function
H	X	Z	Disable Output
L	L	L	Enable Output
L	H	H	Enable Output

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

### Flag Flip-Flop Function Table

(Applies to R or S Flag Flip-Flop)

Inputs			Flag Output	Function
$\overline{CE}$	CP	$\overline{OE}$		
H	X	†	NC	Hold Flag
L	—	†	H	Set Flag
X	X	—	L	Clear Flag

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
— = LOW-to-HIGH Transition  
† = Not LOW-to-HIGH Transition  
NC = No Change

## Functional Description

### Parity Generation Function

OEBR	Number of HIGHS in the Q Outputs of the R Register	Parity Output
H	X	Z
L	0, 2, 4, 6, 8	H
L	1, 3, 5, 7	L

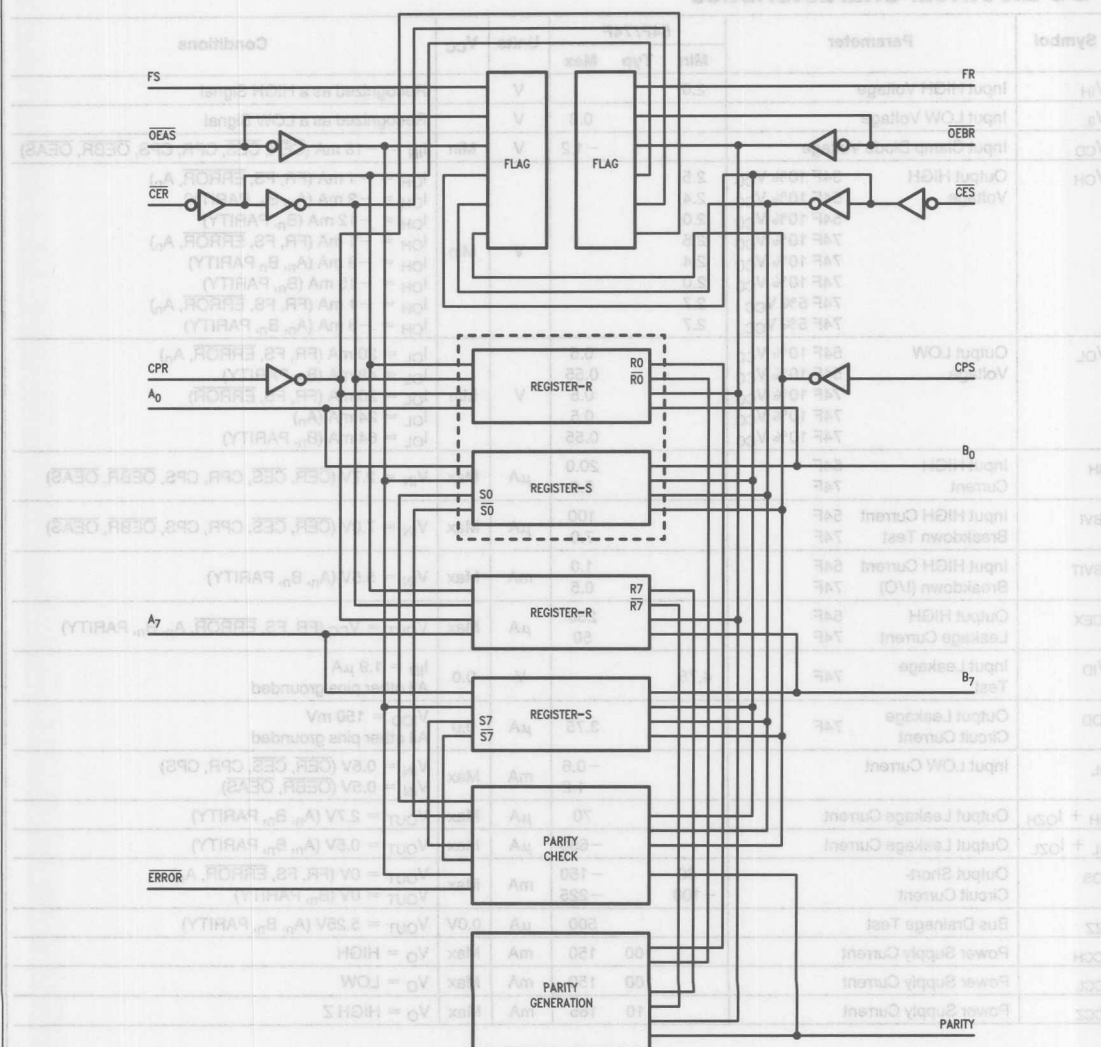
H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

### Parity Check Function

OEAS	Number of HIGHS in the Q Outputs of the S Register	Parity Input	ERROR Output
H	X	X	H
L	0, 2, 4, 6, 8	L	L
L	1, 3, 5, 7	L	H
L	0, 2, 4, 6, 8	H	H
L	1, 3, 5, 7	H	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

## Block Diagram



TL/F/9561-4

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

Ambient Temperature under Bias  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Junction Temperature under Bias  $-55^{\circ}\text{C}$  to  $+175^{\circ}\text{C}$

$V_{CC}$  Pin Potential to Ground Pin  $-0.5\text{V}$  to  $+7.0\text{V}$

Input Voltage (Note 2)  $-0.5\text{V}$  to  $+7.0\text{V}$

Input Current (Note 2)  $-30\text{ mA}$  to  $+5.0\text{ mA}$

Voltage Applied to Output in HIGH State (with  $V_{CC} = 0\text{V}$ )  $-0.5\text{V}$  to  $V_{CC}$

Standard Output  $-0.5\text{V}$  to  $V_{CC}$

TRI-STATE Output  $-0.5\text{V}$  to  $+5.5\text{V}$

Current Applied to Output in LOW State (Max) twice the rated  $I_{OL}$  (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature  
 Military  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
 Commercial  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$

Supply Voltage  
 Military  $+4.5\text{V}$  to  $+5.5\text{V}$   
 Commercial  $+4.5\text{V}$  to  $+5.5\text{V}$

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	$V_{CC}$	Conditions
		Min	Typ	Max			
$V_{IH}$	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
$V_{IL}$	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
$V_{CD}$	Input Clamp Diode Voltage			-1.2	V	Min	$I_{IN} = -18\text{ mA}$ (CER, CES, CPR, CPS, OEER, OEAS)
$V_{OH}$	Output HIGH Voltage	54F 10% $V_{CC}$	2.5		V	Min	$I_{OH} = -1\text{ mA}$ (FR, FS, ERROR, $A_n$ )
		54F 10% $V_{CC}$	2.4				$I_{OH} = -3\text{ mA}$ ( $A_n$ , $B_n$ , PARITY)
		54F 10% $V_{CC}$	2.0				$I_{OH} = -12\text{ mA}$ ( $B_n$ , PARITY)
		74F 10% $V_{CC}$	2.5				$I_{OH} = -1\text{ mA}$ (FR, FS, ERROR, $A_n$ )
		74F 10% $V_{CC}$	2.4				$I_{OH} = -3\text{ mA}$ ( $A_n$ , $B_n$ , PARITY)
		74F 10% $V_{CC}$	2.0				$I_{OH} = -15\text{ mA}$ ( $B_n$ , PARITY)
		74F 5% $V_{CC}$	2.7				$I_{OH} = -1\text{ mA}$ (FR, FS, ERROR, $A_n$ )
$V_{OL}$	Output LOW Voltage	54F 10% $V_{CC}$		0.5	V	Min	$I_{OL} = 20\text{ mA}$ (FR, FS, ERROR, $A_n$ )
		54F 10% $V_{CC}$		0.55			$I_{OL} = 48\text{ mA}$ ( $B_n$ , PARITY)
		74F 10% $V_{CC}$		0.5			$I_{OL} = 20\text{ mA}$ (FR, FS, ERROR)
		74F 10% $V_{CC}$		0.5			$I_{OL} = 24\text{ mA}$ ( $A_n$ )
		74F 10% $V_{CC}$		0.55			$I_{OL} = 64\text{ mA}$ ( $B_n$ , PARITY)
$I_{IH}$	Input HIGH Current	54F		20.0	$\mu\text{A}$	Max	$V_{IN} = 2.7\text{V}$ (CER, CES, CPR, CPS, OEER, OEAS)
		74F		5.0			
$I_{BVI}$	Input HIGH Current Breakdown Test	54F		100	$\mu\text{A}$	Max	$V_{IN} = 7.0\text{V}$ (CER, CES, CPR, CPS, OEER, OEAS)
		74F		7.0			
$I_{BVI}$	Input HIGH Current Breakdown (I/O)	54F		1.0	mA	Max	$V_{IN} = 5.5\text{V}$ ( $A_n$ , $B_n$ , PARITY)
		74F		0.5			
$I_{CEX}$	Output HIGH Leakage Current	54F		250	$\mu\text{A}$	Max	$V_{OUT} = V_{CC}$ (FR, FS, ERROR, $A_n$ , $B_n$ , PARITY)
		74F		50			
$V_{ID}$	Input Leakage Test	74F	4.75		V	0.0	$I_{ID} = 1.9\text{ }\mu\text{A}$ All other pins grounded
$I_{OD}$	Output Leakage Circuit Current	74F		3.75	$\mu\text{A}$	0.0	$V_{IOD} = 150\text{ mV}$ All other pins grounded
$I_{IL}$	Input LOW Current			-0.6	mA	Max	$V_{IN} = 0.5\text{V}$ (CER, CES, CPR, CPS)
				-1.2			$V_{IN} = 0.5\text{V}$ (OEER, OEAS)
$I_{IH} + I_{OZH}$	Output Leakage Current			70	$\mu\text{A}$	Max	$V_{OUT} = 2.7\text{V}$ ( $A_n$ , $B_n$ , PARITY)
$I_{IL} + I_{OZL}$	Output Leakage Current			-650	$\mu\text{A}$	Max	$V_{OUT} = 0.5\text{V}$ ( $A_n$ , $B_n$ , PARITY)
$I_{OS}$	Output Short-Circuit Current		-60	-150	mA	Max	$V_{OUT} = 0\text{V}$ (FR, FS, ERROR, $A_n$ )
			-100	-225			$V_{OUT} = 0\text{V}$ ( $B_n$ , PARITY)
$I_{ZZ}$	Bus Drainage Test			500	$\mu\text{A}$	0.0V	$V_{OUT} = 5.25\text{V}$ ( $A_n$ , $B_n$ , PARITY)
$I_{CCH}$	Power Supply Current		100	150	mA	Max	$V_O = \text{HIGH}$
$I_{CCL}$	Power Supply Current		100	150	mA	Max	$V_O = \text{LOW}$
$I_{CCZ}$	Power Supply Current		110	165	mA	Max	$V_O = \text{HIGH Z}$

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	3.5	6.0	8.0			3.0	9.0	ns	2-3
$t_{PHL}$	CPS or CPR to $A_n$ or $B_n$	4.0	7.0	9.5			3.5	10.5		
$t_{PLH}$	Propagation Delay CPS or CPR to FS or FR	3.0	5.5	7.5			2.5	8.5	ns	2-3
$t_{PHL}$	Propagation Delay $\overline{OEAS}$ to FS	3.5	6.0	8.0			3.0	9.0	ns	2-3
$t_{PLH}$	Propagation Delay	8.0	14.0	18.0			7.0	20.0	ns	2-3
$t_{PHL}$	CPR to Parity	8.5	14.5	18.5			7.5	20.5		
$t_{PLH}$	Propagation Delay	8.0	13.5	17.5			7.0	19.5	ns	2-3
$t_{PHL}$	CPS to ERROR	7.5	13.0	16.5			6.5	18.5		
$t_{PLH}$	Propagation Delay	3.5	6.0	8.0			3.0	9.0	ns	2-3
$t_{PHL}$	$\overline{OEAS}$ to ERROR	3.0	5.0	7.0			2.5	8.0		
$t_{PZH}$	Enable Time $\overline{OEAS}$	3.0	5.5	7.5			2.5	8.5	ns	2-5
$t_{PZL}$	or $\overline{OEER}$ to $B_n$ or $A_n$	3.5	7.0	9.5			3.0	10.5		
$t_{PHZ}$	Disable Time $\overline{OEAS}$	3.0	6.5	8.5			2.5	9.5	ns	2-5
$t_{PLZ}$	or $\overline{OEER}$ to $B_n$ or $A_n$	3.0	5.5	7.5			2.5	8.5		
$t_{PZH}$	Enable Time	3.0	4.5	7.5			2.5	8.5	ns	2-5
$t_{PZL}$	$\overline{OEER}$ to Parity	3.5	6.0	9.5			3.0	10.5		
$t_{PHZ}$	Disable Time	3.0	5.5	8.5			2.5	9.5	ns	2-5
$t_{PLZ}$	$\overline{OEER}$ to Parity	3.0	6.5	7.5			2.5	8.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	7.5				8.5		ns	2-6
$t_s(\text{L})$	$A_n$ or $B_n$ or Parity to CPS or CPR	4.5				5.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0				0		ns	2-6
$t_h(\text{L})$	$A_n$ or $B_n$ or Parity to CPS or CPR	0				0			
$t_s(\text{H})$	Setup, Time HIGH or LOW	6.0				7.0		ns	2-6
$t_s(\text{L})$	CES or CER to CPS or CPR	10.0				11.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0				0		ns	2-4
$t_h(\text{L})$	CES or CER to CPS or CPR	0				0			
$t_w(\text{H})$	Pulse Width, HIGH or LOW	4.0				4.5		ns	2-4
$t_w(\text{L})$	CPS or CPR	6.0				7.0			


**54F/74F563**

## Octal D-Type Latch with TRI-STATE® Outputs

### General Description

The 'F563 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ( $\overline{OE}$ ) inputs.

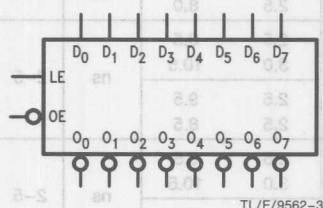
This device is functionally identical to the 'F573, but has inverted outputs.

### Features

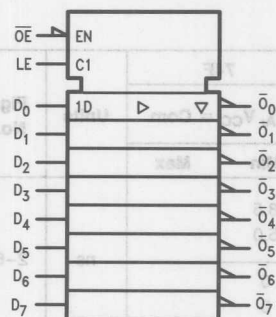
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'F573

**Ordering Code:** See Section 5

### Logic Symbols

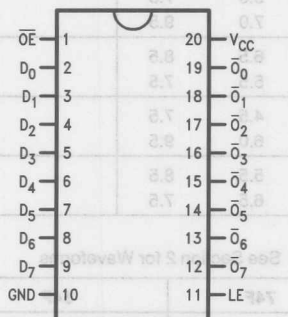


IEEE/IEC



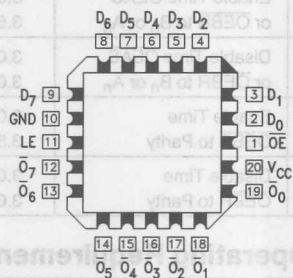
TL/F/9562-5

Pin Assignment for  
DIP, SOIC and Flatpak



TL/F/9562-1

Pin Assignment  
for LCC



TL/F/9562-2

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
D <sub>0</sub> -D <sub>7</sub>	Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
LE	Latch Enable Input (Active HIGH)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{O_0}$ - $\overline{O_7}$	TRI-STATE Latch Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

## Functional Description

The 'F563 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the buffers are in the bi-state mode. When  $\overline{OE}$  is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

### Function Table

Inputs			Internal	Output	Function
$\overline{OE}$	LE	D	Q	O	
H	X	X	X	Z	High Z
H	H	L	H	Z	High Z
H	H	H	L	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	H	H	Transparent
L	H	H	L	L	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level

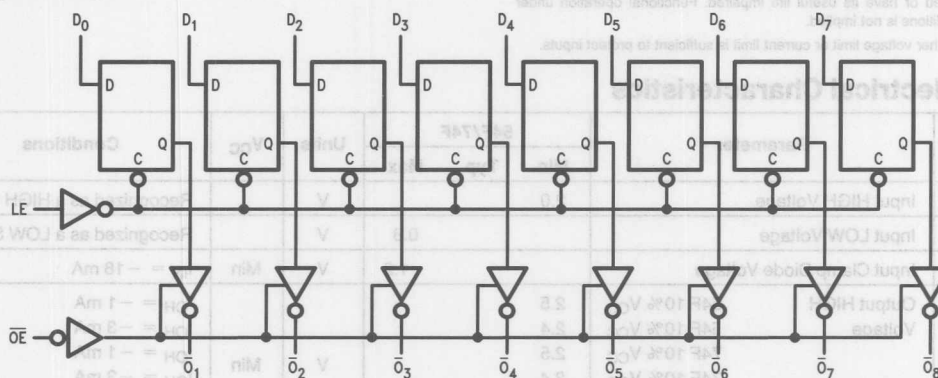
L = LOW Voltage Level

X = Immaterial

Z = High Impedance

NC = No Change

## Logic Diagram



TL/F/9562-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Output LOW Voltage	54F 10% V <sub>CC</sub>	74F 10% V <sub>CC</sub>	0.5	0.5	V	Min	I <sub>OL</sub> = 50 mA I <sub>OL</sub> = 24 mA
Input HIGH Current	54F	74F	20.0	2.0	μA	Max	V <sub>IN</sub> = 2.7V
Input HIGH Current Breakdown Test	54F	74F	100	7.0	μA	Max	V <sub>IN</sub> = 7.0V
Output HIGH Leakage Current	54F	74F	250	20	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
Input Leakage Test	74F	4.75			V	0.0	I <sub>D</sub> = 1.9 μA All Other Pins Grounded
Output Leakage Current	74F	3.75			μA	0.0	V <sub>IC</sub> = 150 mV All Other Pins Grounded
Input LOW Current			-0.8		mA	Max	V <sub>IN</sub> = 0.5V
Output Leakage Current			50		μA	Max	V <sub>OUT</sub> = 2.7V
Output Leakage Current			-50		μA	Max	V <sub>OUT</sub> = 0.5V
Output Short-Circuit Current			-130		mA	Max	V <sub>OUT</sub> = 0V
Bus Drainage Test			500		μA		V <sub>OUT</sub> = 2.5V
Power Supply Current			40	61	mA	Max	V <sub>O</sub> = LOW
Power Supply Current			40	61	mA	Max	V <sub>O</sub> = HIGH Z



## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output	−0.5V to +5.5V
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCL</sub>	Power Supply Current		40	61	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		40	61	mA	Max	V <sub>O</sub> = HIGH Z

## Recommended Operating Conditions

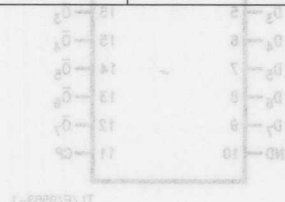
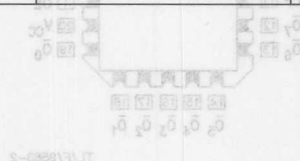
Free Air Ambient Temperature	−55°C to +125°C
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	3.5		8.5	3.0	10.5	3.0	9.5	ns	2-3
$t_{PHL}$	$D_n$ to $\bar{O}_n$	2.5		6.5	2.0	7.5	2.0	7.0		
$t_{PLH}$	Propagation Delay	4.5		9.5	4.0	11.0	4.0	10.5	ns	2-3
$t_{PHL}$	LE to $\bar{O}_n$	3.0		7.0	2.5	7.5	2.5	7.0		
$t_{PZH}$	Output Enable Time	2.0		7.5	2.0	9.5	2.0	9.0	ns	2-5
$t_{PZL}$		3.0		8.5	2.5	10.0	1.5	9.5		
$t_{PHZ}$	Output Disable Time	1.5		5.5	1.5	7.0	1.5	6.5	ns	2-5
$t_{PLZ}$		1.5		5.5	1.5	5.5	1.5	5.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	2.0		2.0		2.0		ns	2-6
$t_s(\text{L})$	$D_n$ to LE	2.0		2.0		2.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	3.0		3.0		3.0		ns	2-6
$t_h(\text{L})$	$D_n$ to LE	3.0		3.0		3.0			
$t_w(\text{H})$	LE Pulse Width, HIGH	4.0		4.0		4.0		ns	2-4



Pin Names	Description	U.L.	Input/Output
$\bar{O}_0 - \bar{O}_7$	TRI-STATE Outputs	1.0/1.0	Output
$\bar{O}_E$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	Input
$\bar{C}_P$	Clock Pulse Input (Active Rising Edge)	1.0/1.0	Input
$D_0 - D_7$	Data Inputs	1.0/1.0	Input


**54F/74F564**

## Octal D-Type Flip-Flop with TRI-STATE® Outputs

### General Description

The 'F564 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ( $\overline{OE}$ ). The information presented to the D inputs is sorted in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

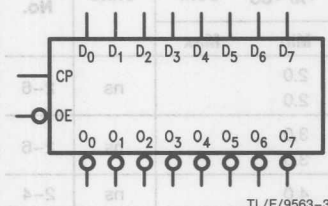
This device is functionally identical to the 'F574, but has inverted outputs.

### Features

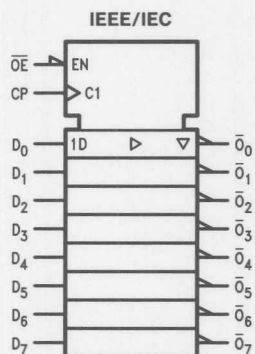
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'F574
- TRI-STATE outputs for bus-oriented applications

### Ordering Code: See Section 5

### Logic Symbols



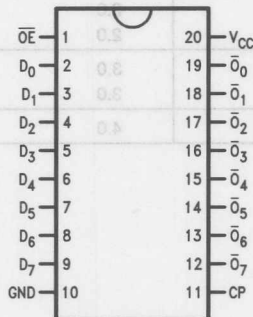
TL/F/9563-3



TL/F/9563-6

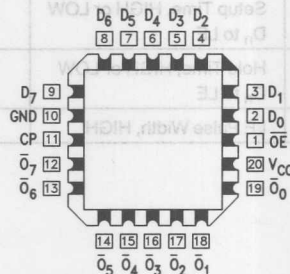
### Connection Diagrams

#### Pin Assignment for DIP, SOIC and Flatpak



TL/F/9563-1

#### Pin Assignment for LCC



TL/F/9563-2

### Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$D_0$ - $D_7$	Data Inputs	1.0/1.0	20 $\mu$ A / -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A / -0.6 mA
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A / -0.6 mA
$\overline{O}_0$ - $\overline{O}_7$	TRI-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

## Functional Description

The 'F564 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

### Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	$\nearrow$	L	H	Z	Load
H	$\nearrow$	H	L	Z	Load
L	$\nearrow$	L	H	H	Data Available
L	$\nearrow$	H	L	L	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level

L = LOW Voltage Level

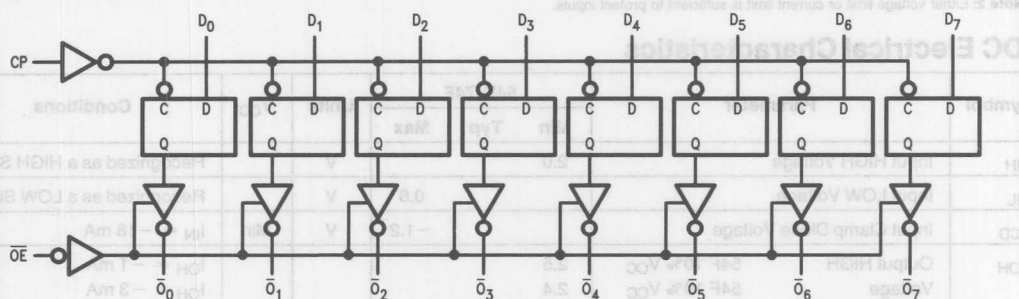
X = Immaterial

Z = High Impedance

$\nearrow$  = LOW-to-HIGH Transition

NC = No Change

## Logic Diagram



TL/F/9563-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = -3 mA
		74F% 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA
		74F% 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = -3 mA
		74F% 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
		74F% 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			-50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCZ</sub>	Power Supply Current		55	86	mA	Max	V <sub>O</sub> = HIGH Z

## Recommended Operating Conditions

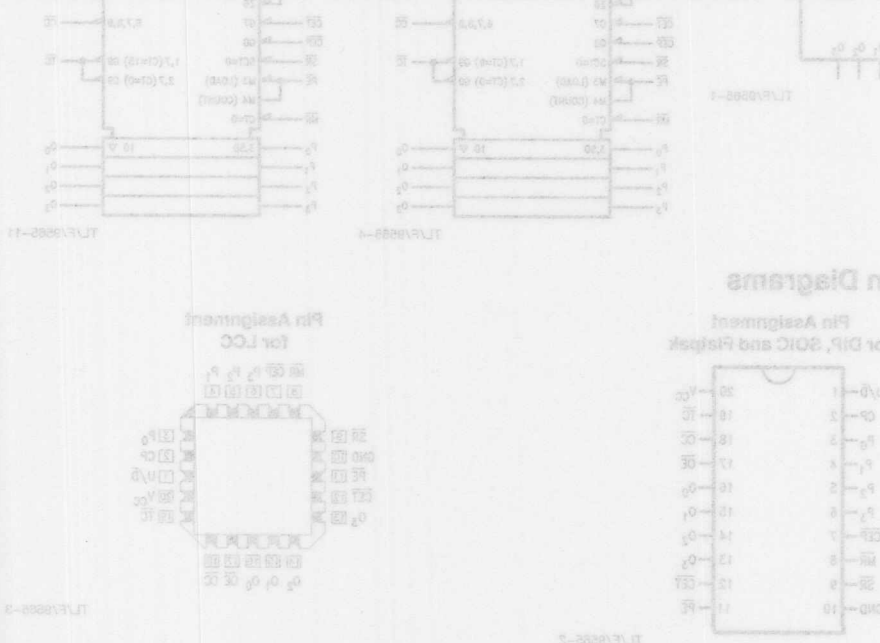
Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	100			60		70		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	2.5	5.2	8.5	2.5	9.5	2.5	8.5	ns	2-3
$t_{\text{PHL}}$	CP to $\overline{O}_n$	2.5	5.9	8.5	2.5	9.5	2.5	8.5		
$t_{\text{PZH}}$	Output Enable Time	3.0	5.6	9.0	2.5	10.5	2.5	10.0		
$t_{\text{PZL}}$		3.0	6.2	9.0	2.5	10.5	2.5	10.0	ns	2-5
$t_{\text{PHZ}}$	Output Disable Time	1.5	3.4	5.5	1.5	7.0	1.5	6.5		
$t_{\text{PLZ}}$		1.5	2.7	5.5	1.5	7.0	1.5	6.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	2.0		2.5		2.0		ns	2-6
$t_s(\text{L})$	$D_n$ to CP	2.5		3.0		2.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0		2.0		2.0		ns	2-4
$t_h(\text{L})$	$D_n$ to CP	2.0		2.0		2.0			
$t_w(\text{H})$	CP Pulse Width	5.0		5.0		5.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	5.0		5.0		5.0			







## 54F/74F568 • 54F/74F569

### 4-Bit Bidirectional Counters with TRI-STATE® Outputs

#### General Description

The 'F568 and 'F569 are fully synchronous, reversible counters with TRI-STATE outputs. The 'F568 is a BCD decade counter; the 'F569 is a binary counter. They feature preset capability for programmable operation, carry lookahead for easy cascading, and a U/D input to control the direction of counting. For maximum flexibility there are both synchronous and master asynchronous reset inputs as well as both Clocked Carry (CC) and Terminal Count (TC) outputs. All state changes except Master Reset are initiated by the rising edge of the clock. A HIGH signal on the Output Enable

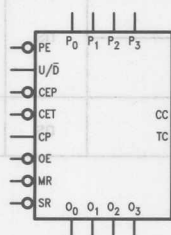
( $\overline{OE}$ ) input forces the output buffers into the high impedance state but does not prevent counting, resetting or parallel loading.

#### Features

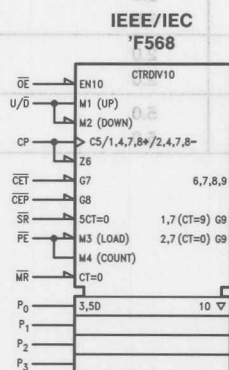
- Synchronous counting and loading
- Lookahead carry capability for easy cascading
- Preset capability for programmable operation
- TRI-STATE outputs for bus organized systems

#### Ordering Code: See Section 5

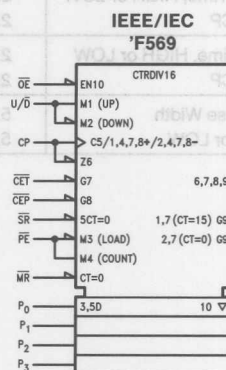
#### Logic Symbols



TL/F/9565-1



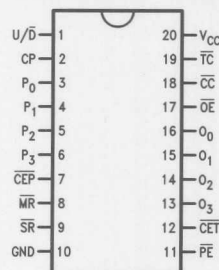
TL/F/9565-4



TL/F/9565-11

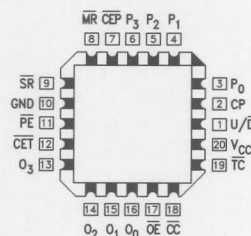
#### Connection Diagrams

Pin Assignment  
for DIP, SOIC and Flatpak



TL/F/9565-2

Pin Assignment  
for LCC



TL/F/9565-3

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$P_0-P_3$	Parallel Data Inputs	1.0/1.0	20 $\mu$ A/−0.6 mA
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	1.0/1.0	20 $\mu$ A/−0.6 mA
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	1.0/1.0	20 $\mu$ A/−1.2 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/−0.6 mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/−1.2 mA
U/ $\overline{D}$	Up/Down Count Control Input	1.0/1.0	20 $\mu$ A/−0.6 mA
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/−0.6 mA
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0	20 $\mu$ A/−0.6 mA
$\overline{SR}$	Synchronous Reset Input (Active LOW)	1.0/1.0	20 $\mu$ A/−0.6 mA
$Q_0-Q_3$	TRI-STATE Parallel Data Outputs	150/40(33.3)	−3 mA/24 mA (20 mA)
$\overline{TC}$	Terminal Count Output (Active LOW)	50/33.3	−1 mA/20 mA
$\overline{CC}$	Clocked Carry Output (Active LOW)	50/33.3	−1 mA/20 mA

## Functional Description

The 'F568 counts modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) it will increment to 0 (LLLL) in the Up mode; in Down mode it will decrement from 0 to 9. The 'F569 counts in the modulo-16 binary sequence. From state 15 it will increment to state 0 in the Up mode; in the Down mode it will decrement from 0 to 15. The clock inputs of all flip-flops are driven in parallel through a clock buffer. All state changes (except due to Master Reset) occurs synchronously with the LOW-to-HIGH transition of the Clock Pulse (CP) input signal.

The circuits have five fundamental modes of operation, in order of precedence: asynchronous reset, synchronous reset, parallel load, count and hold. Five control inputs—Master Reset ( $\overline{MR}$ ), Synchronous Reset ( $\overline{SR}$ ), Parallel Enable ( $\overline{PE}$ ), Count Enable Parallel ( $\overline{CEP}$ ) and Count Enable Trickle ( $\overline{CET}$ )—plus the Up/Down ( $U/\overline{D}$ ) input, determine the mode of operation, as shown in the Mode Select Table. A LOW signal on  $\overline{MR}$  overrides all other inputs and asynchronously forces the flip-flop Q outputs LOW. A LOW signal on  $\overline{SR}$  overrides counting and parallel loading and allows the Q outputs to go LOW on the next rising edge of CP. A LOW signal on  $\overline{PE}$  overrides counting and allows information on the Parallel Data ( $P_n$ ) inputs to be loaded into the flip-flops on the next rising edge of CP. With  $\overline{MR}$ ,  $\overline{SR}$  and  $\overline{PE}$  HIGH,  $\overline{CEP}$  and  $\overline{CET}$  permit counting when both are LOW. Conversely, a HIGH signal on either  $\overline{CEP}$  or  $\overline{CET}$  inhibits counting.

The 'F568 and 'F569 use edge-triggered flip-flops and changing the SR, PE, CEP, CET or U/D inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count ( $\overline{TC}$ ) output is normally HIGH and goes LOW providing  $\overline{CET}$  is LOW, when the

counter reaches zero in the Down mode, or reaches maximum (9 for the 'F568, 15 for the 'F569) in the Up mode.  $\overline{TC}$  will then remain LOW until a state change occurs, whether by counting or presetting, or until  $U/\overline{D}$  or  $\overline{CET}$  is changed. To implement synchronous multistage counters, the connections between the  $\overline{TC}$  output and the  $\overline{CEP}$  and  $\overline{CET}$  inputs can provide either slow or fast carry propagation.

*Figure 1* shows the connections for simple ripple carry, in which the clock period must be longer than the CP to  $\overline{\text{TC}}$  delay of the first stage, plus the cumulative  $\overline{\text{CET}}$  to  $\overline{\text{TC}}$  delays of the intermediate stages, plus the  $\overline{\text{CET}}$  to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in *Figure 2* are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle takes 10 ('F568) or 16 ('F569) clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to  $\overline{\text{TC}}$  delay of the first stage plus the  $\overline{\text{CEP}}$  to CP setup time of the last stage. The  $\overline{\text{TC}}$  output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters. For such applications, the Clocked Carry ( $\overline{\text{CC}}$ ) output is provided. The  $\overline{\text{CC}}$  output is normally HIGH. When  $\overline{\text{CEP}}$ ,  $\overline{\text{CET}}$ , and  $\overline{\text{TC}}$  are LOW, the  $\overline{\text{CC}}$  output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again, as shown in the  $\overline{\text{CC}}$  Truth Table. When the Output Enable ( $\overline{\text{OE}}$ ) is LOW, the parallel data outputs  $\text{O}_0\text{--}\text{O}_3$  are active and follow the flip-flop Q outputs. A HIGH signal on  $\overline{\text{OE}}$  forces  $\text{O}_0\text{--}\text{O}_3$  to the High Z state but does not prevent counting, loading or resetting.

## Logic Equations

Count Enable =  $\overline{CEP} \cdot \overline{CET} \cdot PE$

Up ('F568):  $\overline{TC} = Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3 \cdot (Up) \cdot \overline{CET}$

('F569):  $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (Up) \cdot \overline{CET}$

Down (Both):  $\overline{TC} = Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3 \cdot (Down) \cdot \overline{CET}$

## CC Truth Table

Inputs						Output
SR	PE	CEP	CET	TC*	CP	CC
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	H	X	X	X	H
X	X	X	H	X	X	H
X	X	X	X	H	X	H
H	H	L	L	L	L	L

\*TC is generated internally

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

$\overline{L}$  = HIGH-to-LOW-to-HIGH Clock Transition

## Mode Select Table

Inputs						Operating Mode
MR	SR	PE	CEP	CET	U/D	
L	X	X	X	X	X	Asynchronous Reset
H	H	X	X	X	X	Synchronous Reset
H	L	L	X	X	X	Parallel Load
H	H	H	H	X	X	Hold
H	H	H	X	H	X	Hold
H	H	H	L	L	H	Count Up
H	H	H	L	L	L	Count Down

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

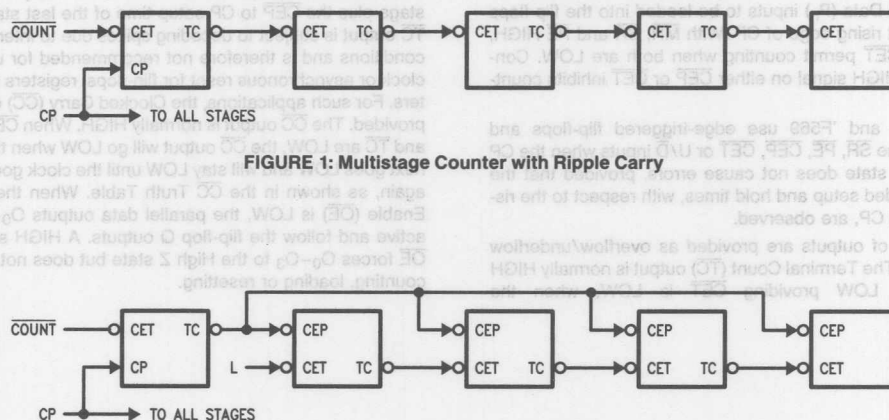


FIGURE 1: Multistage Counter with Ripple Carry

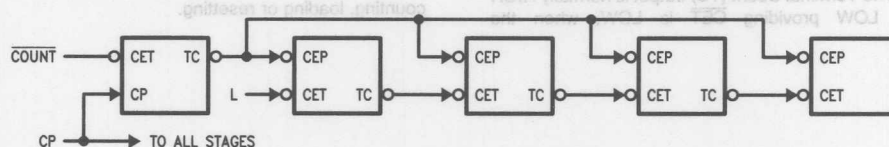
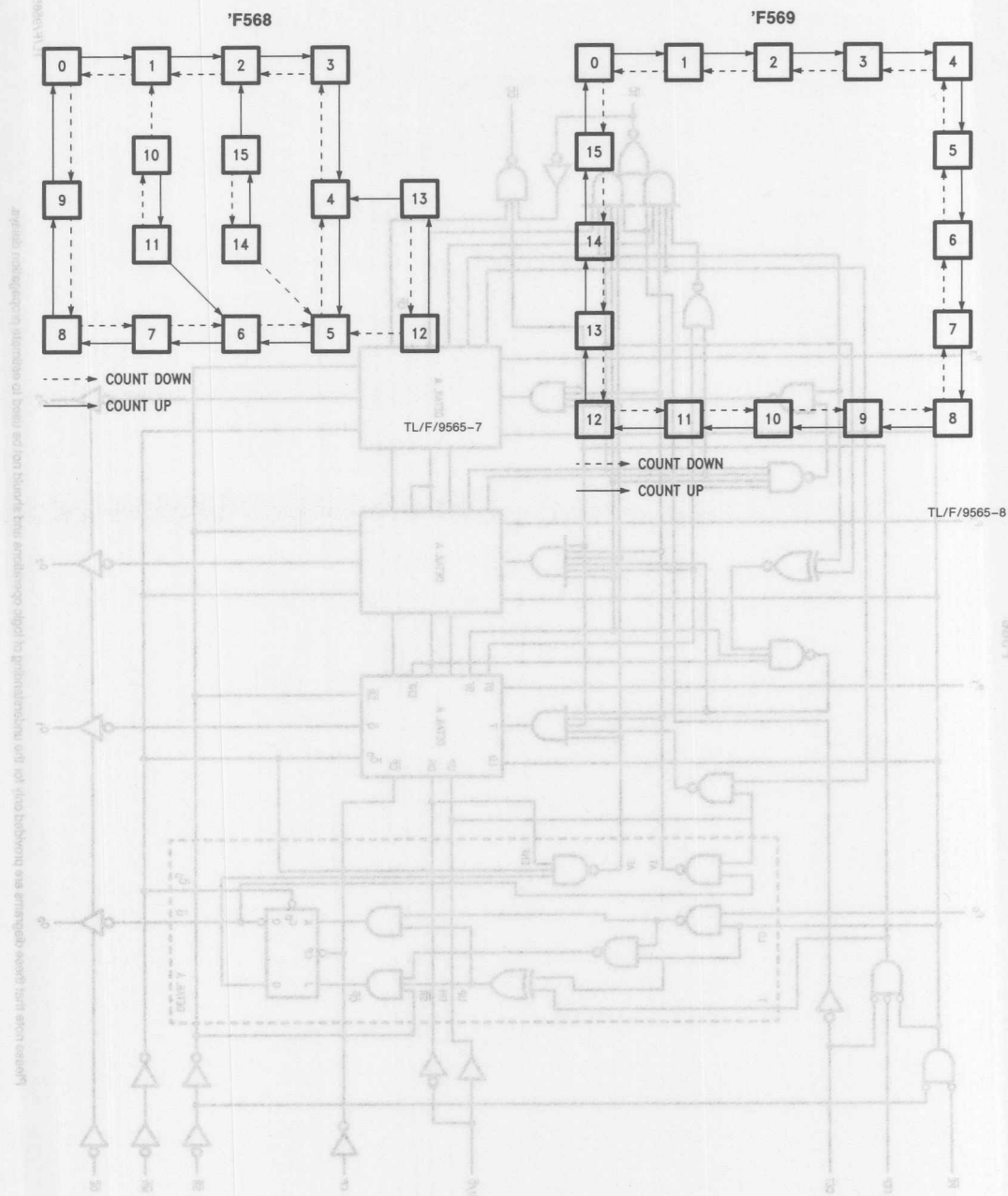


FIGURE 2: Multistage Counter with Lookahead Carry

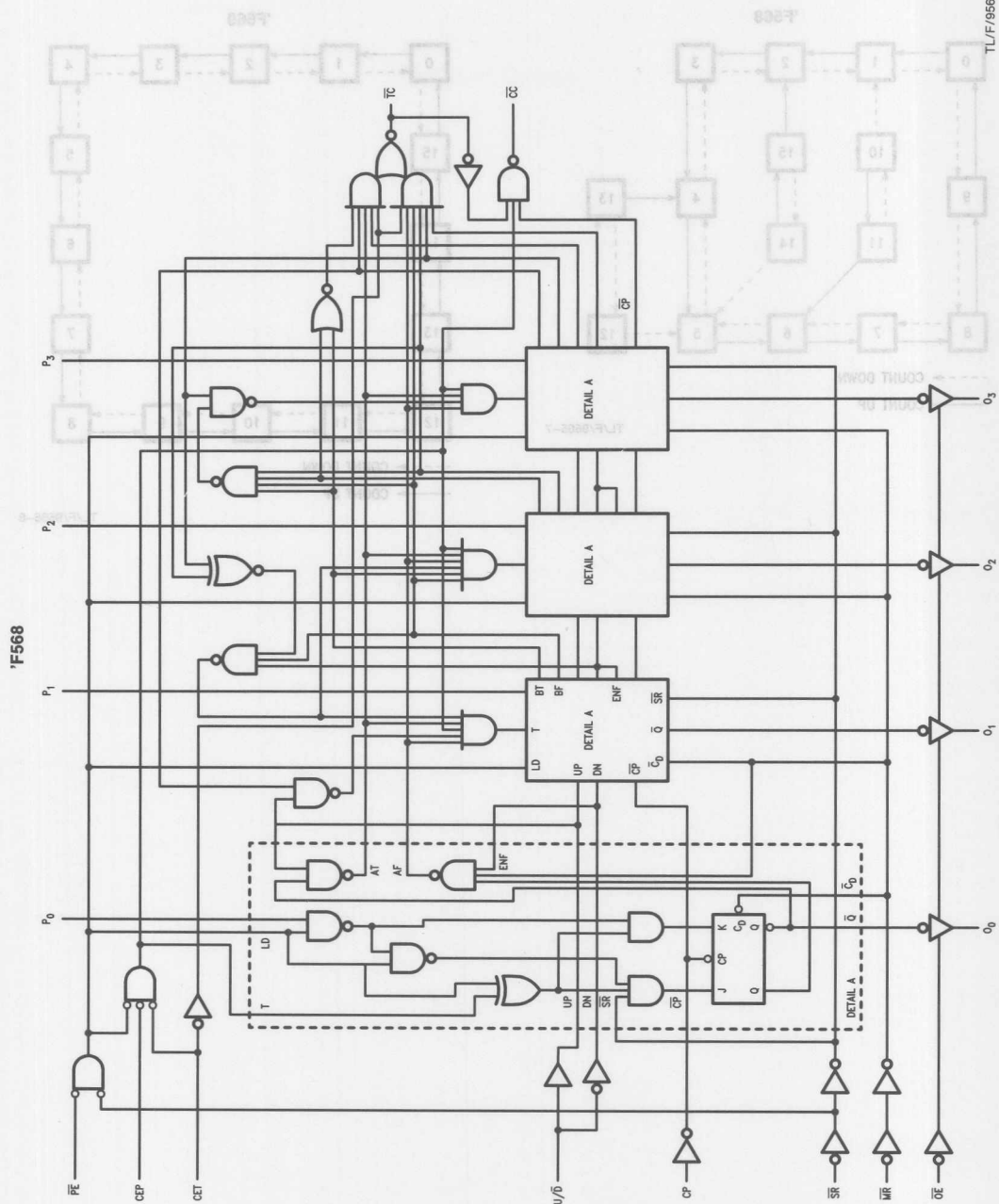
# State Diagrams

Logic Diagrams

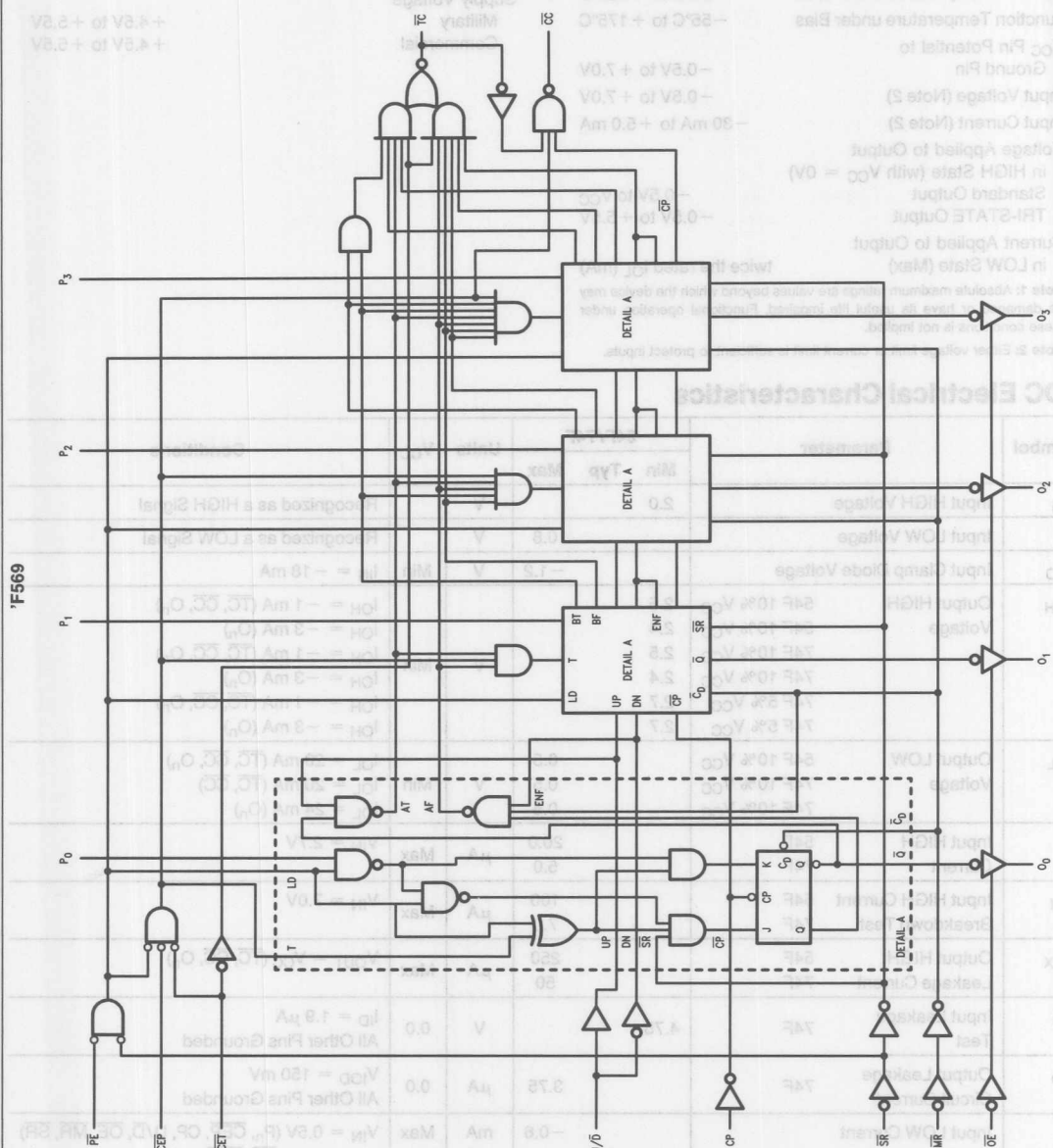
568 • 569



## Logic Diagrams



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA ( $\overline{TC}$ , $\overline{CC}$ , O <sub>n</sub> )
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = -3 mA (O <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA ( $\overline{TC}$ , $\overline{CC}$ , O <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = -3 mA (O <sub>n</sub> )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA ( $\overline{TC}$ , $\overline{CC}$ , O <sub>n</sub> )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -3 mA (O <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA ( $\overline{TC}$ , $\overline{CC}$ , O <sub>n</sub> )
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA ( $\overline{TC}$ , $\overline{CC}$ )
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA (O <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub> ( $\overline{TC}$ , $\overline{CC}$ , O <sub>n</sub> )
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V (P <sub>n</sub> , $\overline{CEP}$ , CP, U/D, $\overline{OE}$ , $\overline{MR}$ , $\overline{SR}$ )
				-1.2	mA	Max	V <sub>IN</sub> = 0.5V (PE, $\overline{CET}$ )

# DC Electrical Characteristic (Continued)

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V (O <sub>n</sub> )
I <sub>OZL</sub>	Output Leakage Current			-50	μA	Max	V <sub>OUT</sub> = 0.5V (O <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V (T <sub>C</sub> , C <sub>C</sub> , O <sub>n</sub> )
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V (O <sub>n</sub> )
I <sub>CCH</sub>	Power Supply Current		45	67	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		45	67	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		45	67	mA	Max	V <sub>O</sub> = HIGH Z

## 'F568

### AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	100	115				90		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	3.0	6.5	8.5			3.0	9.5	ns	2-3
$t_{\text{PHL}}$	CP to $O_n$ (PE HIGH or LOW)	4.0	9.0	11.5			4.0	13.0		
$t_{\text{PLH}}$	Propagation Delay	5.5	12.0	15.5			5.5	17.5	ns	2-3
$t_{\text{PHL}}$	CP to $\overline{\text{TC}}$	4.0	8.5	11.0			4.0	12.5		
$t_{\text{PLH}}$	Propagation Delay	2.5	4.5	6.0			2.5	7.0	ns	2-3
$t_{\text{PHL}}$	$\overline{\text{CET}}$ to $\overline{\text{TC}}$	2.5	6.0	8.0			2.5	9.0		
$t_{\text{PLH}}$	Propagation Delay	3.5	8.5	11.0			3.5	12.5	ns	2-3
$t_{\text{PHL}}$	U/ $\overline{\text{D}}$ to $\overline{\text{TC}}$	4.0	12.5	16.0			4.0	18.0		
$t_{\text{PLH}}$	Propagation Delay	2.5	5.5	7.0			2.5	8.0	ns	2-3
$t_{\text{PHL}}$	CP to $\overline{\text{CC}}$	2.0	4.5	6.0			2.0	7.0		
$t_{\text{PLH}}$	Propagation Delay	2.5	5.0	6.5			2.5	7.5	ns	2-3
$t_{\text{PHL}}$	$\overline{\text{CEP}}, \overline{\text{CET}}$ to $\overline{\text{CC}}$	4.0	8.5	11.0			4.0	12.5		
$t_{\text{PHL}}$	Propagation Delay	5.0	10.0	13.0			5.0	14.5	ns	2-3
$t_{\text{pZH}}$	Output Enable Time	2.5	5.5	7.0			2.5	8.0	ns	2-5
$t_{\text{pZL}}$	$\overline{\text{OE}}$ to $O_n$	3.0	6.0	8.0			3.0	9.0		
$t_{\text{PHZ}}$	Output Disable Time	1.5	5.0	6.5			1.5	7.5		
$t_{\text{PLZ}}$	$\overline{\text{OE}}$ to $O_n$	2.0	4.5	6.0			2.0	7.0		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	4.0				4.5		ns	2-6
$t_s(\text{L})$	$P_n$ to CP	4.0				4.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	3.0				3.5			
$t_h(\text{L})$	$P_n$ to CP	3.0				3.5			
$t_s(\text{H})$	Setup Time, HIGH or LOW	5.0				6.0		ns	2-6
$t_s(\text{L})$	$\overline{\text{CEP}}$ or $\overline{\text{CET}}$ to CP	5.0				6.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0				0			
$t_h(\text{L})$	$\overline{\text{CEP}}$ or $\overline{\text{CET}}$ to CP	0				0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	8.0				9.0		ns	2-6
$t_s(\text{L})$	$\overline{\text{PE}}$ to CP	8.0				9.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0				0			
$t_h(\text{L})$	$\overline{\text{PE}}$ to CP	0				0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	11.0				12.5		ns	2-6
$t_s(\text{L})$	$\text{U}/\overline{\text{D}}$ to CP	16.0				17.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0				0		ns	2-6
$t_h(\text{L})$	$\text{U}/\overline{\text{D}}$ to CP	0				0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	9.5				10.5		ns	2-6
$t_s(\text{L})$	$\overline{\text{SR}}$ to CP	8.5				9.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0				0		ns	2-6
$t_h(\text{L})$	$\overline{\text{SR}}$ to CP	0				0			
$t_w(\text{H})$	CP Pulse Width, HIGH or LOW	4.0				4.5		ns	2-4
$t_w(\text{L})$		6.0				6.5			
$t_w(\text{L})$	$\overline{\text{MR}}$ Pulse Width, LOW	4.5				5.0		ns	2-4
$t_{\text{rec}}$	$\overline{\text{MR}}$ Recovery Time	6.0				7.0		ns	2-6

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**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	90					70		MHz	2-1
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $O_n$ ( $\overline{\text{PE}}$ HIGH or LOW)	3.0 4.0	6.5 9.0	8.5 11.5			3.0 4.0	9.5 13.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $\overline{\text{TC}}$	5.5 4.0	12.0 8.5	15.5 12.5			5.5 4.0	17.5 13.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay $\overline{\text{CET}}$ to $\overline{\text{TC}}$	2.5 2.5	4.5 6.0	6.5 11.0			2.5 2.5	7.0 12.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay U/ $\overline{\text{D}}$ to $\overline{\text{TC}}$	3.5 4.0	8.5 8.0	11.5 12.0			3.5 4.0	12.5 13.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $\overline{\text{CC}}$	2.5 2.0	5.5 4.5	7.0 6.0			2.0 2.0	8.0 7.0	ns	2-3
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay $\overline{\text{CEP}}, \overline{\text{CET}}$ to $\overline{\text{CC}}$	2.5 4.0	5.0 8.5	6.5 11.0			2.0 4.0	7.5 12.5	ns	2-3
$t_{\text{PHL}}$	Propagation Delay MR to $O_n$	5.0	10.0	13.0			5.0	14.5	ns	2-3
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output Enable Time $\overline{\text{OE}}$ to $O_n$	2.5 3.0	5.5 6.0	8.0 9.0			2.5 3.0	8.5 10.0	ns	2-5
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output Disable Time $\overline{\text{OE}}$ to $O_n$	1.5 2.0	5.0 4.5	7.0 6.0			1.5 2.0	8.0 7.0		

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'F569

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	4.0				4.5		ns	2-6
$t_s(\text{L})$	$P_n$ to CP	4.0				4.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	3.0				3.5		ns	2-6
$t_h(\text{L})$	$P_n$ to CP	3.0				3.5			
$t_s(\text{H})$	Setup Time, HIGH or LOW	7.0				8.0		ns	2-6
$t_s(\text{L})$	$\overline{\text{CEP}}$ or $\overline{\text{CET}}$ to CP	5.0				6.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0				0		ns	2-6
$t_h(\text{L})$	$\overline{\text{CEP}}$ or $\overline{\text{CET}}$ to CP	0.5				0.5			
$t_s(\text{H})$	Setup Time, HIGH or LOW	8.0				9.0		ns	2-6
$t_s(\text{L})$	$\overline{\text{PE}}$ to CP	8.0				9.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0.0				1.0		ns	2-6
$t_h(\text{L})$	$\overline{\text{PE}}$ to CP	0				0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	11.0				12.5		ns	2-6
$t_s(\text{L})$	$\text{U}/\overline{\text{D}}$ to CP	7.0				8.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0				0		ns	2-6
$t_h(\text{L})$	$\text{U}/\overline{\text{D}}$ to CP	0				0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	10.5				11.0		ns	2-6
$t_s(\text{L})$	$\overline{\text{SR}}$ to CP	8.5				9.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0				0		ns	2-6
$t_h(\text{L})$	$\overline{\text{SR}}$ to CP	0				0			
$t_w(\text{H})$	CP Pulse Width, HIGH or LOW	4.0				4.5		ns	2-4
$t_w(\text{L})$		7.0				8.0			
$t_w(\text{L})$	$\overline{\text{MR}}$ Pulse Width, LOW	4.5				6.0		ns	2-4
$t_{\text{rec}}$	$\overline{\text{MR}}$ Recovery Time	6.0				8.0		ns	2-6



## 54F/74F573

### Octal D-Type Latch with TRI-STATE® Outputs

#### General Description

The 'F573 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (OE) inputs.

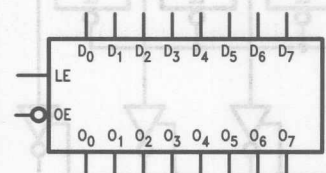
This device is functionally identical to the 'F373 but has different pinouts.

#### Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'F373
- TRI-STATE outputs for bus interfacing
- Guaranteed 4000V minimum ESD protection

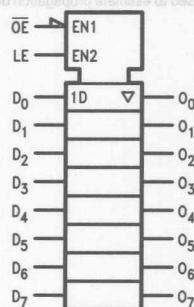
**Ordering Code:** See Section 5

#### Logic Symbol



TL/F/9566-1

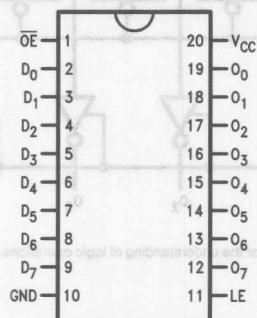
#### IEEE/IEC



TL/F/9566-4

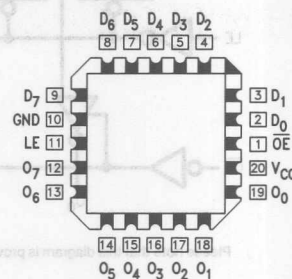
#### Connection Diagrams

##### Pin Assignment for DIP, SOIC and Flatpak



TL/F/9566-2

##### Pin Assignment for LCC



TL/F/9566-3

**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$D_0-D_7$	Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
LE	Latch Enable Input (Active HIGH)	1.0/1.0	20 $\mu$ A/ -0.6 mA
OE	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$O_0-O_7$	TRI-STATE Latch Outputs	150/40(33.3)	-3 mA/24 mA (20 mA)



## Functional Description

The 'F573 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the buffers are in the bi-state mode. When  $\overline{OE}$  is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Function Table

Inputs			Outputs
$\overline{OE}$	LE	D	O
L	H	H	H
L	H	L	L
L	L	X	$O_0$
H	X	X	Z

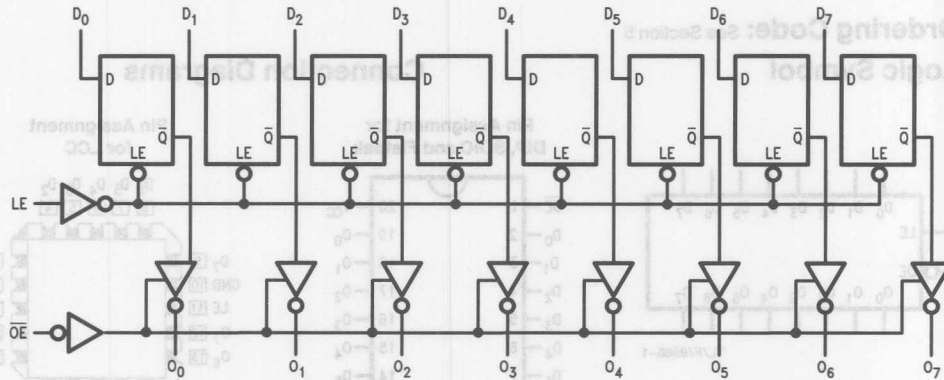
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

$O_0$  = Value stored from previous clock cycle

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

ESD Last Passing Voltage (Min) 4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCL</sub>	Power Supply Current		35	55	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		35	55	mA	Max	V <sub>O</sub> = HIGH Z

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay $D_n$ to $O_n$	3.0	5.3	7.0	3.0	9.0	3.0	8.0	ns	2-3
$t_{PHL}$		2.0	3.7	6.0	2.0	7.0	2.0	6.5		
$t_{PLH}$	Propagation Delay $LE$ to $O_n$	5.0	9.0	11.0	5.0	13.5	5.0	12.0	ns	2-3
$t_{PHL}$		3.0	5.2	7.0	3.0	7.5	3.0	7.0		
$t_{PZH}$	Output Enable Time	2.0	5.0	8.0	2.0	10.0	2.0	9.0	ns	2-5
$t_{PZL}$		2.0	5.6	8.5	2.0	10.0	2.0	9.5		
$t_{PHZ}$	Output Disable Time	1.5	4.5	5.5	1.5	7.0	1.5	6.5		
$t_{PLZ}$		1.5	3.8	5.5	1.5	5.5	1.5	5.5		

## AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	2.0		2.0		2.0		ns	2-6
$t_s(\text{L})$	$D_n$ to LE	2.0		2.0		2.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	3.0		3.0		3.0		ns	2-4
$t_h(\text{L})$	$D_n$ to LE	3.5		4.0		3.5			
$t_w(\text{H})$	LE Pulse Width, HIGH	4.0		4.0		4.0			



## 54F/74F574

### Octal D-Type Flip-Flop with TRI-STATE® Outputs

#### General Description

The 'F574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ( $\overline{OE}$ ). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH (CP) transition.

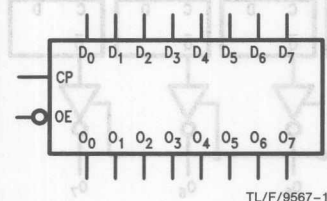
This device is functionally identical to the 'F374 except for the pinouts.

#### Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'F374
- TRI-STATE outputs for bus-oriented applications

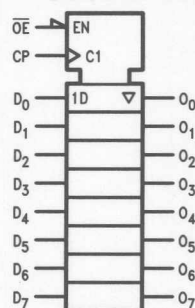
**Ordering Code:** See Section 5

#### Logic Symbols



TL/F/9567-1

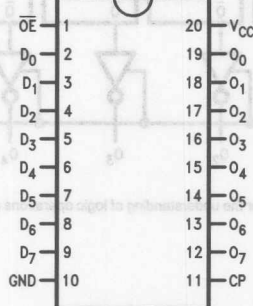
#### IEEE/IEC



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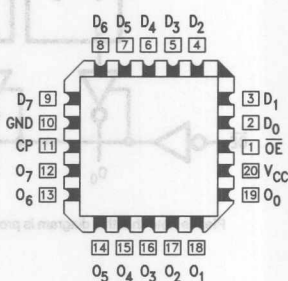
#### Connection Diagrams

##### Pin Assignment for DIP, SOIC and Flatpak



TL/F/9567-2

##### Pin Assignment for LCC



TL/F/9567-3

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
D <sub>0</sub> -D <sub>7</sub>	Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
CP	Clock Pulse Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
O <sub>0</sub> -O <sub>7</sub>	TRI-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

## Functional Description

The 'F574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

### Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	$\nearrow$	L	L	Z	Load
H	$\nearrow$	H	H	Z	Load
L	$\nearrow$	L	L	L	Data Available
L	$\nearrow$	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level

L = LOW Voltage Level

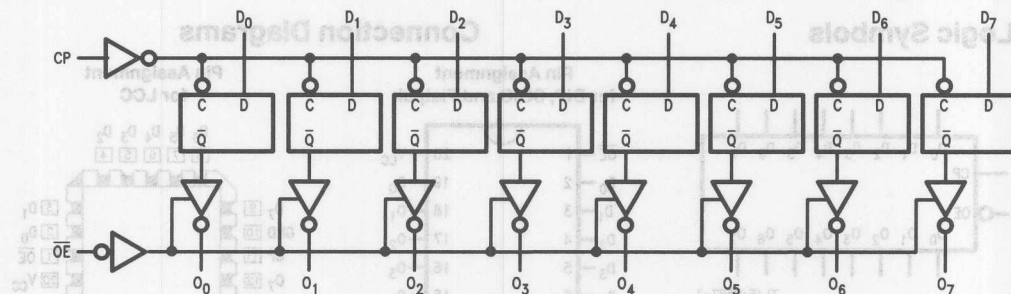
X = Immaterial

Z = High Impedance

$\nearrow$  = LOW-to-HIGH Transition

NC = No Change

## Logic Diagram



TL/F/9567-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Pin Number	Description	U.L.	
		HIGH/LOW	Input (kV <sub>in</sub> ) Output (kV <sub>out</sub> )
D <sub>0</sub> -D <sub>7</sub>	Data inputs	1.0/1.0	20 mA/1.0 - 0.8 mA
CP	Clock Pulse Input (Active LOW)	1.0/1.0	20 mA/1.0 - 0.8 mA
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 mA/1.0 - 0.8 mA
O <sub>0</sub> -O <sub>7</sub>	TRI-STATE Outputs	1.0/1.0 (23.3)	-8 mV/24 mA (20 mA)

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
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Input Voltage (Note 2)	−0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	−30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
---	--------------------------

Standard Output TRI-STATE Output	−0.5V to +5.5V
----------------------------------	----------------

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BI</sub>	Input HIGH Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCZ</sub>	Power Supply Current		55	86	mA	Max	V <sub>O</sub> = HIGH Z



**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$			54F $T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{pF}$		74F $T_A, V_{CC} = \text{Com}$ $C_L = 50\text{pF}$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	100			60		70		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	2.5	5.3	8.5	2.5	9.5	2.5	8.5	ns	2-3
$t_{\text{PHL}}$	CP to $O_n$	2.5	5.3	8.5	2.5	9.5	2.5	8.5		
$t_{\text{PZH}}$	Output Enable Time	3.0	5.5	9.0	2.5	10.5	2.5	10.0	ns	2-5
$t_{\text{PZL}}$		3.0	6.0	9.0	2.5	10.5	2.5	10.0		
$t_{\text{PHZ}}$	Output Disable Time	1.5	3.3	5.5	1.5	7.0	1.5	6.5		
$t_{\text{PLZ}}$		1.5	2.8	5.5	1.5	7.0	1.5	6.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F $T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		54F $T_A, V_{CC} = \text{Mil}$		74F $T_A, V_{CC} = \text{Com}$		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Set-up Time, HIGH or LOW	2.5		3.0		2.5		ns	2-6
$t_s(\text{L})$	$D_n$ to CP	2.0		2.5		2.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0		2.0		2.0		ns	2-4
$t_h(\text{L})$	$D_n$ to CP	2.0		2.0		2.0			
$t_w(\text{H})$	CP Pulse Width	5.0		5.0		5.0		ns	
$t_w(\text{L})$	HIGH or LOW	5.0		5.0		5.0			

100	Power Supply Current		55	88	mA	Max	V <sub>CC</sub> = HIGH V <sub>I</sub> = 0.0V
101	Bus Drainage Test			800	μA	0.0V	V <sub>OUT</sub> = 0.55V
102	Output Short-Circuit Current	-80	-130	mA	Max	V <sub>OUT</sub> = 0V	
103	Output Leakage Current		-80	μA	Max	V <sub>OUT</sub> = 0.5V	
104	Output Leakage Current		80	μA	Max	V <sub>OUT</sub> = 2.7V	
105	Input LOW Current		-0.6	mA	Max	V <sub>IN</sub> = 0.5V	
106	Circuit Current	74F	3.75	μA	0.0	All Other Pins Grounded	V <sub>CC</sub> = 180 mV
107	Input Leakage Test	74F	4.75	μA	0.0	All Other Pins Grounded	I <sub>IN</sub> = 1.8 μA
108	Leakage Current	74F	80	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>	
109	Input HIGH Current	74F	100	μA	Max	V <sub>IN</sub> = 7.0V	
110	Breakdown Test	74F	7.0	μA	Max		
111	Current	74F	8.0	μA	Max	V <sub>IN</sub> = 2.7V	
112	Input HIGH Voltage	74F 102F V <sub>CC</sub>	0.3	V	Min	I <sub>OL</sub> = 24 mA	I <sub>OL</sub> = 20 mA
113	Output LOW Voltage	74F 102F V <sub>CC</sub>	0.3	V	Min		
114	Voltage	74F 52F V <sub>CC</sub> 74F 102F V <sub>CC</sub> 74F 102F V <sub>CC</sub> 74F 102F V <sub>CC</sub> 74F 102F V <sub>CC</sub> 74F 102F V <sub>CC</sub>	2.7 2.7 2.4 2.8 2.4 2.4	V	Min	I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -3 mA	

## 54F/74F579 8-Bit Bidirectional Binary Counter with TRI-STATE® Outputs

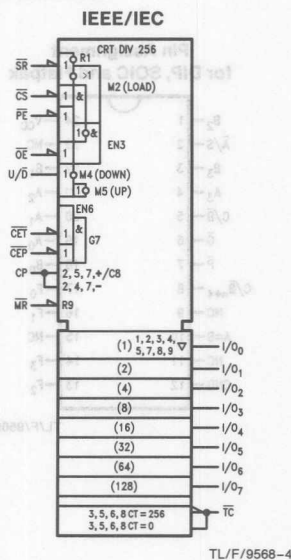
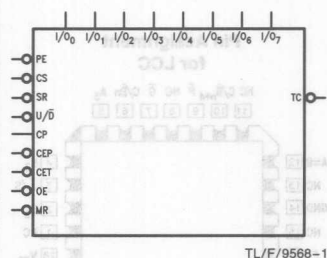
### General Description

The 'F579 is a fully synchronous 8-stage up/down counter with multiplexed TRI-STATE I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry lookahead for easy cascading and a U/D input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

### Features

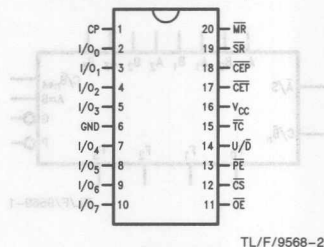
- Multiplexed TRI-STATE I/O ports
- Built-in lookahead carry capability
- Count frequency 100 MHz typ
- Supply current 75 mA typ

### Logic Symbols

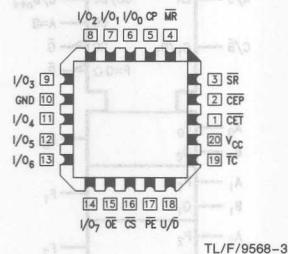


### Connection Diagrams

#### Pin Assignment for DIP, SOIC and Flatpak



#### Pin Assignment for LCC





## 54F/74F582

### 4-Bit BCD Arithmetic Logic Unit

#### General Description

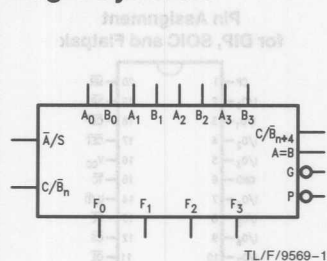
The 'F582 is a 24-pin expandable Arithmetic Logic Unit (ALU) that performs two arithmetic operations (A plus B, A minus B), compare (A equals B), and binary to BCD conversion. In addition to a ripple carry output, carry Propagate (P) and Generate (G) outputs are provided for use with the 'F182 carry lookahead generator for high-speed expansion to higher decades. It is functionally equivalent to the 82S82.

#### Features

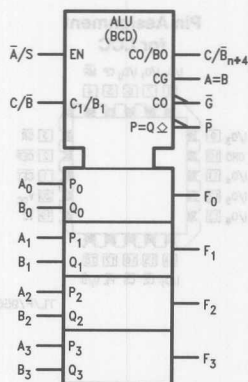
- Performs four BCD functions
- P and G outputs for high-speed expansion
- Add/subtract delay 22 ns max
- Lookahead delay 15.5 ns max
- Supply current 80 mA max
- 24-Lead 300 mil slim package

**Ordering Code:** See Section 5

#### Logic Symbols

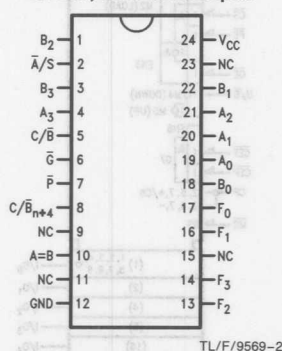


#### IEEE/IEC

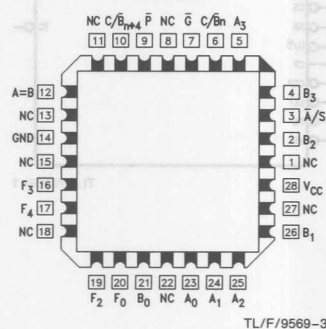


#### Connection Diagrams

##### Pin Assignment for DIP, SOIC and Flatpak



##### Pin Assignment for LCC



# Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
A <sub>0</sub> –A <sub>3</sub>	A Operand Inputs	1.0/2.0	20 $\mu$ A/–1.2 mA
B <sub>0</sub>	B Operand Input	1.0/1.0	20 $\mu$ A/–0.6 mA
B <sub>1</sub>	B Operand Input	1.0/5.0	20 $\mu$ A/–3 mA
B <sub>2</sub>	B Operand Input	1.0/3.0	20 $\mu$ A/–1.8 mA
B <sub>3</sub>	B Operand Input	1.0/2.0	20 $\mu$ A/–1.2 mA
F <sub>0</sub> –F <sub>3</sub>	Functional Outputs	50/33.3	–1 mA/20 mA
A = B	Comparator Output	OC*/33.3	*/20 mA
$\bar{P}$	Carry Propagate Output	50/33.3	–1 mA/20 mA
$\bar{G}$	Carry Generate Output	50/33.3	–1 mA/20 mA
C/ $\bar{B}$	Carry/Borrow Input	1.0/1.0	20 $\mu$ A/–0.6 mA
C/ $\bar{B}_{n+4}$	Carry/Borrow Output	50/33.3	–1 mA/20 mA
$\bar{A}/S$	Add/Subtract	1.0/3.0	20 $\mu$ A/–1.8 mA

\*OC—Open Collector

## Functional Description

The 'F582 Binary Coded Decimal (BCD) Arithmetic Logic Unit (ALU) is a 24-pin expandable unit that performs addition, subtraction, comparison of two numbers, and binary to BCD conversion.

The 'F582's input and output logic includes a Carry/Borrow which is generated internally in the lookahead mode, allowing BCD arithmetic to be computed directly. For more than one BCD decade, the Carry/Borrow term may ripple between 'F582s.

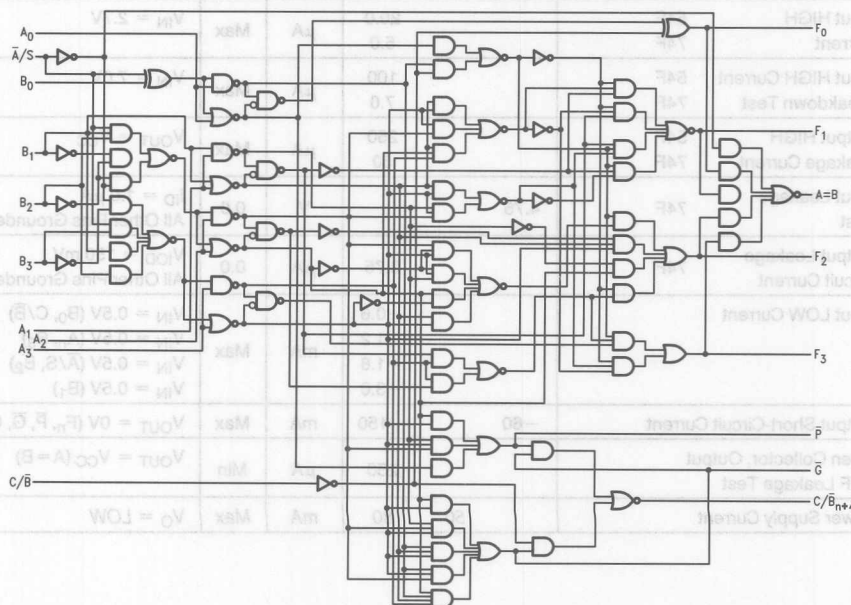
When  $\bar{A}/S$  is LOW, BCD addition is performed ( $A + B + C/\bar{B} = F$ ). If the sum is greater than 9, binary to BCD conversion results at the output.

When  $\bar{A}/S$  is HIGH, subtraction is performed. If the C/ $\bar{B}$  is LOW, then the subtraction is accomplished by internally

computing the 9s complement addition of two BCD numbers ( $A - B - 1 = F$ ). When C/ $\bar{B}$  is HIGH, the difference of the two numbers is figured as  $A - B = F$ . For A greater than or equal to B, the BCD difference appears at the output F in its true form. If A is less than B and C/ $\bar{B}$  is HIGH, the difference appears at the output as the 10s complement of the true form. If A is less than B and C/ $\bar{B}$  is LOW, the 9s complement of the true form appears at the output F. As long as A is less than B, and Active LOW borrow is also generated.

The 'F582 also performs binary to BCD conversion. For inputs between 10 and 15, binary to BCD conversion occurs by grounding the B inputs and applying the binary number to the other set of inputs. This will generate a carry term to the next decade.

## Logic Diagram



TL/F/9569-4

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	-0.5V to V <sub>CC</sub>
Standard Output TRI-STATE® Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

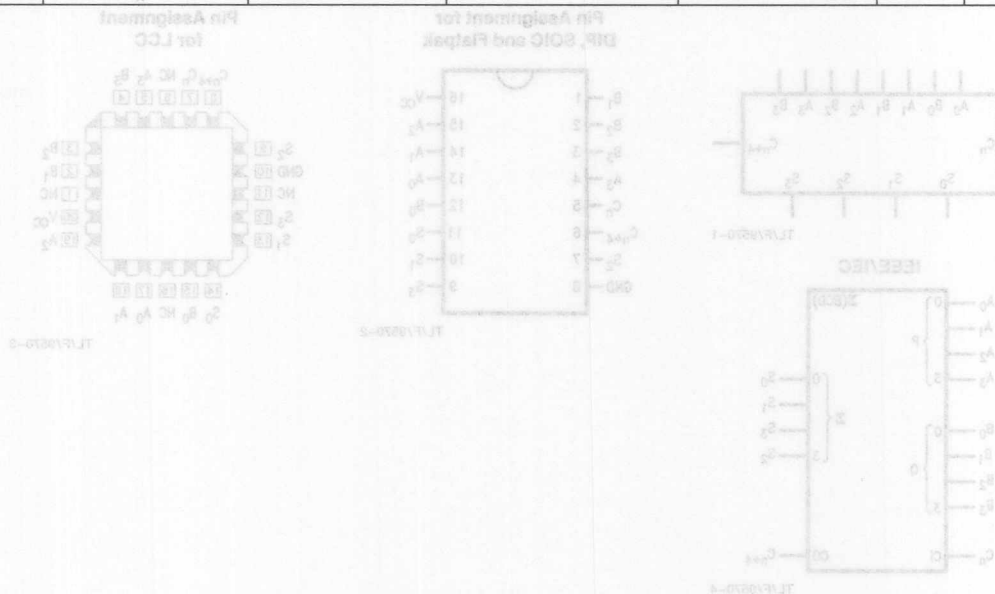
Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA (F <sub>n</sub> , $\bar{P}$ , $\bar{G}$ , C/ $\bar{B}_n + 4$ )
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA (F <sub>n</sub> , $\bar{P}$ , $\bar{G}$ , C/ $\bar{B}_n + 4$ )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA (F <sub>n</sub> , $\bar{P}$ , $\bar{G}$ , C/ $\bar{B}_n + 4$ )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6 -1.2 -1.8 -3.0	mA	Max	V <sub>IN</sub> = 0.5V (B <sub>0</sub> , C/ $\bar{B}$ ) V <sub>IN</sub> = 0.5V (A <sub>n</sub> , B <sub>3</sub> ) V <sub>IN</sub> = 0.5V ( $\bar{A}$ /S, B <sub>2</sub> ) V <sub>IN</sub> = 0.5V (B <sub>1</sub> )
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150			V <sub>OUT</sub> = 0V (F <sub>n</sub> , $\bar{P}$ , $\bar{G}$ , C/ $\bar{B}_n + 4$ )
I <sub>OHC</sub>	Open Collector, Output OFF Leakage Test			250	μA	Min	V <sub>OUT</sub> = V <sub>CC</sub> (A = B)
I <sub>CC</sub>	Power Supply Current		50	80	mA	Max	V <sub>O</sub> = LOW

**Recommended Operating Conditions**

Free Air Ambient Temperature	Military	-55°C to +125°C
	Commercial	0°C to +70°C
Supply Voltage	Military	+4.5V to +5.5V
	Commercial	+4.5V to +5.5V

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n$ or $B_n$ to $F_n$	2.5 2.5	29.0 22.0			2.5 2.5	31.0 23.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n$ or $B_n$ to $C/\overline{B}_{n+4}$	4.0 4.0	21.5 16.0			4.0 4.0	24.0 17.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $C/\overline{B}_n$ to $C/\overline{B}_{n+4}$	3.5 2.0	8.5 6.5			3.0 2.0	9.5 7.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n$ or $B_n$ to $A = B$	8.0 6.0	35.0 25.0			7.5 5.5	28.5 24.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n$ or $B_n$ to $\overline{G}$ or $\overline{P}$	4.0 3.5	18.0 15.5			4.0 3.5	19.0 16.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{A}/S$ to $F_n$	2.5 7.0	33.0 18.0			2.5 6.5	34.0 19.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $C/\overline{B}$ to $F_n$	4.0 2.5	21.0 14.0			3.5 2.5	23.0 15.5	ns	2-3



Unit Loading/Fan Out: See Section 2 for U.L. Definitions

Pin Number	Description	74F14F	
		HIGH/LOW	U.L. Input/Output
$A_0-A_3$	A Output Inputs	1.0/2.0	20 pA/-1.5 mA
$B_0-B_3$	B Output Inputs	1.0/2.0	20 pA/-1.5 mA
$C_n$	Carry Input	1.0/1.0	20 pA/-0.8 mA
$S_0-S_3$	Sum Outputs	20/20.0	-1 mA/20 mA
$C_n+4$	Carry Output	20/20.0	-1 mA/20 mA





## 54F/74F583

### 4-Bit BCD Adder

#### General Description

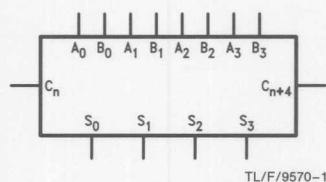
The 'F583 high-speed 4-bit, BCD full adder with internal carry lookahead accepts two 4-bit decimal numbers ( $A_0$ – $A_3$ ,  $B_0$ – $B_3$ ) and a Carry Input ( $C_n$ ). It generates the decimal sum outputs ( $S_0$ – $S_3$ ), and a Carry Output ( $C_{n+4}$ ) if the sum is greater than 9. The 'F583 is the functional equivalent of the 82S83.

#### Features

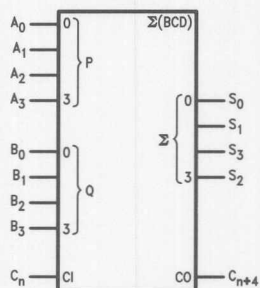
- Adds two decimal numbers
- Full internal lookahead
- Fast ripple carry for economical expansion
- Sum output delay time 16.5 ns max
- Ripple carry delay time 8.5 ns max
- Input to ripple delay time 14.0 ns max
- Supply current 60 mA max
- Available in SOIC, (300 mil only)

**Ordering Code:** See Section 5

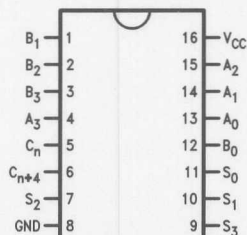
#### Logic Symbols



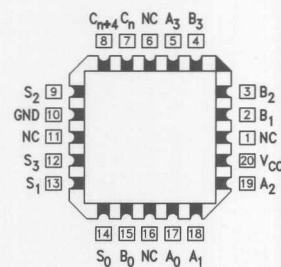
IEEE/IEC



Pin Assignment for  
DIP, SOIC and Flatpak



Pin Assignment  
for LCC



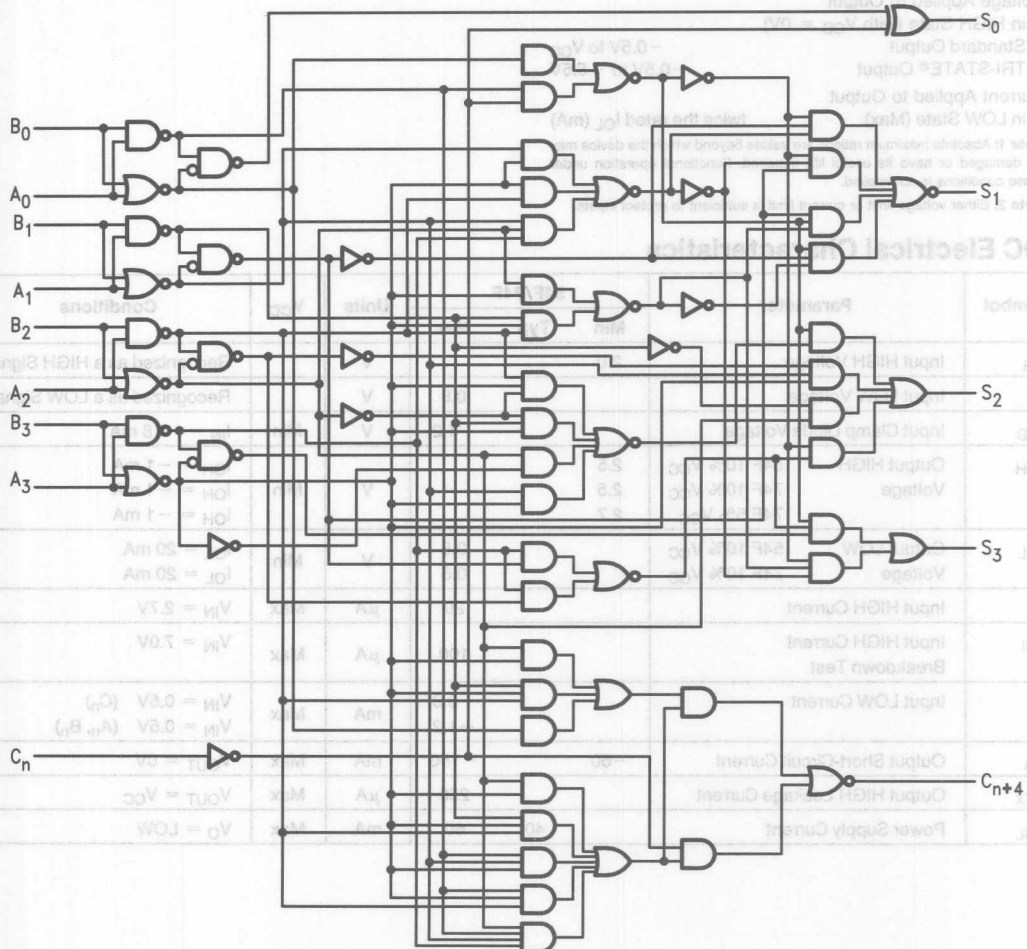
**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_0$ – $A_3$	A Operand Inputs	1.0/2.0	20 $\mu$ A/ –1.2 mA
$B_0$ – $B_3$	B Operand Inputs	1.0/2.0	20 $\mu$ A/ –1.2 mA
$C_n$	Carry Input	1.0/1.0	20 $\mu$ A/ –0.6 mA
$S_0$ – $S_3$	Sum Outputs	50/33.3	–1 mA/20 mA
$C_{n+4}$	Carry Output	50/33.3	–1 mA/20 mA

## Functional Description

The 'F583 4-bit binary coded (BCD) full adder performs the addition of two decimal numbers ( $A_0$ – $A_3$ ,  $B_0$ – $B_3$ ). The look-ahead generates the BCD carry terms internally, allowing the 'F583 to then do BCD addition correctly. For BCD numbers 0 through 9 at A and B inputs, the BCD sum forms at the output. In the addition of two BCD numbers totalling a number greater than 9, a valid BCD number and a carry will result.

## Logic Diagram



TL/F/9570-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

Ambient Temperature under Bias  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Junction Temperature under Bias  $-55^{\circ}\text{C}$  to  $+175^{\circ}\text{C}$

$V_{CC}$  Pin Potential to Ground Pin  $-0.5\text{V}$  to  $+7.0\text{V}$

Input Voltage (Note 2)  $-0.5\text{V}$  to  $+7.0\text{V}$

Input Current (Note 2)  $-30\text{ mA}$  to  $+5.0\text{ mA}$

Voltage Applied to Output

in HIGH State (with  $V_{CC} = 0\text{V}$ )

Standard Output  $-0.5\text{V}$  to  $V_{CC}$

TRI-STATE® Output  $-0.5\text{V}$  to  $+5.5\text{V}$

Current Applied to Output

in LOW State (Max) twice the rated  $I_{OL}$  (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	$V_{CC}$	Conditions
		Min	Typ	Max			
$V_{IH}$	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
$V_{IL}$	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
$V_{CD}$	Input Clamp Diode Voltage			-1.2	V	Min	$I_{IN} = -18\text{ mA}$
$V_{OH}$	Output HIGH Voltage	54F 10% $V_{CC}$	2.5		V	Min	$I_{OH} = -1\text{ mA}$
		74F 10% $V_{CC}$	2.5				$I_{OH} = -1\text{ mA}$
		74F 5% $V_{CC}$	2.7				$I_{OH} = -1\text{ mA}$
$V_{OL}$	Output LOW Voltage	54F 10% $V_{CC}$		0.5	V	Min	$I_{OL} = 20\text{ mA}$
		74F 10% $V_{CC}$		0.5			$I_{OL} = 20\text{ mA}$
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	Max	$V_{IN} = 2.7\text{V}$
$I_{BVI}$	Input HIGH Current Breakdown Test			100	$\mu\text{A}$	Max	$V_{IN} = 7.0\text{V}$
$I_{IL}$	Input LOW Current			-0.6	mA	Max	$V_{IN} = 0.5\text{V}$ ( $C_n$ )
				-1.2			$V_{IN} = 0.5\text{V}$ ( $A_n, B_n$ )
$I_{OS}$	Output Short-Circuit Current	-60		-150	mA	Max	$V_{OUT} = 0\text{V}$
$I_{CEX}$	Output HIGH Leakage Current			250	$\mu\text{A}$	Max	$V_{OUT} = V_{CC}$
$I_{CCL}$	Power Supply Current		40	60	mA	Max	$V_O = \text{LOW}$

## Recommended Operating Conditions

Free Air Ambient Temperature

Military  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Commercial  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$

Supply Voltage

Military  $+4.5\text{V}$  to  $+5.5\text{V}$

Commercial  $+4.5\text{V}$  to  $+5.5\text{V}$

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

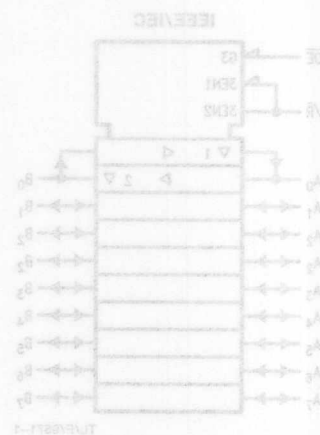
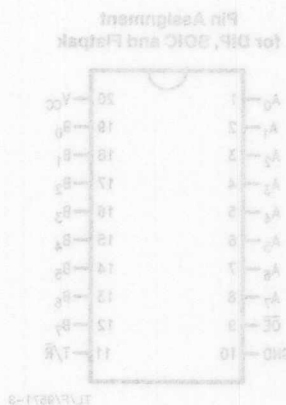
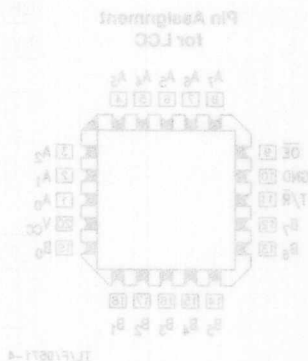
Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	2.5	13.0	16.5	2.5	20.5	2.5	17.5	ns	2-3
$t_{PHL}$	$A_n$ or $B_n$ to $S_n$	2.5	11.0	14.0	2.5	19.0	2.5	15.0		
$t_{PLH}$	Propagation Delay	2.5	6.5	8.5	2.5	10.5	2.5	9.5	ns	2-3
$t_{PHL}$	$C_n$ to $C_{n+4}$	2.5	5.0	6.5	2.5	8.5	2.5	7.5		
$t_{PLH}$	Propagation Delay	4.0	11.0	14.0	4.0	19.5	4.0	15.0	ns	2-3
$t_{PHL}$	$A_n$ or $B_n$ to $C_{n+4}$	4.0	8.0	10.5	4.0	13.5	4.0	11.5		

**Features**

- Non-inverting buffers
- Bidirectional data path
- 8 outputs sink 84 mA (48 mA Mil) source 12 mA
- Guaranteed 4000V minimum ESD protection

specified in this section. The maximum current sinking capability is 84 mA (50 mA Mil) at the A ports and 84 mA (48 mA Mil) at the B ports. The Transceiver (TV) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables

Ordering Code: See Section 5

**Logic Symbols**

**Connection Diagrams**



**54F/74F588**

## Octal Bidirectional Transceiver with TRI-STATE® Inputs/Outputs and IEEE-488 Termination Resistors

### General Description

The 'F588 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. The B ports have termination resistors as specified in the IEEE-488 specifications. Current sinking capability is 24 mA (20 mA Mil) at the A ports and 64 mA (48 mA Mil) at the B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables

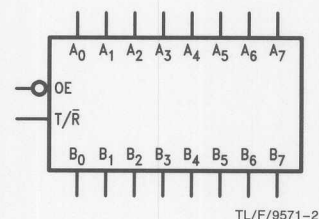
data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a high impedance condition.

### Features

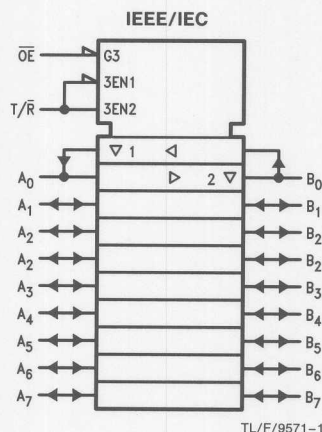
- Non-inverting buffers
- Bidirectional data path
- B outputs sink 64 mA (48 mA Mil), source 12 mA
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

### Logic Symbols



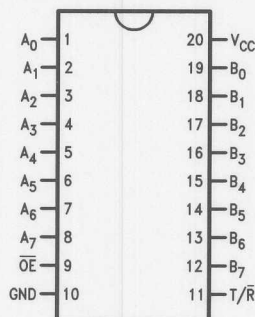
TL/F/9571-2



TL/F/9571-1

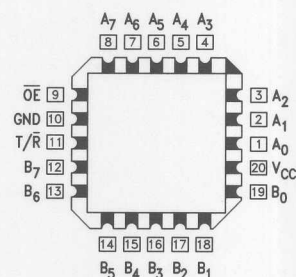
### Connection Diagrams

Pin Assignment  
for DIP, SOIC and Flatpak



TL/F/9571-3

Pin Assignment  
for LCC



TL/F/9571-4

# Unit Loading/Fan Out: See Section 2 for U.L. definitions

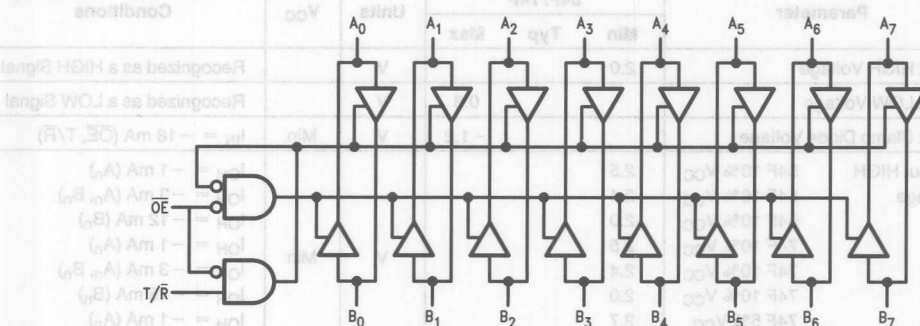
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/2.0	20 $\mu$ A/ -1.2 mA
$T/\overline{R}$	Transmit/Receive Control Input	1.0/2.0	20 $\mu$ A/ -1.2 mA
$A_0$ - $A_7$	A Port Inputs or TRI-STATE Outputs	3.5/1.083	70 $\mu$ A/ -0.65 mA
$B_0$ - $B_7$	B Port Inputs or TRI-STATE Outputs	150/40 (33.3) *T/5.33 600/106.6 (80)	-3 mA/24 mA (20 mA) -3 mA/3.2 mA -12 mA/64 mA (48 mA)

\*T = Resistive Termination per IEEE-488 Standard

## Truth Table

Inputs		Outputs
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Impedance

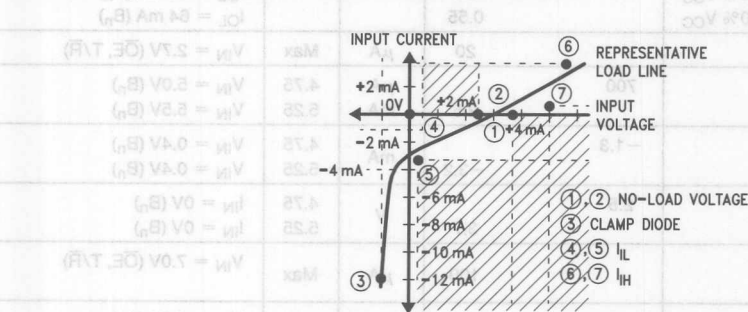
## Logic Diagram



TL/F/9571-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## B Port Input Characteristic with $T/\overline{R}$ LOW



TL/F/9571-6



**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA

Voltage Applied to Output in HIGH State (with V<sub>CC</sub> = 0V)

Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output

in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

ESD Last Passing Voltage (Min) 4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

Truth Table

Outputs	Inputs	
	T/R	OE
Bus B Data to Bus A	L	L
Bus A Data to Bus B	H	L
High Impedance	X	H

**DC Electrical Characteristics**

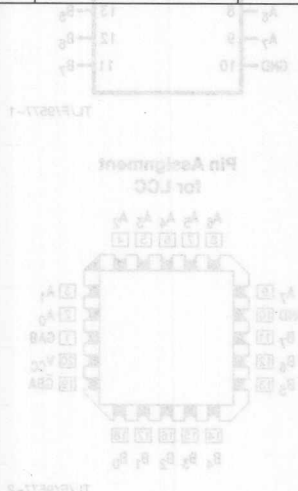
Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA (OE, T/ $\bar{R}$ )
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA (A <sub>n</sub> )
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA (A <sub>n</sub> , B <sub>n</sub> )
		54F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = −12 mA (B <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA (A <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA (A <sub>n</sub> , B <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = −15 mA (B <sub>n</sub> )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA (A <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA (A <sub>n</sub> )
		54F 10% V <sub>CC</sub>		0.55			I <sub>OL</sub> = 48 mA (B <sub>n</sub> )
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA (A <sub>n</sub> )
		74F 10% V <sub>CC</sub>		0.55			I <sub>OL</sub> = 64 mA (B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current			20	μA	Max	V <sub>IN</sub> = 2.7V (OE, T/ $\bar{R}$ )
I <sub>IH</sub> + I <sub>OZH</sub>	I <sub>IH</sub> IEEE-488		700		μA	4.75	V <sub>IN</sub> = 5.0V (B <sub>n</sub> )
				2.5	mA	5.25	V <sub>IN</sub> = 5.5V (B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	I <sub>IL</sub> IEEE-488		−1.3			4.75	V <sub>IN</sub> = 0.4V (B <sub>n</sub> )
				−3.2	mA	5.25	V <sub>IN</sub> = 0.4V (B <sub>n</sub> )
V <sub>NL</sub>	No Load Voltage		2.5		V	4.75	I <sub>IN</sub> = 0V (B <sub>n</sub> )
				3.7		5.25	I <sub>IN</sub> = 0V (B <sub>n</sub> )
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			100	μA	Max	V <sub>IN</sub> = 7.0V (OE, T/ $\bar{R}$ )
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)			1.0	mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> )

**DC Electrical Characteristics** (Continued)

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
I <sub>IL</sub>	Input LOW Current			-1.2	mA	Max	V <sub>IN</sub> = 0.5V ( $\overline{OE}$ , T/ $\overline{R}$ )
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			-650	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current	-60 -100		-150 -225	mA	Max	V <sub>OUT</sub> = 0V (A <sub>n</sub> ) V <sub>OUT</sub> = 0V (B <sub>n</sub> )
I <sub>CEx</sub>	Output HIGH Leakage Current			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub> (A <sub>n</sub> )
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CCH</sub>	Power Supply Current		67	100	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		90	135	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		83	125	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	2.5	4.5	6.0			2.5	7.0	ns	2-3
$t_{PHL}$	A to B or B to A	2.5	5.0	6.5			2.5	7.5		
$t_{PZH}$	Output Enable Time	2.5	5.0	7.0			2.5	8.0	ns	2-5
$t_{PZL}$	T/ $\overline{R}$ or $\overline{OE}$ to A or B	2.5	7.0	9.0			2.5	10.0		
$t_{PHZ}$	Output Disable Time	2.5	5.5	7.0			2.5	8.0		
$t_{PLZ}$	T/ $\overline{R}$ or $\overline{OE}$ to A or B	2.5	5.5	7.0			2.5	8.0		



Pin Names	Description	U.L. HIGH/LOW	Input/Output for 74F00
B <sub>0</sub> -B <sub>7</sub>	TRI-STATE Outputs	150/40 (2.2)	-8 mA/64 mA (48 mA)
A <sub>0</sub> -A <sub>7</sub>	TRI-STATE Outputs	150/40 (2.2)	-8 mA/64 mA (48 mA)
G <sub>0</sub> , G <sub>8</sub>	Enable Inputs	1.0/1.0	20 μA/-0.8 mA



## 54F/74F620 • 54F/74F623

### Inverting Octal Bus Transceiver with TRI-STATE® Outputs

#### General Description

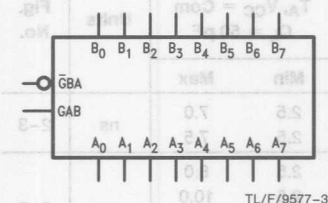
These devices are octal bus transceivers designed for asynchronous two-way data flow between the A and B busses. Both busses are capable of sinking 64 mA and have TRI-STATE outputs. Dual enable pins (GAB,  $\overline{\text{GBA}}$ ) allow data transmission from the A bus to the B bus or from the B bus to the A bus. The 'F620 is an inverting option of the 'F623.

#### Features

- Designed for asynchronous two-way data flow between busses
- Outputs sink 64 mA
- Dual enable inputs control direction of data flow
- Guaranteed 4000V minimum ESD protection
- 'F620 is an inverting option of the 'F623

**Ordering Code:** See Section 5

#### Logic Symbol

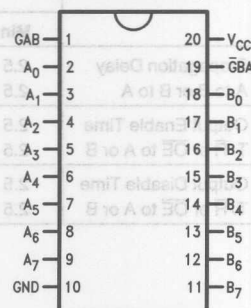


**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{\text{GBA}}$ , GAB	Enable Inputs	1.0/1.0	20 $\mu\text{A}$ / -0.6 mA
$A_0$ - $A_7$	A Inputs or TRI-STATE Outputs	3.5/1.083	70 $\mu\text{A}$ / -0.4 mA
$B_0$ - $B_7$	B Inputs or TRI-STATE Outputs	150/40 (33.3)	-3 mA/64 mA (48 mA)
		3.5/1.083	70 $\mu\text{A}$ / -0.4 mA
		150/40 (33.3)	-3 mA/64 mA (48 mA)

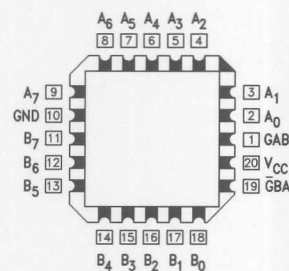
#### Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak



TL/F/9577-1

Pin Assignment  
for LCC



TL/F/9577-2

and GAB low), the outputs are in the high impedance state and data is stored at the A and B busses. When  $\overline{\text{GBA}}$  is

Function Table

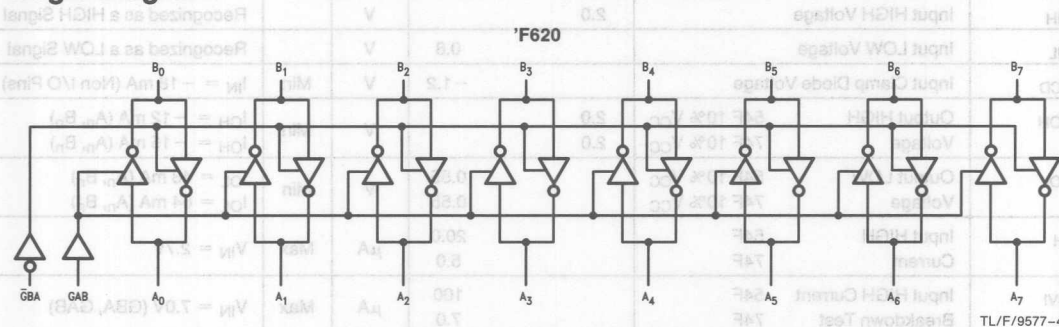
Enable Inputs		Operation	
$\overline{\text{GBA}}$	GAB	'F620	'F623
L	L	$\overline{\text{B}}$ Data to A Bus	B Data to A Bus
H	H	$\overline{\text{A}}$ Data to B Bus	A Data to B Bus
H	L	Z	Z
L	H	$\overline{\text{B}}$ Data to A Bus, $\overline{\text{A}}$ Data to B Bus	B Data to A Bus, A Data to B Bus

H = HIGH Voltage Level

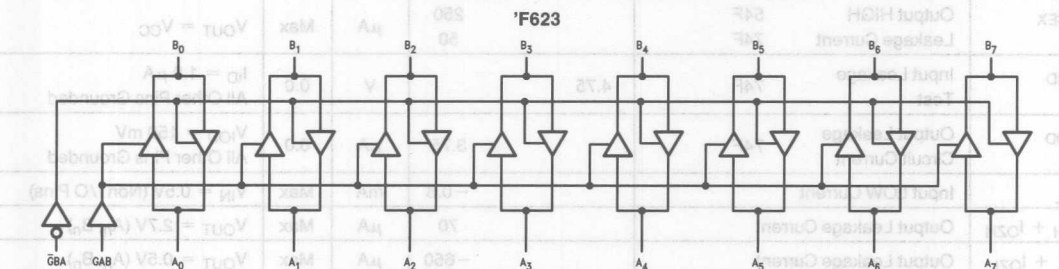
L = LOW Voltage Level

Z = High Impedance

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	–0.5V to V <sub>CC</sub>
Standard Output TRI-STATE Output	–0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)  
ESD Last Passing Voltage (Min) 4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	–55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			–1.2	V	Min	I <sub>IN</sub> = –18 mA (Non I/O Pins)
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.0		V	Min	I <sub>OH</sub> = –12 mA (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OH</sub> = –15 mA (A <sub>n</sub> , B <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.0				
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.55	V	Min	I <sub>OL</sub> = 48 mA (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OL</sub> = 64 mA (A <sub>n</sub> , B <sub>n</sub> )
		74F 10% V <sub>CC</sub>		0.55			
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V (GBA, GAB)
		74F		7.0			
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)	54F		1.0	mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
		74F		0.5			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			–0.6	mA	Max	V <sub>IN</sub> = 0.5V (Non I/O Pins)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			–650	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current		–100	–225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCCH</sub>	Power Supply Current ('F620)			82	mA	Max	V <sub>O</sub> = HIGH, V <sub>IN</sub> = 0.2V
I <sub>CCCL</sub>	Power Supply Current ('F620)			82	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current ('F620)			95	mA	Max	V <sub>O</sub> = HIGH Z
I <sub>CCCH</sub>	Power Supply Current ('F623)			65	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCCL</sub>	Power Supply Current ('F623)			82	mA	Max	V <sub>O</sub> = LOW, V <sub>IN</sub> = 0.2V
I <sub>CCZ</sub>	Power Supply Current ('F623)			85	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	2.5		7.5			2.0	8.0	ns	2-3
$t_{PHL}$	A Input to B Output ('F620)	2.0		7.0			2.0	7.0		
$t_{PLH}$	Propagation Delay	2.5		7.5			2.0	8.0	ns	2-3
$t_{PHL}$	B Input to A Output ('F620)	2.0		7.0			2.0	7.0		
$t_{PLH}$	Propagation Delay	1.5		6.5			1.5	7.5	ns	2-3
$t_{PHL}$	A Input to B Output ('F623)	2.0		7.0			2.0	7.5		
$t_{PLH}$	Propagation Delay	1.5		6.5			1.5	7.5	ns	2-3
$t_{PHL}$	B Input to A Output ('F623)	2.0		7.0			2.0	7.5		
$t_{PZH}$	Enable Time	2.0		7.0			2.0	8.0	ns	2-5
$t_{PZL}$	$\overline{\text{G}}\text{BA Input to A Output}$	2.5		8.0			2.0	8.5		
$t_{PHZ}$	Disable Time	1.5		6.5			1.5	7.5	ns	2-5
$t_{PLZ}$	$\overline{\text{G}}\text{BA Input to A Output}$	1.0		5.5			1.0	5.5		
$t_{PZH}$	Enable Time	2.0		7.5			2.0	8.5	ns	2-5
$t_{PZL}$	GAB Input to B Output ('F620)	3.0		8.0			2.0	8.5		
$t_{PHZ}$	Disable Time	2.5		8.0			2.0	9.0	ns	2-5
$t_{PLZ}$	GAB Input to B Output ('F620)	2.0		7.5			2.0	8.0		
$t_{PZH}$	Enable Time	2.0		7.5			2.0	8.5	ns	2-5
$t_{PZL}$	GAB Input to B Output ('F623)	2.5		8.0			2.0	8.5		
$t_{PHZ}$	Disable Time	2.0		8.0			2.0	9.0	ns	2-5
$t_{PLZ}$	GAB Input to B Output ('F623)	2.0		8.0			2.0	8.0		



Pin Names	Description	U.L.	
		HIGH/LOW	Input/Output
$\overline{\text{CE}}_0 - \overline{\text{CE}}_3$	Check Word Bit Input	3.5/1.083	70 $\mu\text{A}$ - 850 $\mu\text{A}$
$\overline{\text{CE}}_0 - \overline{\text{CE}}_3$	or TRI-STATE Output	150/40 (83.3)	-3 mA/24 mA (50 mA)
$\overline{\text{CE}}_0 - \overline{\text{CE}}_3$	Data Word Bit Input	3.5/1.083	70 $\mu\text{A}$ - 850 $\mu\text{A}$
$\overline{\text{CE}}_0 - \overline{\text{CE}}_3$	or TRI-STATE Output	150/40 (83.3)	-3 mA/24 mA (50 mA)
$\overline{\text{CE}}_0 - \overline{\text{CE}}_3$	Output Enable Data Bits	1.0/1.0	20 $\mu\text{A}$ - 0.5 mA
$\overline{\text{CE}}_0 - \overline{\text{CE}}_3$	Output Latch Enable Data Bit	1.0/1.0	20 $\mu\text{A}$ - 0.5 mA
$\overline{\text{CE}}_0 - \overline{\text{CE}}_3$	Output Enable Check Bit	1.0/1.0	20 $\mu\text{A}$ - 0.5 mA
$\overline{\text{CE}}_0 - \overline{\text{CE}}_3$	Select Pins	1.0/1.0	20 $\mu\text{A}$ - 0.5 mA
$\overline{\text{CE}}_0 - \overline{\text{CE}}_3$	Single Error Flag	50/33.3	-1 mA/20 mA
$\overline{\text{CE}}_0 - \overline{\text{CE}}_3$	Multiple Error Flag	50/33.3	-1 mA/20 mA





## 54F/74F632

### 32-Bit Parallel Error Detection and Correction Circuit

#### General Description

The 'F632 device is a 32-bit parallel error detection and correction circuit (EDAC) in a 52-pin or 68-pin package. The EDAC uses a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDAC to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error

condition of all LOWs or all HIGHs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.

Read-modify-write (byte-control) operations can be performed by using output latch enable, LEDBO, and the individual  $\overline{\text{OEB}}_0$  through  $\overline{\text{OEB}}_3$  byte control pins.

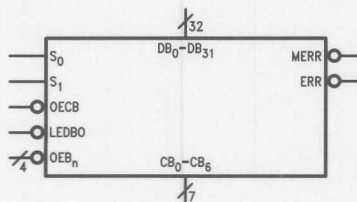
Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the Data Bit and Check Bit input latches. These will determine if the failure occurred in memory or in the EDAC.

#### Features

- Detects and corrects single-bit errors
- Detects and flags dual-bit errors
- Built-in diagnostic capability
- Fast write and read cycle processing times
- Byte-write capability
- Guaranteed 4000V minimum ESD protection

#### Ordering Code: See Section 5

#### Logic Symbol



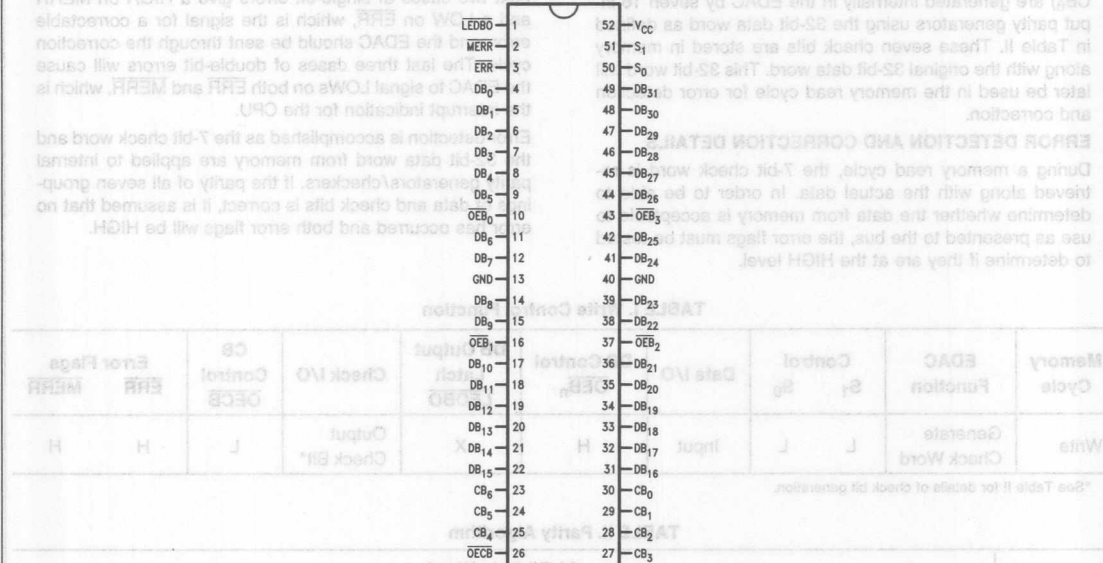
TL/F/9579-1

#### Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\text{CB}_0\text{--}\text{CB}_6$	Check Word Bit, Input or TRI-STATE® Output	3.5/1.083 150/40 (33.3)	70 $\mu\text{A}$ /–650 $\mu\text{A}$ –3 mA/24 mA (20 mA)
$\text{DB}_0\text{--}\text{DB}_{31}$	Data Word Bit, Input or TRI-STATE Output	3.5/1.083 150/40 (33.3)	70 $\mu\text{A}$ /–650 $\mu\text{A}$ –3 mA/24 mA (20 mA)
$\overline{\text{OEB}}_0\text{--}\overline{\text{OEB}}_3$	Output Enable Data Bits	1.0/1.0	20 $\mu\text{A}$ /–0.6 mA
LEDBO	Output Latch Enable Data Bit	1.0/1.0	20 $\mu\text{A}$ /–0.6 mA
OECB	Output Enable Check Bit	1.0/1.0	20 $\mu\text{A}$ /–0.6 mA
$\text{S}_0, \text{S}_1$	Select Pins	1.0/1.0	20 $\mu\text{A}$ /–0.6 mA
ERR	Single Error Flag	50/33.3	–1 mA/20 mA
MERR	Multiple Error Flag	50/33.3	–1 mA/20 mA

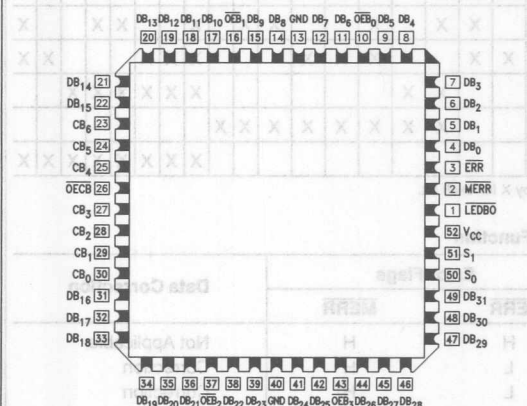
## Connection Diagrams

### Pin Assignment for Side Brazed DIP



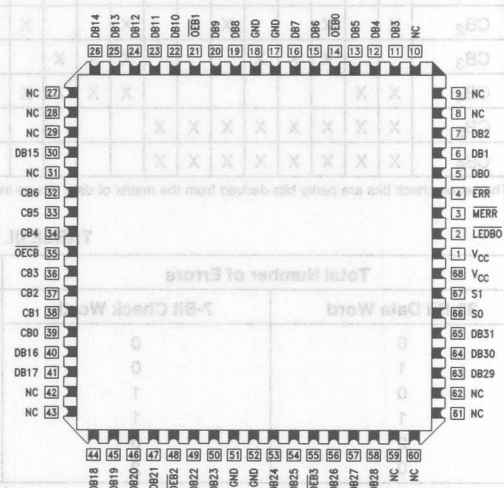
TI / F / 9579-2

### Pin Assignment for LCC and PCC 52-Pin



TL/F/9579-3

### Pin Assignment for LCC and PCC 68-Pin



NC—No internal connection

During a memory write cycle, the seven 16-bit (CB<sub>6</sub>) are generated internally in the EDAC by seven 16-input parity generators using the 32-bit data word as defined in Table II. These seven check bits are stored in memory along with the original 32-bit data word. This 32-bit word will later be used in the memory read cycle for error detection and correction.

#### ERROR DETECTION AND CORRECTION DETAILS

During a memory read cycle, the 7-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from memory is acceptable to use as presented to the bus, the error flags must be tested to determine if they are at the HIGH level.

next two cases of single-bit errors give a HIGH on MERR and a LOW on ERR, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal LOWs on both ERR and MERR, which is the interrupt indication for the CPU.

Error detection is accomplished as the 7-bit check word and the 32-bit data word from memory are applied to internal parity generators/checkers. If the parity of all seven groupings of data and check bits is correct, it is assumed that no error has occurred and both error flags will be HIGH.

TABLE I. Write Control Function

Memory Cycle	EDAC Function	Control S <sub>1</sub> S <sub>0</sub>	Data I/O	DB Control OEB <sub>n</sub>	DB Output Latch LEDBO	Check I/O	CB Control OECS	Error Flags ERR MERR
Write	Generate Check Word	L L	Input	H	X	Output Check Bit*	L	H H

\*See Table II for details of check bit generation.

TABLE II. Parity Algorithm

Check Word Bit	32-Bit Data Word																															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB <sub>0</sub>	X		X	X		X					X		X	X	X			X			X		X	X	X		X					X
CB <sub>1</sub>				X		X		X		X		X		X	X	X				X		X		X		X		X	X	X	X	
CB <sub>2</sub>	X		X			X	X		X			X	X			X	X		X			X	X		X			X	X			X
CB <sub>3</sub>			X	X	X				X	X	X				X	X			X	X	X				X	X	X				X	X
CB <sub>4</sub>	X	X							X	X	X	X	X	X			X	X							X	X	X	X	X	X		
CB <sub>5</sub>	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X								
CB <sub>6</sub>	X	X	X	X	X	X	X	X																	X	X	X	X	X	X	X	X

The seven check bits are parity bits derived from the matrix of data bits as indicated by X for each bit.

TABLE III. Error Function

Total Number of Errors		Error Flags		Data Correction
32-Bit Data Word	7-Bit Check Word	ERR	MERR	
0	0	H	H	Not Applicable
1	0	L	H	Correction
0	1	L	H	Correction
1	1	L	L	Interrupt
2	0	L	L	Interrupt
0	2	L	L	Interrupt

H = HIGH Voltage Level  
L = LOW Voltage Level

## Functional Description (Continued)

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set LOW. Any single error in the 32-bit data word will change the state of either three or five bits of the 7-bit check word. Any single error in the 7-bit check word changes the state of only that one bit. In either case, the single error flag (ERR) will be set LOW while the dual error flag (MERR) will remain HIGH.

Any 2-bit error will change the state of an even number of check bits. The 2-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set LOW when any 2-bit error is detected.

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all LOWs and all HIGHs will be detected.

As the corrected word is made available on the data I/O port (DB<sub>0</sub> through DB<sub>31</sub>), the check word I/O port (CB<sub>0</sub> through CB<sub>6</sub>) presents a 7-bit syndrome error code. This syndrome error code can be used to locate the bad memory chip. See Table V for syndrome decoding.

### READ-MODIFY-WRITE (BYTE CONTROL) OPERATIONS

The 'F632 device is capable of byte-write operations. The 39-bit word from memory must first be latched into the Data Bit and Check Bit input latches. This is easily accomplished by switching from the read and flag mode ( $S_1 = H, S_0 = L$ ) to the latch input mode ( $S_1 = H, S_0 = H$ ). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking LEDBO from a LOW to a HIGH.

Byte control can now be employed on the data word through the  $\overline{OEB}_0$  through  $\overline{OEB}_3$  controls.  $\overline{OEB}_0$  controls DB<sub>0</sub>–DB<sub>7</sub> (byte 0),  $\overline{OEB}_1$  controls DB<sub>8</sub>–DB<sub>15</sub> (byte 1),  $\overline{OEB}_2$  controls DB<sub>16</sub>–DB<sub>23</sub> (byte 2), and  $\overline{OEB}_3$  controls DB<sub>24</sub>–DB<sub>31</sub> (byte 3). Placing a HIGH on the byte control will disable the output and the user can modify the byte. If a LOW is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking controls  $S_1$  and  $S_0$  LOW. Table VI lists the read-modify-write functions.

### DIAGNOSTIC OPERATIONS

The 'F632 is capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control. In the diagnostic mode ( $S_1 = L, S_0 = H$ ), the check word is latched into the input latch while the data input latch remains transparent. This lets the user apply various data words against a fixed known check word. If the user applies a diagnostic data word with an error in any bit location, the ERR flag should be LOW. If a diagnostic data word with two errors in any bit location is applied, the MERR flag should be LOW. After the check word is latched into the input latch, it can be verified by taking  $\overline{OECB}$  LOW. This outputs the latched check word. The diagnostic data word can be latched into the output data latch and verified. By changing from the diagnostic mode ( $S_1 = L, S_0 = H$ ) to the correction mode ( $S_1 = H, S_0 = H$ ), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table VII lists the diagnostic functions.

TABLE IV. Read, Flag and Correct Function

Memory Cycle	EDAC Function	Control $S_1$ $S_0$	Data I/O	DB Control $\overline{OEB}_n$	DB Output Latch LEDBO	Check I/O	CB Control $\overline{OECB}$	Error Flags ERR MERR
Read	Read & Flag	H L	Input	H	X	Input	H	Enabled (Note 1)
Read	Latch Input Data & Check Bits	H H	Latched Input Data	H	L	Latched Input Check Word	H	Enabled (Note 1)
Read	Output Corrected Data & Syndrome Bits	H H	Output Corrected Data Word	L	X	Output Syndrome Bits (Note 2)	L	Enabled (Note 1)

Note 1: See Table III for error description.

Note 2: See Table V for error location.

## Functional Description (Continued)

TABLE V. Syndrome Decoding

Syndrome Bits							Error
6	5	4	3	2	1	0	
L	L	L	L	L	L	L	unc
L	L	L	L	L	L	H	2-Bit
L	L	L	L	L	H	H	2-Bit
L	L	L	L	L	H	H	unc
L	L	L	L	H	L	L	2-Bit
L	L	L	L	H	H	H	unc
L	L	L	L	H	H	L	unc
L	L	L	L	H	H	H	2-Bit (Note 2)
L	L	L	H	L	L	L	2-Bit
L	L	L	H	L	L	H	unc
L	L	L	H	L	H	L	DB <sub>31</sub>
L	L	L	H	L	H	H	2-Bit
L	L	L	H	H	L	L	unc
L	L	L	H	H	L	H	2-Bit
L	L	L	H	H	H	L	2-Bit
L	L	L	H	H	H	H	DB <sub>30</sub>
L	L	H	L	L	L	L	2-Bit
L	L	H	L	L	L	H	unc
L	L	H	L	L	H	L	DB <sub>29</sub>
L	L	H	L	L	H	H	2-Bit
L	L	H	H	L	L	L	DB <sub>28</sub>
L	L	H	H	L	L	H	2-Bit
L	L	H	H	L	H	L	2-Bit
L	L	H	H	L	H	H	DB <sub>27</sub>
L	L	H	H	L	L	L	DB <sub>26</sub>
L	L	H	H	L	L	H	2-Bit
L	L	H	H	L	L	H	2-Bit
L	L	H	H	L	H	L	DB <sub>25</sub>
L	L	H	H	L	H	H	2-Bit
L	L	H	H	H	L	L	2-Bit
L	L	H	H	H	L	H	DB <sub>24</sub>
L	L	H	H	H	H	L	unc
L	L	H	H	H	H	H	2-Bit

CB<sub>X</sub> = Error in check bit XDB<sub>Y</sub> = Error in data bit Y

2-Bit = Double-bit error

unc = Uncorrectable multi-bit error

**Note:** 2-bit and unc condition will cause both ERR and MERR to be LOW.**Note 1:** Syndrome bits for all LOWs. MERR and ERR LOW for all LOWs, only ERR LOW for DB<sub>30</sub> error.**Note 2:** Syndrome bits for all HIGHs.

## Functional Description (Continued)

TABLE V. Syndrome Decoding (Continued)

Syndrome Bits							Error
6	5	4	3	2	1	0	
H	L	L	L	L	L	L	2-Bit
H	L	L	L	L	L	H	unc
H	L	L	L	L	H	L	unc
H	L	L	L	L	H	H	2-Bit
H	L	L	L	H	L	L	unc
H	L	L	L	H	L	H	2-Bit
H	L	L	L	H	H	L	2-Bit
H	L	L	L	H	H	H	unc
H	L	L	H	L	L	L	unc
H	L	L	H	L	L	H	2-Bit
H	L	L	H	L	H	L	2-Bit
H	L	L	H	L	H	H	DB <sub>15</sub>
H	L	L	H	H	L	L	2-Bit
H	L	L	H	H	L	H	unc
H	L	L	H	H	H	L	DB <sub>14</sub>
H	L	L	H	H	H	H	2-Bit
H	L	H	L	L	L	L	unc
H	L	H	L	L	L	H	2-Bit
H	L	H	L	L	H	L	2-Bit
H	L	H	L	L	H	H	DB <sub>13</sub>
H	L	H	L	H	L	L	2-Bit
H	L	H	L	H	L	H	DB <sub>12</sub>
H	L	H	L	H	H	L	DB <sub>11</sub>
H	L	H	L	H	H	H	2-Bit
H	L	H	H	L	L	L	2-Bit
H	L	H	H	L	L	H	DB <sub>10</sub>
H	L	H	H	L	H	L	DB <sub>9</sub>
H	L	H	H	L	H	H	2-Bit
H	L	H	H	H	L	L	DB <sub>8</sub>
H	L	H	H	H	L	H	2-Bit
H	L	H	H	H	H	L	2-Bit
H	L	H	H	H	H	H	CB <sub>5</sub>

Syndrome Bits							Error
6	5	4	3	2	1	0	
H	H	L	L	L	L	L	unc
H	H	L	L	L	L	H	2-Bit
H	H	L	L	L	H	L	2-Bit
H	H	L	L	L	H	H	DB <sub>23</sub>
H	H	L	L	H	L	L	2-Bit
H	H	L	L	H	L	H	DB <sub>22</sub>
H	H	L	L	H	H	L	DB <sub>21</sub>
H	H	L	L	H	H	H	2-Bit
H	H	L	H	L	L	L	2-Bit
H	H	L	H	L	L	H	DB <sub>20</sub>
H	H	L	H	L	H	L	DB <sub>19</sub>
H	H	L	H	L	H	H	2-Bit
H	H	L	H	H	L	L	DB <sub>18</sub>
H	H	L	H	H	L	H	2-Bit
H	H	L	H	H	H	L	2-Bit
H	H	L	H	H	H	H	CB <sub>4</sub>
H	H	H	L	L	L	L	2-Bit
H	H	H	L	L	L	H	DB <sub>16</sub>
H	H	H	L	L	H	L	unc
H	H	H	L	L	H	H	2-Bit
H	H	H	L	H	L	L	DB <sub>17</sub>
H	H	H	L	H	L	H	2-Bit
H	H	H	L	H	H	L	2-Bit
H	H	H	L	H	H	H	CB <sub>3</sub>
H	H	H	H	L	L	L	unc (Note 1)
H	H	H	H	L	L	H	2-Bit
H	H	H	H	L	H	L	2-Bit
H	H	H	H	L	H	H	CB <sub>2</sub>
H	H	H	H	H	L	L	2-Bit
H	H	H	H	H	L	H	CB <sub>1</sub>
H	H	H	H	H	H	L	CB <sub>0</sub>
H	H	H	H	H	H	H	None

CB<sub>x</sub> = Error in check bit XDB<sub>y</sub> = Error in data bit Y

2-Bit = Double-bit error

unc = Uncorrectable multi-bit error

**Note:** 2-bit and unc condition will cause both ERR and MERR to be LOW**Note 1:** Syndrome bits for all LOWs. MERR and ERR LOW for all LOWs, only ERR LOW for DB<sub>30</sub> error.**Note 2:** Syndrome bits for all HIGHs.



## Functional Description (Continued)

TABLE VI. Read-Modify-Write Function\*

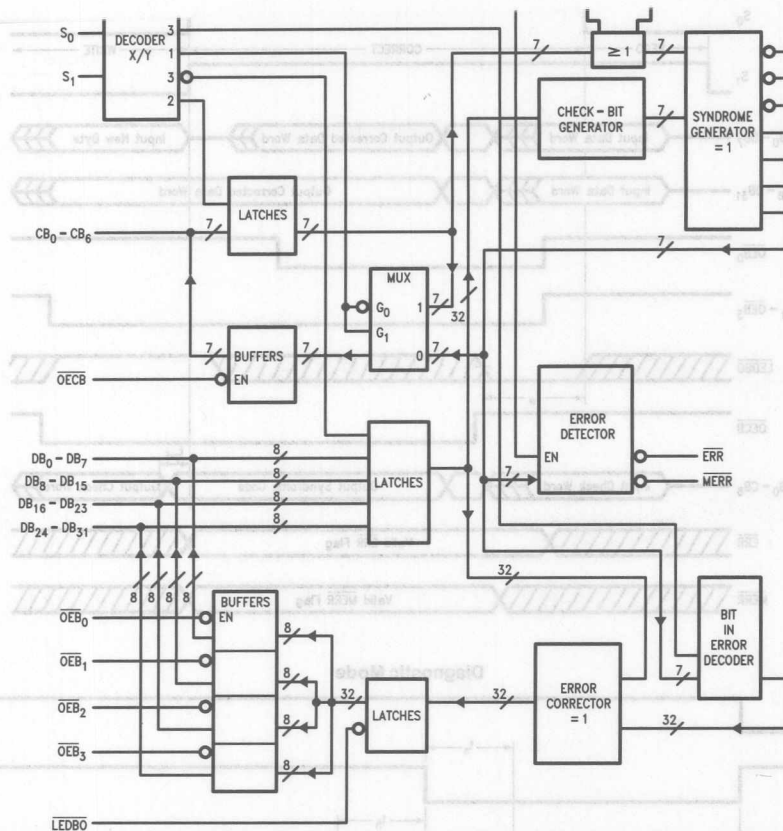
Memory Cycle	EDAC Function	Control S <sub>1</sub>	Control S <sub>0</sub>	BYTEn*	OEEn*	DB Output Latch LEDBO	Check I/O	CB Control OECB	Error Flags ERR MERR
Read	Read & Flag	H	L	Input	H	X	Input	H	Enabled
Read	Latch Input Data & Check Bits	H	H	Latched Input Data	H	L	Latched Input Check Word	H	Enabled
Read	Latch Corrected Data Word into Output Latch	H	H	Latched Output Data Word	H	H	High Z Output Syndrome Bits	H	Enabled
Modify/Write	Modify Appropriate Byte or Bytes & Generate New Check Word	L	L	Input Modified BYTE <sub>0</sub>	H	H	Output Check Word	L	H H
				Output Unchanged BYTE <sub>0</sub>	L				

\*OEEn controls DB<sub>0</sub>–DB<sub>7</sub> (BYTE<sub>0</sub>); OEEn controls DB<sub>8</sub>–DB<sub>15</sub> (BYTE<sub>1</sub>); OEEn controls DB<sub>16</sub>–DB<sub>23</sub> (BYTE<sub>2</sub>); OEEn controls DB<sub>24</sub>–DB<sub>31</sub> (BYTE<sub>3</sub>).

TABLE VII. Diagnostic Function

EDAC Function	Control S <sub>1</sub>	Control S <sub>0</sub>	Data I/O	DB Byte Control OEEn	DB Output Latch LEDBO	Check I/O	CB Control OECB	Error Flags ERR MERR
Read & Flag	H	L	Input Correct Data Word	H	X	Input Correct Check Bits	H	H
Latch Input Check Word while Data Input Latch Remains Transparent	L	H	Input Diagnostic Data Word*	H	L	Latched Input Check Bits	H	Enabled
Latch Diagnostic Data Word into Output Latch	L	H	Input Diagnostic Data Word*	H	H	Output Latched Check Bits	L	Enabled
						High Z	H	
Latch Diagnostic Data Word into Input Latch	H	H	Latched Input Diagnostic Data Word	H	H	Output Syndrome Bits	L	Enabled
						High Z	H	
Output Diagnostic Data Word & Syndrome Bits	H	H	Output Diagnostic Data Word	L	H	Output Syndrome Bits	L	Enabled
						High Z	H	
Output Corrected Diagnostic Data Word & Output Syndrome Bits	H	H	Output Corrected Diagnostic Data Word	L	L	Output Syndrome Bits	L	Enabled
						High Z	H	

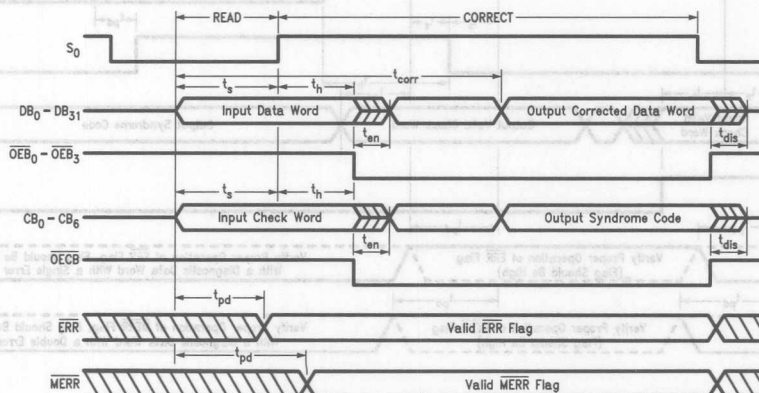
\*Diagnostic data is a data word with an error in one bit location except when testing the MERR error flag. In this case, the diagnostic data word will contain errors in two bit locations.



TL/F/9579-4

## Timing Waveforms

### Read, Flag and Correct Mode

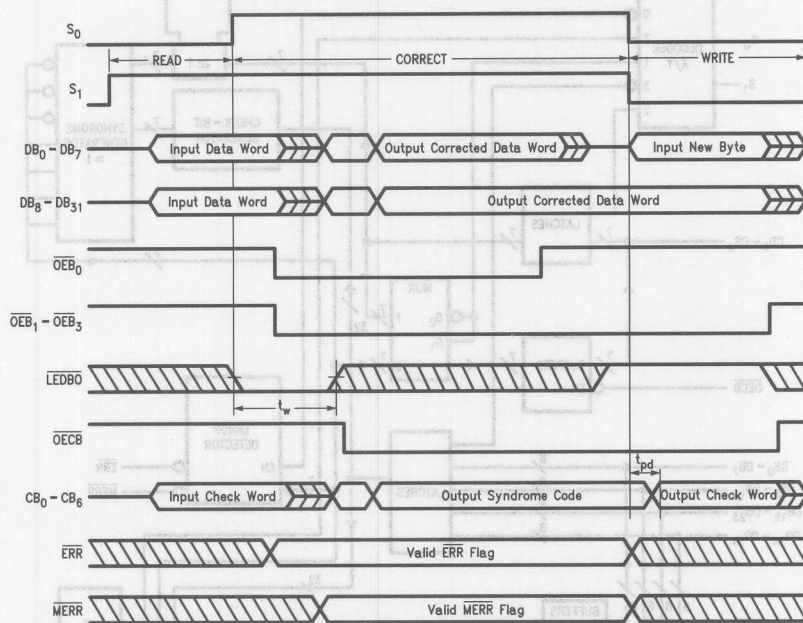


TL/F/9579-5

## Timing Waveforms (Continued)

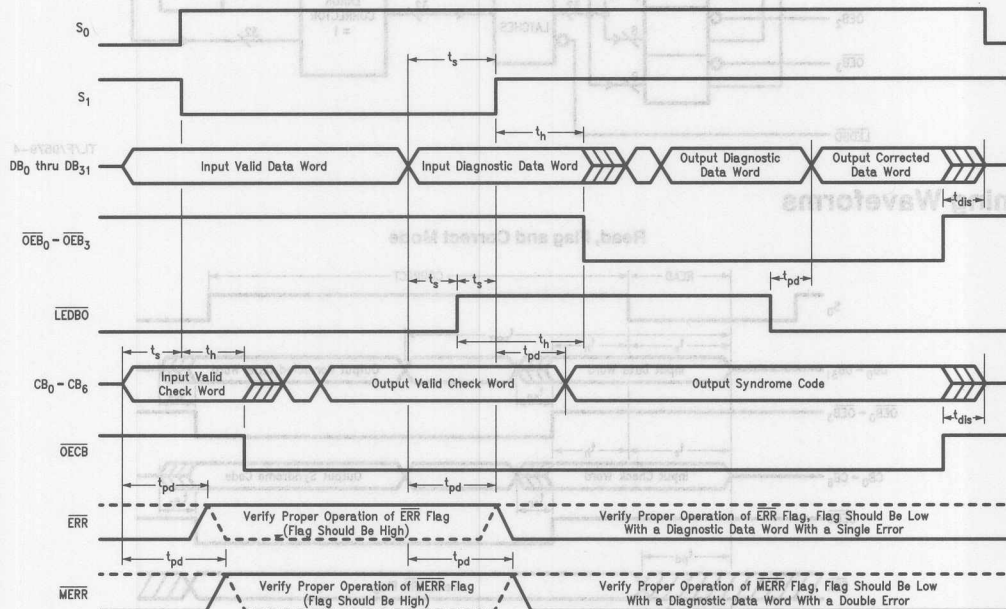
Block Diagram

## Read, Correct and Modify Mode



TL/F/9579-6

## Diagnostic Mode



TL/F/9579-7

# Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

Ambient Temperature under Bias  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Junction Temperature under Bias  $-55^{\circ}\text{C}$  to  $+175^{\circ}\text{C}$

$V_{\text{CC}}$  Pin Potential to Ground Pin  $-0.5\text{V}$  to  $+7.0\text{V}$

Input Voltage (Note 2)  $-0.5\text{V}$  to  $+7.0\text{V}$

Input Current (Note 2)  $-30\text{ mA}$  to  $+5.0\text{ mA}$

Voltage Applied to Output in HIGH State (with  $V_{\text{CC}} = 0\text{V}$ ) Standard Output  $-0.5\text{V}$  to  $V_{\text{CC}}$

TRI-STATE Output  $-0.5\text{V}$  to  $+5.5\text{V}$

Current Applied to Output in LOW State (Max) twice the rated  $I_{\text{OL}}$  (mA)

ESD Last Passing Voltage (Min) 4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature  
Military  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
Commercial  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$

Supply Voltage  
Military  $+4.5\text{V}$  to  $+5.5\text{V}$   
Commercial  $+4.5\text{V}$  to  $+5.5\text{V}$

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	$V_{\text{CC}}$	Conditions
		Min	Typ	Max			
$V_{\text{IH}}$	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
$V_{\text{IL}}$	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
$V_{\text{CD}}$	Input Clamp Diode Voltage			1.2	V	Min	$I_{\text{IN}} = -18\text{ mA}$
$V_{\text{OH}}$	Output HIGH Voltage	54F 10% $V_{\text{CC}}$	2.5		V	Min	$I_{\text{OH}} = -1\text{ mA}$ (ERR, MERR, $\text{DB}_n$ , $\text{CB}_n$ )
		54F 10% $V_{\text{CC}}$	2.4				$I_{\text{OH}} = -3\text{ mA}$ ( $\text{DB}_n$ , $\text{CB}_n$ )
		74F 10% $V_{\text{CC}}$	2.5				$I_{\text{OH}} = -1\text{ mA}$ (ERR, MERR, $\text{DB}_n$ , $\text{CB}_n$ )
		74F 10% $V_{\text{CC}}$	2.4				$I_{\text{OH}} = -3\text{ mA}$ ( $\text{DB}_n$ , $\text{CB}_n$ )
		74F 5% $V_{\text{CC}}$	2.7				$I_{\text{OH}} = -1\text{ mA}$ (ERR, MERR, $\text{DB}_n$ , $\text{CB}_n$ )
		74F 5% $V_{\text{CC}}$	2.7				$I_{\text{OH}} = -3\text{ mA}$ ( $\text{DB}_n$ , $\text{CB}_n$ )
$V_{\text{OL}}$	Output LOW Voltage	54F 10% $V_{\text{CC}}$		0.5	V	Min	$I_{\text{OL}} = 20\text{ mA}$ (ERR, MERR, $\text{DB}_n$ , $\text{CB}_n$ )
		74F 10% $V_{\text{CC}}$		0.5			$I_{\text{OL}} = 20\text{ mA}$ (ERR, MERR)
		74F 10% $V_{\text{CC}}$		0.5			$I_{\text{OL}} = 24\text{ mA}$ ( $\text{DB}_n$ , $\text{CB}_n$ )
$I_{\text{IH}}$	Input HIGH Current	54F		20.0	$\mu\text{A}$	Max	$V_{\text{IN}} = 2.7\text{V}$ ( $S_0$ , $S_1$ , $\text{OEB}_n$ , $\text{OECB}$ , $\text{LEDBO}$ )
		74F		5.0			
$I_{\text{BVI}}$	Input HIGH Current Breakdown Test	54F		100	$\mu\text{A}$	Max	$V_{\text{IN}} = 7.0\text{V}$ ( $S_0$ , $S_1$ , $\text{OEB}_n$ , $\text{OECB}$ , $\text{LEDBO}$ )
		74F		7.0			
$I_{\text{BVT}}$	Input HIGH Current Breakdown (I/O)	54F		1.0	mA	Max	$V_{\text{IN}} = 5.5\text{V}$ ( $\text{CB}_n$ , $\text{DB}_n$ )
		74F		0.5			
$I_{\text{CEX}}$	Output HIGH Leakage Current	54F		250	$\mu\text{A}$	Max	$V_{\text{OUT}} = V_{\text{CC}}$
		74F		50			
$V_{\text{ID}}$	Input Leakage Test	74F	4.75		V	0.0	$I_{\text{ID}} = 1.9\text{ }\mu\text{A}$ All Other Pins Grounded
$I_{\text{OD}}$	Output Leakage Circuit Current	74F		3.75	$\mu\text{A}$	0.0	$V_{\text{IOD}} = 150\text{ mV}$ All Other Pins Grounded
$I_{\text{IL}}$	Input LOW Current			-0.6	mA	Max	$V_{\text{IN}} = 0.5\text{V}$ ( $S_0$ , $S_1$ , $\text{OEB}_n$ , $\text{OECB}$ , $\text{LEDBO}$ )
$I_{\text{IH}} + I_{\text{OZH}}$	Output Leakage Current			70	$\mu\text{A}$	Max	$V_{\text{I/O}} = 2.7\text{V}$ ( $\text{CB}_n$ , $\text{DB}_n$ )
$I_{\text{IL}} + I_{\text{OZL}}$	Output Leakage Current			-650	$\mu\text{A}$	Max	$V_{\text{I/O}} = 0.5\text{V}$ ( $\text{CB}_n$ , $\text{DB}_n$ )
$I_{\text{OZH}}$	Output Leakage Current			70	$\mu\text{A}$	Max	$V_{\text{I/O}} = 2.7\text{V}$ ( $\text{CB}_n$ , $\text{DB}_n$ )
$I_{\text{OZL}}$	Output Leakage Current			-650	$\mu\text{A}$	Max	$V_{\text{I/O}} = 0.5\text{V}$ ( $\text{CB}_n$ , $\text{DB}_n$ )
$I_{\text{OS}}$	Output Short-Circuit Current		-60	-150	mA	Max	$V_{\text{OUT}} = 0\text{V}$
$I_{\text{ZZ}}$	Bus Drainage Test			500	$\mu\text{A}$	0.0V	$V_{\text{OUT}} = 5.25\text{V}$ ( $\text{CB}_n$ , $\text{DB}_n$ )
$I_{\text{CC}}$	Power Supply Current			340	mA	Max	$T_{\text{A}} = 0^{\circ}\text{C}-25^{\circ}\text{C}$
$I_{\text{CC}}$	Power Supply Current			325	mA	Max	$T_{\text{A}} = 25^{\circ}\text{C}-70^{\circ}\text{C}$

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay DB or CB to ERR	4.0	14.0	27.0			4.0	31.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay DB to ERR	4.0	21.0	27.0			4.0	31.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay DB or CB to MERR	5.0	17.0	27.0			5.0	31.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay DB to MERR	5.0	23.0	27.0			5.0	31.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S <sub>0</sub> and S <sub>1</sub> , LOW, to DB	4.0	12.0	16.0			4.0	20.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S <sub>1</sub> to CB	4.0	10.5	14.0			4.0	15.0	ns	2-3
t <sub>PLH</sub>	Propagation Delay S <sub>0</sub> or S <sub>1</sub> to ERR or MERR	2.0	11.5	13.0			2.0	14.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay DB to CB	4.0	16.0	23.0			4.0	25.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEDBO to DB	2.0	11.0	13.0			2.0	14.0	ns	2-3
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OEB <sub>n</sub> to DB	1.0	6.0	10.0			1.0	10.0	ns	2-5
t <sub>PHZ</sub> t <sub>PZL</sub>	Output Disable Time OEB <sub>n</sub> to DB	1.0	5.0	10.0			1.0	10.0	ns	2-5
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OECB to CB	1.0	6.0	10.0			1.0	10.0	ns	2-5
t <sub>PHZ</sub> t <sub>PZL</sub>	Output Disable Time OECB to CB	1.0	5.0	10.0			1.0	10.0	ns	2-5
V <sub>IN</sub> = 2.7V (S <sub>0</sub> , S <sub>1</sub> , OEB <sub>n</sub> , OECB, LEDBO)		Max	μA	20.0			24F		Input HIGH Current	I <sub>ih</sub>
V <sub>IN</sub> = 2.7V (S <sub>0</sub> , S <sub>1</sub> , OEB <sub>n</sub> , OECB, LEDBO)		Max	μA	100			24F		Input HIGH Current Breakdown Test	I <sub>ih</sub>
V <sub>IN</sub> = 2.7V (S <sub>0</sub> , S <sub>1</sub> , OEB <sub>n</sub> , OECB, LEDBO)		Max	μA	1.0			24F		Input HIGH Current Breakdown (I <sub>ih</sub> )	I <sub>ih</sub>
V <sub>OUT</sub> = V <sub>CC</sub>		Max	μA	250			24F		Output HIGH Leakage Current	I <sub>oh</sub>
I <sub>D</sub> = 1.5 μA All Other Pins Grounded		0.0	V				24F		Input Leakage Test	V <sub>il</sub>
V <sub>OD</sub> = 180 mV All Other Pins Grounded		0.0	μA	3.75			24F		Output Leakage Circuit Current	I <sub>od</sub>
V <sub>IN</sub> = 0.5V (S <sub>0</sub> , S <sub>1</sub> , OEB <sub>n</sub> , OECB, LEDBO)		Max	mA	-0.8					Input LOW Current	I <sub>il</sub>
V <sub>OD</sub> = 2.7V (CB <sub>n</sub> , DB <sub>n</sub> )		Max	μA	70					Output Leakage Current	I <sub>il</sub> + I <sub>ozh</sub>
V <sub>OD</sub> = 0.5V (CB <sub>n</sub> , DB <sub>n</sub> )		Max	μA	-850					Output Leakage Current	I <sub>il</sub> + I <sub>ozl</sub>
V <sub>OD</sub> = 2.7V (CB <sub>n</sub> , DB <sub>n</sub> )		Max	μA	70					Output Leakage Current	I <sub>ozh</sub>
V <sub>OD</sub> = 0.5V (CB <sub>n</sub> , DB <sub>n</sub> )		Max	μA	-850					Output Leakage Current	I <sub>ozl</sub>
V <sub>OUT</sub> = 0V		Max	mA	-150					Output Short-Circuit Current	I <sub>os</sub>
V <sub>OUT</sub> = 0.5V (CB <sub>n</sub> , DB <sub>n</sub> )		0.0V	μA	800					Bus Drainage Test	I <sub>zs</sub>
T <sub>A</sub> = 0°C - 25°C		Max	mA	340					Power Supply Current	I <sub>cc</sub>
T <sub>A</sub> = 25°C - 70°C		Max	mA	325					Power Supply Current	I <sub>cc</sub>

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s$	Setup Time, HIGH or LOW DB/CB before $S_0$ HIGH ( $S_1$ HIGH)	3.0				3.0		ns	2-6
$t_s(\text{H})$	Setup Time, HIGH $S_0$ HIGH before LEDBO HIGH	12.0				14.0		ns	2-6
$t_s(\text{H})$	Setup Time, HIGH LEDBO HIGH before $S_0$ or $S_1$ LOW	0				0		ns	2-6
$t_s(\text{H})$	Setup Time, HIGH LEDBO HIGH before $S_1$ HIGH	0				0		ns	2-6
$t_s$	Setup Time, HIGH or LOW Diagnostic DB before $S_1$ HIGH	0				0		ns	2-6
$t_s$	Setup Time, HIGH or LOW Diagnostic CB before $S_1$ LOW or $S_0$ HIGH	3.0				3.0		ns	2-6
$t_s$	Setup Time, HIGH or LOW Diagnostic DB before LEDBO HIGH ( $S_1$ LOW, $S_0$ HIGH)	8.0				8.0		ns	2-6
$t_h(\text{L})$	Hold Time, LOW $S_0$ LOW after $S_1$ HIGH	8.0				8.0		ns	2-6
$t_h$	Hold Time, HIGH or LOW DB and CB Hold after $S_0$ HIGH	8.0				8.0		ns	2-6
$t_h$	Hold Time, HIGH or LOW DB Hold after $S_1$ HIGH	8.0				8.0		ns	2-6
$t_h$	Hold Time, HIGH or LOW CB Hold after $S_1$ LOW or $S_0$ HIGH	5.0				5.0		ns	2-6
$t_h$	Hold Time, HIGH or LOW Diagnostic DB after LEDBO HIGH ( $S_1$ LOW, $S_0$ HIGH)	0				0		ns	2-6
$t_w(\text{L})^*$	LEDBO Pulse Width	8.0				8.0		ns	2-4
$t_{\text{corr}}^*$	Correction Time		25.0				28.0	ns	

\*Note: These parameters are guaranteed by characterization or other tests performed.

Pin Name	Description	U.L. HIGH/LOW	Input High/Low Output Low/High
OE	Output Enable Input (Active LOW)	1.0V/0.	20 $\mu\text{A}$ - 0.8 mA
$\overline{\text{TR}}$	Transmit/Receive Input	1.0V/0.	20 $\mu\text{A}$ - 0.8 mA
A0-A7	Side A Inputs or TRI-STATE Outputs	3.5V/0.66V	70 $\mu\text{A}$ - 0.4 mA
B0-B7	Side B Inputs or TRI-STATE Outputs	3.5V/0.66V	70 $\mu\text{A}$ - 0.4 mA
		600V/0.8 (80)	-12 mV/84 mA (48 mA)
		600V/0.8 (80)	-12 mV/84 mA (48 mA)





## 54F/74F640 • 54F/74F643 • 54F/74F645

### Octal Bus Transceiver with TRI-STATE® Outputs

#### General Description

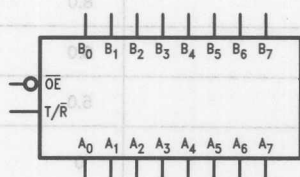
These devices are octal bus transceivers designed for asynchronous two-way data flow between the A and B busses. Both busses are capable of sinking 64 mA, have TRI-STATE outputs, and a common output enable pin. The direction of data flow is determined by the transmit/receive (T/R) input. The 'F645 is a high speed/low power version of the 'F245. The 'F640 is an inverting option of the 'F645. The 'F643 has a noninverting A bus and an inverting B bus.

#### Features

- Designed for asynchronous two-way data flow between busses
- Outputs sink 64 mA
- Transmit/receive (T/R) input controls the direction of data flow
- Guaranteed 4000V minimum ESD protection
- 'F645 is a lower power, faster version of the 'F245
- 'F640 is an inverting option of the 'F645
- 'F643 has noninverting A bus and inverting B bus

**Ordering Code:** See Section 5

#### Logic Symbol



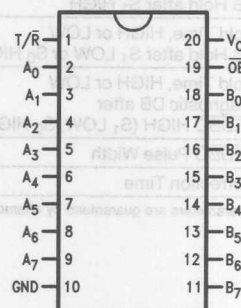
TL/F/10267-3

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
T/R	Transmit/Receive Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
A <sub>0</sub> -A <sub>7</sub>	Side A Inputs or TRI-STATE Outputs	3.5/0.667	70 $\mu$ A/ -0.4 mA
B <sub>0</sub> -B <sub>7</sub>	Side B Inputs or TRI-STATE Outputs	600/106.6 (80)	-12 mA/64 mA (48 mA)
		3.5/0.667	70 $\mu$ A/ -0.4 mA
		600/106.6 (80)	-12 mA/64 mA (48 mA)

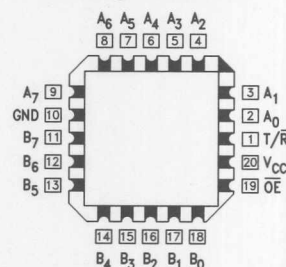
#### Connection Diagrams

##### Pin Assignment for DIP, SOIC and Flatpak



TL/F/10267-1

##### Pin Assignment for LCC



TL/F/10267-2

## Functional Description

The output enable ( $\overline{OE}$ ) is active LOW. If the device is disabled ( $\overline{OE}$  HIGH), the outputs are in the high impedance state. The transmit/receive input ( $T/\overline{R}$ ) controls whether data is transmitted from the A bus to the B bus or from the B bus to the A bus. When  $T/\overline{R}$  is LOW, B data is sent to the A bus. If  $T/\overline{R}$  is HIGH, A data is sent to the B bus.

## Function Table

Inputs		Outputs		
$\overline{OE}$	$T/\overline{R}$	'F640	'F643	'F645
L	L	Bus $\overline{B}$ data to Bus A	Bus B data to Bus A	Bus B data to Bus A
L	H	Bus $\overline{A}$ data to Bus B	Bus $\overline{A}$ data to Bus B	Bus A data to Bus B
H	X	Z	Z	Z

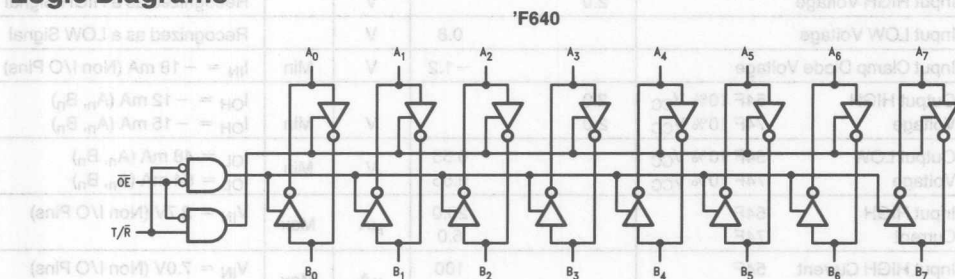
H = High voltage level

L = Low voltage level

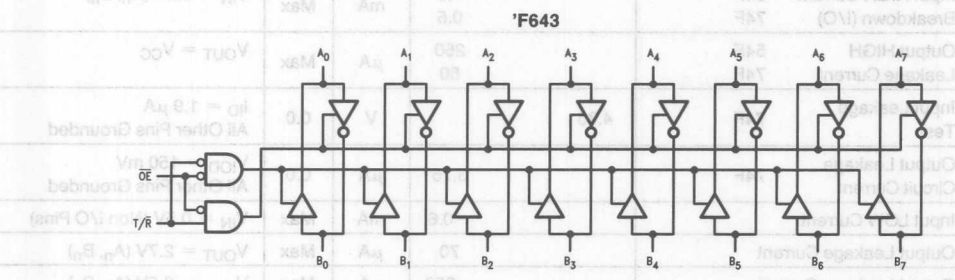
X = Don't care

Z = High-impedance state

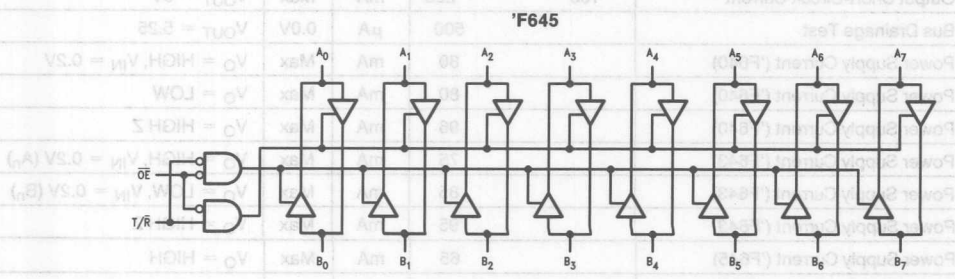
## Logic Diagrams



TL/F/10267-4



TL/F/10267-5



TL/F/10267-6

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output	−0.5V to +5.5V
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)  
ESD Last Passing Voltage (Min) 4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	−55°C to +125°C
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA (Non I/O Pins)
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>	2.0 2.0		V	Min	I <sub>OH</sub> = −12 mA (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OH</sub> = −15 mA (A <sub>n</sub> , B <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.55 0.55	V	Min	I <sub>OL</sub> = 48 mA (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OL</sub> = 64 mA (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V (Non I/O Pins)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V (Non I/O Pins)
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)	54F 74F		1.0 0.5	mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V (Non I/O Pins)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			−650	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current		−100	−225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25
I <sub>CCH</sub>	Power Supply Current ('F640)			80	mA	Max	V <sub>O</sub> = HIGH, V <sub>IN</sub> = 0.2V
I <sub>CCL</sub>	Power Supply Current ('F640)			80	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current ('F640)			96	mA	Max	V <sub>O</sub> = HIGH Z
I <sub>CCH</sub>	Power Supply Current ('F643)			75	mA	Max	V <sub>O</sub> = HIGH, V <sub>IN</sub> = 0.2V (A <sub>n</sub> )
I <sub>CCL</sub>	Power Supply Current ('F643)			85	mA	Max	V <sub>O</sub> = LOW, V <sub>IN</sub> = 0.2V (B <sub>n</sub> )
I <sub>CCZ</sub>	Power Supply Current ('F643)			95	mA	Max	V <sub>O</sub> = HIGH Z
I <sub>CCH</sub>	Power Supply Current ('F645)			65	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current ('F645)			80	mA	Max	V <sub>O</sub> = LOW, V <sub>IN</sub> = 0.2V
I <sub>CCZ</sub>	Power Supply Current ('F645)			90	mA	Max	V <sub>O</sub> = HIGH Z

**'F640 AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay A Input to B Output	2.5 2.0		7.5 7.0			2.0 2.0	8.0 7.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay B Input to A Output	2.5 2.0		7.5 7.0			2.0 2.0	8.0 7.0	ns	2-3
$t_{PZH}$ $t_{PZL}$	Enable Time $\overline{\text{OE}}$ Input to A Output	2.5 2.5		7.5 8.0			2.0 2.0	9.0 8.5	ns	2-5
$t_{PHZ}$ $t_{PLZ}$	Disable Time $\overline{\text{OE}}$ Input to A Output	1.5 1.5		7.0 6.0			1.0 1.5	7.5 6.0		
$t_{PZH}$ $t_{PZL}$	Enable Time $\overline{\text{OE}}$ Input to B Output	2.5 2.5		7.5 8.0			2.0 2.0	9.0 8.5	ns	2-5
$t_{PHZ}$ $t_{PLZ}$	Disable Time $\overline{\text{OE}}$ Input to B Output	1.5 1.5		7.0 6.0			1.0 1.5	7.5 6.0		

**'F643 AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay A Input to B Output	2.5 2.0		7.5 7.0			2.0 2.0	8.0 7.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay B Input to A Output	1.5 2.0		6.0 7.0			1.5 2.0	7.0 7.5	ns	2-3
$t_{PZH}$ $t_{PZL}$	Enable Time $\overline{OE}$ Input to A Output	2.5 2.5		8.0 8.5			2.0 2.0	9.0 8.5	ns	2-5
$t_{PHZ}$ $t_{PLZ}$	Disable Time $\overline{OE}$ Input to A Output	1.5 1.0		7.0 5.5			1.0 1.0	8.0 5.5		
$t_{PZH}$ $t_{PZL}$	Enable Time $\overline{OE}$ Input to B Output	2.5 2.5		7.5 8.0			2.0 2.0	9.0 8.5	ns	2-5
$t_{PHZ}$ $t_{PLZ}$	Disable Time $\overline{OE}$ Input to B Output	1.5 1.5		6.5 6.0			1.0 1.5	7.5 6.0		

**'F645 AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay A Input to B Output	1.5 2.0		6.0 7.0			1.5 2.0	7.0 7.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay B Input to A Output	1.5 2.0		6.0 7.0			1.5 2.0	7.0 7.5	ns	2-3
$t_{PZH}$ $t_{PZL}$	Enable Time $\overline{OE}$ Input to A Output	2.5 2.5		8.0 8.5			2.0 2.0	9.0 8.5	ns	2-5
$t_{PHZ}$ $t_{PLZ}$	Disable Time $\overline{OE}$ Input to A Output	1.5 1.0		7.0 5.5			1.0 1.0	8.0 5.5		
$t_{PZH}$ $t_{PZL}$	Enable Time $\overline{OE}$ Input to B Output	2.5 2.5		7.5 8.5			2.0 2.5	9.5 9.0	ns	2-5
$t_{PHZ}$ $t_{PLZ}$	Disable Time $\overline{OE}$ Input to B Output	1.5 1.0		6.5 5.5			1.0 1.0	7.5 5.5		

**'F643 AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Fig. No.	Units	74F			54F			74F			Parameter	Symbol
		$T_A, V_{CC} = \text{Com}$ $C_L = 50 \text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50 \text{ pF}$			$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50 \text{ pF}$				
		Min	Max		Min	Max		Min	Typ	Max		
2-3	ns	8.0	5.0			7.5	5.5			Propagation Delay A Input to B Output	$t_{PLH}$ $t_{PHL}$	
		7.0	5.0			7.0	5.0					
2-3	ns	7.0	5.0			8.0	5.5			Propagation Delay B Input to A Output	$t_{PLH}$ $t_{PHL}$	
		7.5	5.0			7.0	5.0					
2-5	ns	8.0	5.0			8.0	5.5			Enable Time $\overline{OE}$ Input to A Output	$t_{PZH}$ $t_{PZL}$	
		8.5	5.0			8.5	5.5					
		8.0	1.0			7.0	1.5			Disable Time $\overline{OE}$ Input to A Output	$t_{PHZ}$ $t_{PLZ}$	
		8.5	1.0			8.5	1.0					
2-5	ns	8.0	5.0			7.5	5.5			Enable Time $\overline{OE}$ Input to B Output	$t_{PZH}$ $t_{PZL}$	
		8.5	5.0			8.0	5.5					
		8.0	1.0			7.5	1.5			Disable Time $\overline{OE}$ Input to B Output	$t_{PHZ}$ $t_{PLZ}$	
		8.5	1.0			8.5	1.5					

## 54F/74F646 • 54F/74F648

### Octal Transceiver/Register with TRI-STATE® Outputs

#### General Description

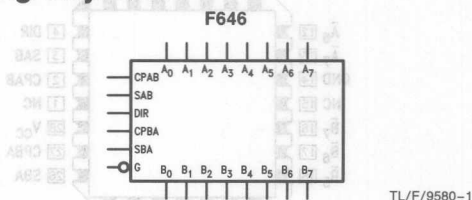
These devices consist of bus transceiver circuits with TRI-STATE, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control  $\bar{G}$  and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control  $\bar{G}$  is Active LOW. In the isolation mode (control  $\bar{G}$  HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

#### Features

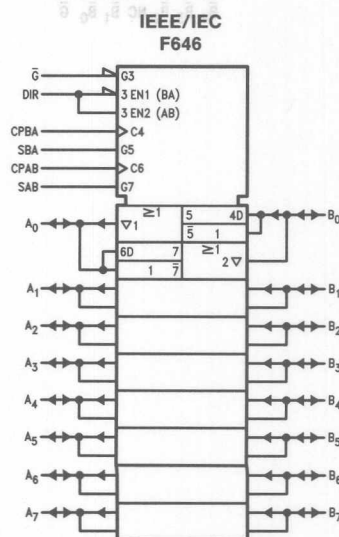
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of true and inverting ('F648) data paths
- TRI-STATE outputs
- 300 mil slim DIP
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

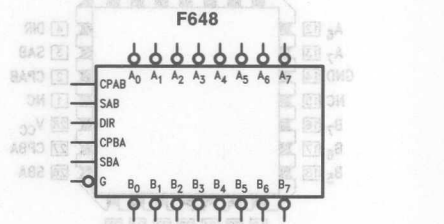
#### Logic Symbols



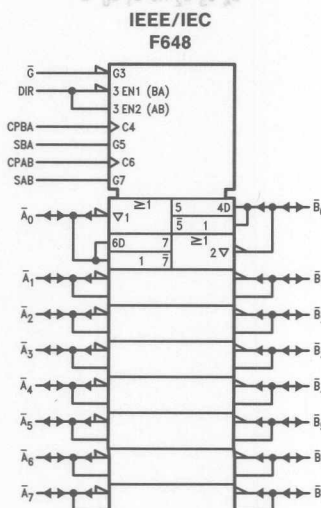
TL/F/9580-1



TL/F/9580-4



TL/F/9580-7

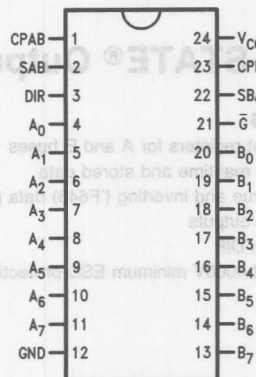


TL/F/9580-9



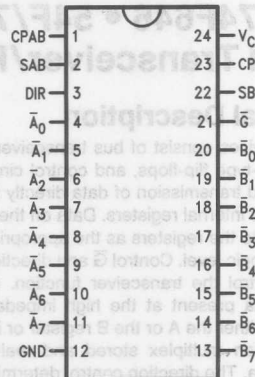
## Connection Diagrams

Pin Assignment  
for DIP, SOIC and Flatpak  
F646



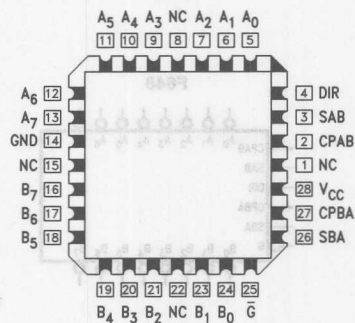
TL/F/9580-2

Pin Assignment  
for DIP, SOIC and Flatpak  
F648



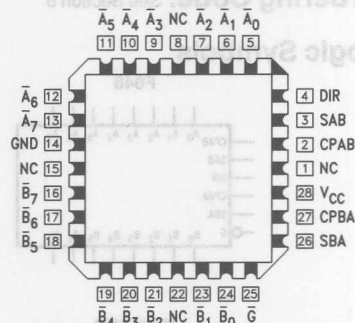
TL/F/9580-8

Pin Assignment  
for LCC  
F646



TL/F/9580-3

Pin Assignment  
for LCC  
F648









TL/F/9580-10

# Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
A <sub>0</sub> –A <sub>7</sub>	Data Register A Inputs/ TRI-STATE Outputs	3.5/1.083 600/106.6 (80)	70 $\mu$ A/ –650 $\mu$ A –12 mA/64 mA (48 mA)
B <sub>0</sub> –B <sub>7</sub>	Data Register B Inputs/ TRI-STATE Outputs	3.5/1.083 600/106.6 (80)	70 $\mu$ A/ –650 $\mu$ A –12 mA/64 mA (48 mA)
CPAB, CPBA	Clock Pulse Inputs	1.0/1.0	20 $\mu$ A/ –0.6 mA
SAB, SBA	Select Inputs	1.0/1.0	20 $\mu$ A/ –0.6 mA
$\bar{G}$	Output Enable Input	1.0/1.0	20 $\mu$ A/ –0.6 mA
DIR	Direction Control Input	1.0/1.0	20 $\mu$ A/ –0.6 mA

Function Table


Inputs						Data I/O*		Function
$\bar{G}$	DIR	CPAB	CPBA	SAB	SBA	A <sub>0</sub> –A <sub>7</sub>	B <sub>0</sub> –B <sub>7</sub>	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X		X	X	X			Clock A <sub>n</sub> Data into A Register
H	X	X		X	X			Clock B <sub>n</sub> Data into B Register
L	H	X	X	L	X	Input	Output	A <sub>n</sub> to B <sub>n</sub> —Real Time (Transparent Mode)
L	H		X	L	X			Clock A <sub>n</sub> Data into A Register
L	H	H or L	X	H	X			A Register to B <sub>n</sub> (Stored Mode)
L	H		X	H	X			Clock A <sub>n</sub> Data into A Register and Output to B <sub>n</sub>
L	L	X	X	X	L	Output	Input	B <sub>n</sub> to A <sub>n</sub> —Real Time (Transparent Mode)
L	L	X		X	L			Clock B <sub>n</sub> Data into B Register
L	L	X	H or L	X	H			B Register to A <sub>n</sub> (Stored Mode)
L	L	X		X	H			Clock B <sub>n</sub> Data into B Register and Output to A <sub>n</sub>

\*The data output functions may be enabled or disabled by various signals at the  $\bar{G}$  and DIR Inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

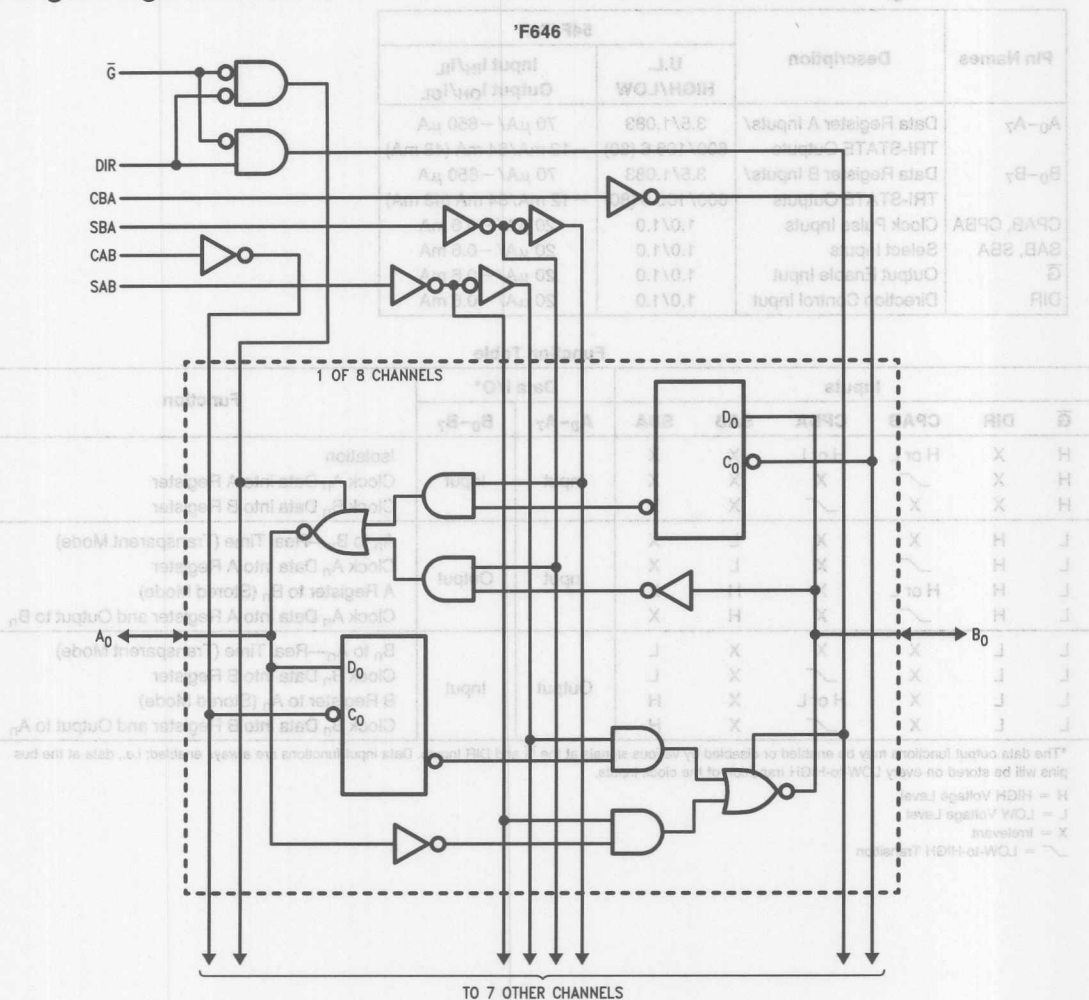
H = HIGH Voltage Level

L = LOW Voltage Level

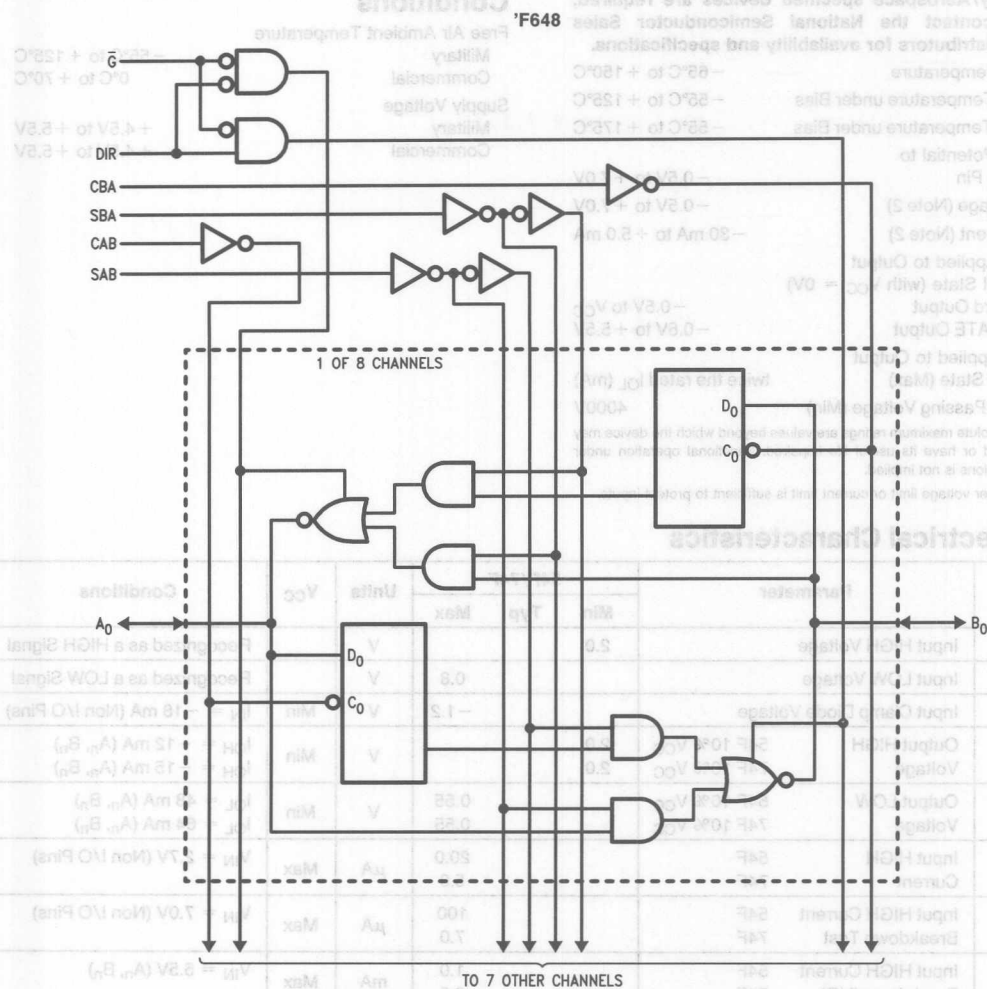
X = Irrelevant

 = LOW-to-HIGH Transition

## Logic Diagrams (Continued)



## Logic Diagrams (Continued)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

TL/F/9580-6

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA (Non I/O Pins)
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>	2.0 2.0		V	Min	I <sub>OH</sub> = −12 mA (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OH</sub> = −15 mA (A <sub>n</sub> , B <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.55 0.55	V	Min	I <sub>OL</sub> = 48 mA (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OL</sub> = 64 mA (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V (Non I/O Pins)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V (Non I/O Pins)
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)	54F 74F		1.0 0.5	mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V (Non I/O Pins)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			−650	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current		−100	−225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current			135	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			150	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current			150	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	90		75		90		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	2.0	7.0	2.0	8.5	2.0	8.0	ns	2-3
$t_{\text{PHL}}$	Clock to Bus	2.0	8.0	2.0	9.5	2.0	9.0		
$t_{\text{PLH}}$	Propagation Delay	1.0	7.0	1.0	8.0	1.0	7.5	ns	2-3
$t_{\text{PHL}}$	Bus to Bus ('F646)	1.0	6.5	1.0	8.0	1.0	7.0		
$t_{\text{PLH}}$	Propagation Delay	2.0	8.5	1.0	10.0	2.0	9.0	ns	2-3
$t_{\text{PHL}}$	Bus to Bus ('F648)	1.0	7.5	1.0	9.0	1.0	8.0		
$t_{\text{PLH}}$	Propagation Delay	2.0	8.5	2.0	11.0	2.0	9.5	ns	2-3
$t_{\text{PHL}}$	SBA or SAB to A or B	2.0	8.0	2.0	10.0	2.0	9.0		
$t_{\text{pZH}}$	Enable Time	2.0	8.5	2.0	10.0	2.0	9.0	ns	
$t_{\text{pZL}}$	$\overline{\text{OE}}$ to A or B	2.0	12.0	2.0	13.5	2.0	12.5		
$t_{\text{PHZ}}$	Disable Time	1.0	7.5	1.0	9.0	1.0	8.5	ns	2-5
$t_{\text{PLZ}}$	$\overline{\text{OE}}$ to A or B	2.0	9.0	2.0	11.0	2.0	9.5		
$t_{\text{pZH}}$	Enable Time	2.0	14.0	2.0	16.0	2.0	15.0	ns	
$t_{\text{pZL}}$	DIR to A or B	2.0	13.0	2.0	15.0	2.0	14.0		
$t_{\text{PHZ}}$	Disable Time	1.0	9.0	1.0	10.0	1.0	9.5	ns	2-5
$t_{\text{PLZ}}$	DIR to A or B	2.0	11.0	2.0	12.0	2.0	11.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	5.0		5.0		5.0		ns	2-6
$t_s(\text{L})$	Bus to Clock	5.0		5.0		5.0		ns	
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0		2.5		2.0		ns	2-6
$t_h(\text{L})$	Bus to Clock	2.0		2.5		2.0		ns	
$t_w(\text{H})$	Clock Pulse Width	5.0		5.0		5.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	5.0		5.0		5.0		ns	





## 54F/74F651 • 54F/74F652 Transceivers/Registers

### General Description

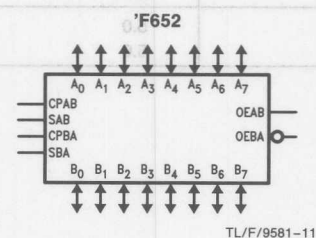
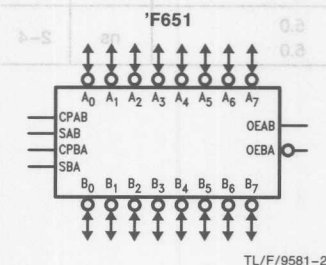
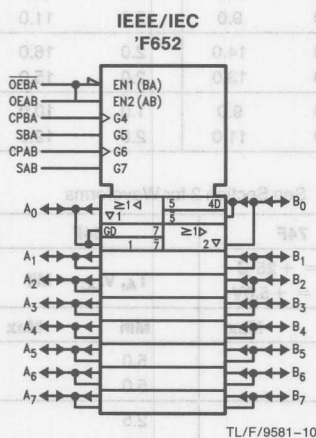
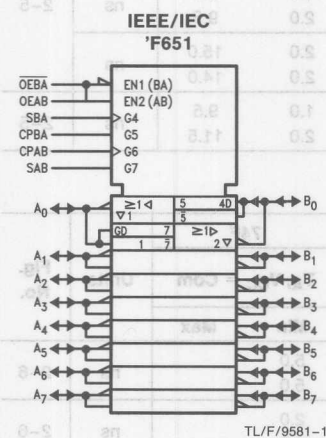
These devices consist of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, OEBA) are provided to control the transceiver function.

### Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of non-inverting and inverting data paths
  - 'F651 inverting
  - 'F652 non-inverting
- Guaranteed 4000V minimum ESD protection

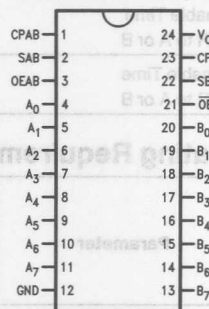
**Ordering Code:** See Section 5

### Logic Symbols

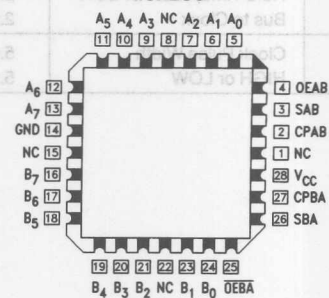


### Connection Diagrams

#### Pin Assignment DIP, SOIC and Flatpak

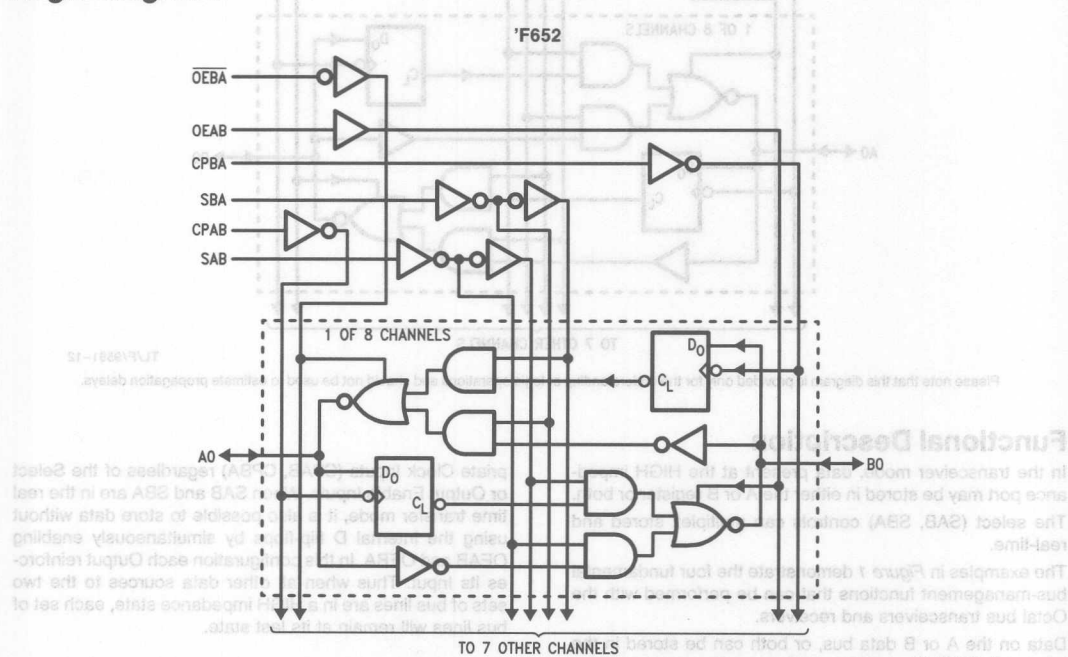


#### Pin Assignment for LCC



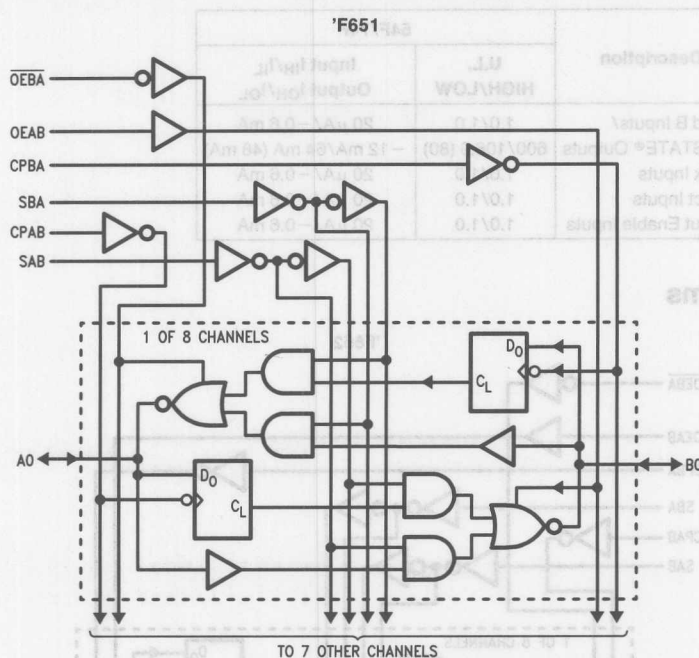
**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_0-A_7, B_0-B_7$	A and B Inputs/ TRI-STATE® Outputs	1.0/1.0	20 $\mu$ A/ -0.6 mA -12 mA/64 mA (48 mA)
CPAB, CPBA	Clock Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
SAB, SBA	Select Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
OEAB, OEBA	Output Enable Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA

**Logic Diagrams**

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Logic Diagrams (Continued)



TL/F/9581-12

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

### Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both. The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the Octal bus transceivers and receivers.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appro-

appropriate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

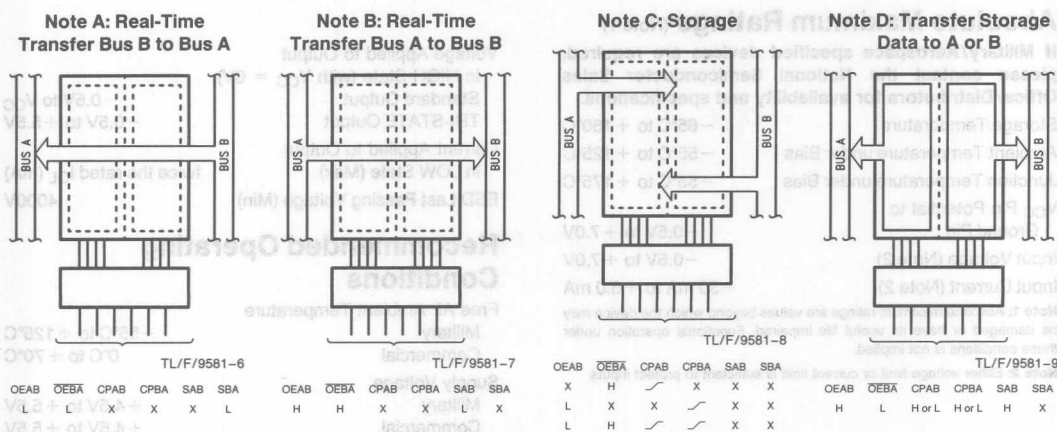


FIGURE 1

Inputs						Inputs/Outputs (Note 1)		Operating Mode
OEAB	OEBA	CPAB	CPBA	SAB	SBA	A <sub>0</sub> thru A <sub>7</sub>	B <sub>0</sub> thru B <sub>7</sub>	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	/	/	X	X		Input	Store A and B Data
X	H	/	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	/	/	X	X	Input	Output	Store A in Both Registers
L	X	H or L	/	X	X	Not Specified	Input	Hold A, Store B
L	L	/	/	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L		Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Input	Output	Store B Data to A Bus
H	H	X	X	L	X			Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 / = LOW to HIGH Clock Transition

**Note 1:** The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Recommended Operating Conditions**

Free Air Ambient Temperature	−55°C to +125°C
Military Commercial	0°C to +70°C
Supply Voltage	
Military Commercial	+4.5V to +5.5V
	+4.5V to +5.5V

**DC Electrical Characteristics**

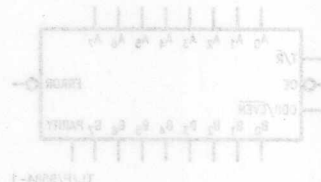
Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				−1.2	V	Min	I <sub>IN</sub> = −18 mA (Non I/O Pins)
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.0			V	Min	I <sub>OH</sub> = −12 mA (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OH</sub> = −15 mA (A <sub>n</sub> , B <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.0					
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>			0.55	V	Min	I <sub>OL</sub> = 48 mA (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OL</sub> = 64 mA (A <sub>n</sub> , B <sub>n</sub> )
		74F 10% V <sub>CC</sub>			0.55			
I <sub>IH</sub>	Input HIGH Current	54F 74F			20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V (Non I/O Pins)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F			100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)	54F 74F			1.0 0.5	mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F			250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F			3.75	μA	0.0	V <sub>I<sub>OD</sub></sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current				−0.6	mA	Max	V <sub>IN</sub> = 0.5V (Non I/O Pins)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current				70	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current				−650	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current		−100		−225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test				500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current			105	135	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			118	150	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current			115	150	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Max. Clock Frequency	90		75		90		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	2.0	7.0	2.0	8.5	2.0	8.0	ns	2-3
$t_{\text{PHL}}$	Clock to Bus	2.0	8.0	2.0	9.5	2.0	9.0		
$t_{\text{PLH}}$	Propagation Delay	2.0	8.5	1.0	9.0	2.0	9.0	ns	2-3
$t_{\text{PHL}}$	Bus to Bus ('F651)	1.0	7.5	1.0	8.0	1.0	8.0		
$t_{\text{PLH}}$	Propagation Delay	1.0	7.0	1.0	8.0	1.0	7.5	ns	2-3
$t_{\text{PHL}}$	Bus to Bus ('F652)	1.0	6.5	1.0	8.0	1.0	7.0		
$t_{\text{PLH}}$	Propagation Delay	2.0	8.5	2.0	11.0	2.0	9.5	ns	2-3
$t_{\text{PHL}}$	SBA or SAB to A or B	2.0	8.0	2.0	10.0	2.0	9.0		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
t <sub>PZH</sub>	Enable Time	2.0	9.5	2.0	10.0	2.0	10.0	ns	2-5
t <sub>PZL</sub>	*OEBA to A	2.0	12.0	2.0	10.0	2.0	12.5		
t <sub>PHZ</sub>	Disable Time	1.0	7.5	1.0	9.0	1.0	8.0		
t <sub>PLZ</sub>	*OEBA to A	2.0	8.5	1.0	9.0	2.0	9.0		
t <sub>PZH</sub>	Enable Time	2.0	9.5	2.0	10.0	2.0	10.0		
t <sub>PZL</sub>	OEAB to B	3.0	13.0	2.0	12.0	3.0	14.0		
t <sub>PHZ</sub>	Disable Time	2.0	9.0	1.0	9.0	2.0	10.0	ns	2-5
t <sub>PLZ</sub>	OEAB to B	2.0	10.5	1.0	12.0	2.0	11.0		
t <sub>S</sub> (H)	Setup Time, HIGH or	5.0		5.0		5.0		ns	2-6
t <sub>S</sub> (L)	LOW, Bus to Clock	5.0		5.0		5.0			
t <sub>H</sub> (H)	Hold Time, HIGH or	2.0		2.5		2.0		ns	2-6
t <sub>H</sub> (L)	LOW, Bus to Clock	2.0		2.5		2.0			
t <sub>w</sub> (H)	Clock Pulse Width	5.0		5.0		5.0		ns	2-4
t <sub>w</sub> (L)	HIGH or LOW	5.0		5.0		5.0			







## 54F/74F657 Octal Bidirectional Transceiver with 8-Bit Parity Generator/Checker and TRI-STATE® Outputs

### General Description

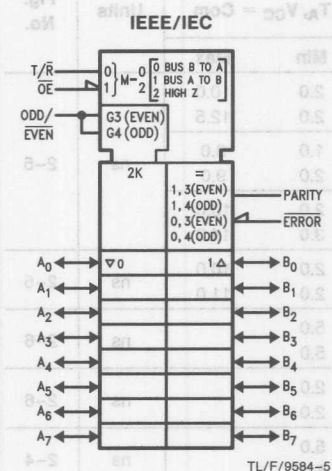
The 'F657 contains eight non-inverting buffers with TRI-STATE® outputs and an 8-bit parity generator/checker. It is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 24 mA (20 mA mil) at the A port and 64 mA (48 mA mil) at the B port.

### Features

- 300 Mil 24-pin slimline DIP
- Combines 'F245 and 'F280A functions in one package
- TRI-STATE outputs
- B Outputs sink 64 mA (48 mA mil)
- 12 mA source current, B side
- Input diodes for termination effects

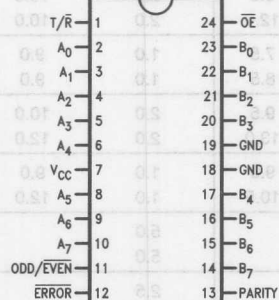
**Ordering Code:** See Section 5

### Logic Symbols



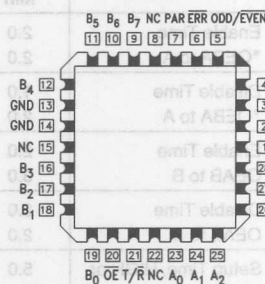
### Connection Diagrams

Pin Assignment  
for DIP, SOIC  
and Flatpak

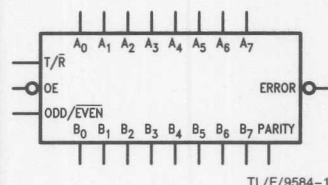


TL/F/9584-2

Pin Assignment  
for LCC



TL/F/9584-3



TL/F/9584-1

		HIGH/LOW	Output $I_{OH}/I_{OL}$
$A_0-A_7$	Data Inputs/ TRI-STATE Outputs	4.5/0.15 150/40 (33.3)	90 $\mu A$ / - 90 $\mu A$ - 3 mA/24 mA (20 mA)
$B_0-B_7$	Data Inputs/ TRI-STATE Outputs	3.5/0.117 600/106.6 (80)	70 $\mu A$ / - 70 $\mu A$ - 12 mA/64 mA (48 mA)
$T/\bar{R}$	Transmit/Receive Input	2.0/0.067	40 $\mu A$ / - 40 $\mu A$
$\bar{OE}$	Enable Input	2.0/0.067	40 $\mu A$ / - 40 $\mu A$
PARITY	Parity Input/ TRI-STATE Output	3.5/0.117 600/106.6 (80)	70 $\mu A$ / - 70 $\mu A$ - 12 mA/64 mA (48 mA)
ODD/ $\bar{EVEN}$	ODD/ $\bar{EVEN}$ Parity Input	1.0/0.033	20 $\mu A$ / - 20 $\mu A$
ERROR	Error Output	600/106.6 (80)	- 12 mA/64 mA (48 mA)

## Functional Description

The Transmit/Receive ( $T/\bar{R}$ ) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from the A port to the B port; Receive (active LOW) enables data from the B port to the A port.

The Output Enable ( $\bar{OE}$ ) input disables the parity and  $\bar{ERROR}$  outputs and both the A and B ports by placing them in a HIGH-Z condition when the Output Enable input is HIGH.

When transmitting ( $T/\bar{R}$  HIGH), the parity generator detects whether an even or odd number of bits on the A port are HIGH and compares these with the condition of the parity select (ODD/ $\bar{EVEN}$ ).

If the Parity Select is HIGH and an even number of A inputs are HIGH, the Parity output is HIGH.

In receiving mode ( $T/\bar{R}$  LOW), the parity select and number of HIGH inputs on port B are compared to the condition of the Parity input. If an even number of bits on the B port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, then  $\bar{ERROR}$  will be HIGH to indicate no error. If an odd number of bits on the B port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, the  $\bar{ERROR}$  will be LOW indicating an error.

Function Table

Number of Inputs That Are High	Inputs			Input/Output	Outputs	
	$\bar{OE}$	$T/\bar{R}$	ODD/ $\bar{EVEN}$	Parity	$\bar{ERROR}$	Outputs Mode
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Immaterial	H	X	X	Z	Z	Z

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Function Table

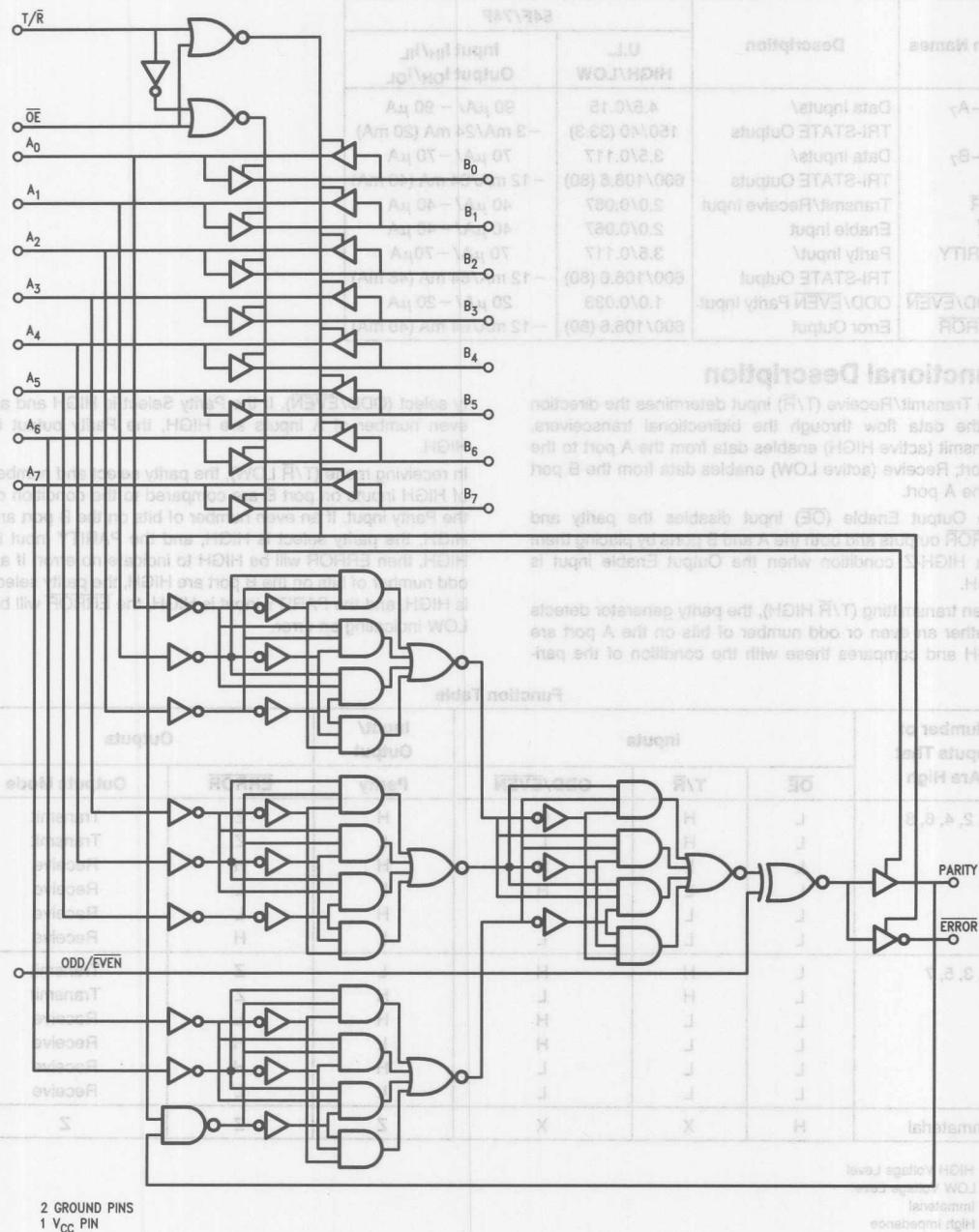
Inputs		Outputs
$\bar{OE}$	$T/\bar{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High-Z State

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

## Functional Block Diagram



**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max)

twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA (A <sub>n</sub> )
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA (A <sub>n</sub> , B <sub>n</sub> , Parity, ERROR)
		54F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = −12 mA (B <sub>n</sub> , Parity, ERROR)
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA (A <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA (A <sub>n</sub> , B <sub>n</sub> , Parity, ERROR)
		74F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = −15 mA (B <sub>n</sub> , Parity, ERROR)
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA (A <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA (A <sub>n</sub> )
		54F 10% V <sub>CC</sub>		0.55			I <sub>OL</sub> = 48 mA (B <sub>n</sub> , Parity, ERROR)
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA (A <sub>n</sub> )
		74F 10% V <sub>CC</sub>		0.55			I <sub>OL</sub> = 64 mA (B <sub>n</sub> , Parity, ERROR)
I <sub>IH</sub>	Input HIGH Current			20 40	μA	Max	V <sub>IN</sub> = 2.7V (ODD/EVEN) V <sub>IN</sub> 2.7V (T/R, OE)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			100	μA	V <sub>CC</sub> = 0	V <sub>IN</sub> = 7.0V (T/R, OE, ODD/EVEN)
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)		1.0 2.0		mA	Max	V <sub>IN</sub> = 5.5V (Parity, B <sub>n</sub> ) V <sub>IN</sub> = 5.5V (A <sub>n</sub> )
I <sub>IL</sub>	Input LOW Current		−20 −40		μA	Max	V <sub>IN</sub> = 0.5V (ODD/EVEN) V <sub>IN</sub> = 0.5V (T/R, OE)
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V (ERROR)
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V (ERROR)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70 90	μA	Max	V <sub>I/O</sub> = 2.7V (B <sub>n</sub> , Parity) V <sub>I/O</sub> = 2.7V (A <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			−70 −90	μA	Max	V <sub>I/O</sub> = 0.5V (B <sub>n</sub> , Parity) V <sub>I/O</sub> = 0.5V (A <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current	−60 −100	−150 −225		mA	Max	V <sub>OUT</sub> = 0V (A <sub>n</sub> ) V <sub>OUT</sub> = 0V (B <sub>n</sub> , Parity, ERROR)
I <sub>CEx</sub>	Output HIGH Leakage Current		250		μA	Max	V <sub>OUT</sub> = V <sub>CC</sub> (ERROR)
			1.0		mA	Max	V <sub>OUT</sub> = V <sub>CC</sub> (B <sub>n</sub> , Parity)
			2.0		mA	Max	V <sub>OUT</sub> = V <sub>CC</sub> (A <sub>n</sub> )
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V (A <sub>n</sub> , B <sub>n</sub> , Parity, ERROR)
I <sub>CCH</sub>	Power Supply Current		101	125	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		112	150	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		109	145	mA	Max	V <sub>O</sub> = HIGH Z

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n$ to $B_n$ , $B_n$ to $A_n$	2.5 3.0	4.5 4.9	8.0 7.5	2.5 3.0	9.5 8.5	2.5 3.0	9.0 8.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n$ to Parity	6.5 7.0	10.1 10.9	14.0 15.0	5.5 5.5	18.0 20.5	6.0 6.0	16.0 16.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay ODD/EVEN to PARITY	4.5 4.5	7.8 8.8	11.0 12.0	4.0 4.5	14.0 16.5	4.0 4.5	13.0 13.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay ODD/EVEN to ERROR	4.5 4.5	7.5 8.2	11.0 12.0	4.0 4.5	14.0 16.5	4.0 4.5	13.0 13.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $B_n$ to ERROR	8.0 8.0	14.0 15.0	20.5 21.5	7.5 7.5	27.0 28.5	7.5 7.5	23.0 23.5	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay PARITY to ERROR	7.0 7.5	10.8 11.8	15.5 16.5	6.0 6.5	20.0 22.0	6.0 7.5	17.0 18.5	ns	2-3
$t_{pZH}$ $t_{pZL}$	Output Enable Time $\overline{OE}$ to $A_n/B_n$	3.0 4.0	5.0 6.5	8.0 10.0	2.5 3.5	11.0 13.5	2.5 3.5	9.5 11.0	ns	2-5
$t_{pHZ}$ $t_{pLZ}$	Output Disable Time $\overline{OE}$ to $A_n/B_n$	1.0 1.0	4.5 4.9	8.0 7.5	1.0 1.0	9.5 8.5	1.0 1.0	9.0 8.0	ns	2-5
$t_{pZH}$ $t_{pZL}$	Output Enable Time $\overline{OE}$ to ERROR (Note 1)	3.0 4.0	5.0 7.7	8.0 10.0	2.5 3.5	11.0 13.5	2.5 3.5	9.5 11.0	ns	2-5
$t_{pHZ}$ $t_{pLZ}$	Output Disable Time $\overline{OE}$ to ERROR	1.0 1.0	4.5 4.9	8.0 7.5	1.0 1.0	9.5 8.5	1.0 1.0	9.0 8.0	ns	2-5
$t_{pZH}$ $t_{pZL}$	Output Enable Time $\overline{OE}$ to PARITY	3.0 4.0	5.0 7.7	8.0 10.0	2.5 3.5	11.0 13.5	2.5 3.5	9.5 11.0	ns	2-5
$t_{pHZ}$ $t_{pLZ}$	Output Disable Time $\overline{OE}$ to PARITY	1.0 1.0	4.6 5.1	8.0 7.5	1.0 1.0	9.5 8.5	1.0 1.0	9.0 8.0	ns	2-5

**Note 1:** These delay times reflect the TRI-STATE recovery time only and not the signal time through the buffers or the parity check circuitry. To assure VALID information at the ERROR pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the ERROR output after the ERROR pin has been enabled (Output Enable times). VALID data at the ERROR pin  $\geq$  (A to PARITY) + (Output Enable Time).

## 54F/74F673A

### 16-Bit Serial-In, Serial/Parallel-Out Shift Register

#### General Description

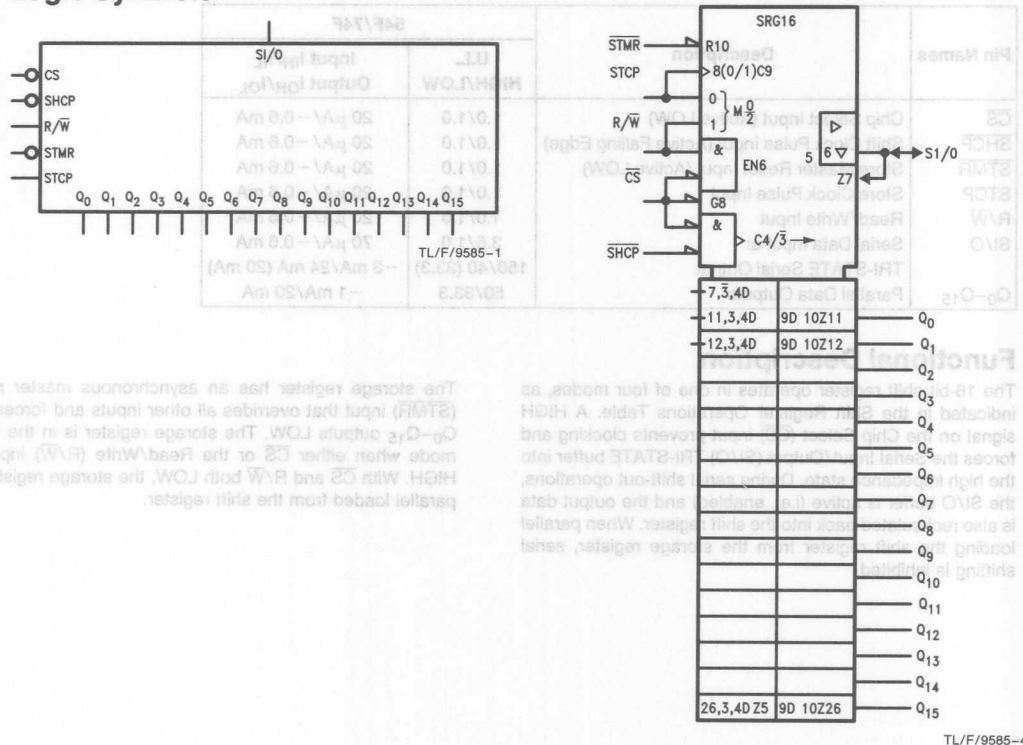
The 'F673A contains a 16-bit serial-in, serial-out shift register and a 16-bit parallel-out storage register. A single pin serves either as an input for serial entry or as a TRI-STATE® serial output. In the Serial-out mode, the data recirculates in the shift register. By means of a separate clock, the contents of the shift register are transferred to the storage register for parallel outputting. The contents of the storage register can also be parallel loaded back into the shift register. A HIGH signal on the Chip Select input prevents both shifting and parallel transfer. The storage register may be cleared via STMR.

#### Features

- Serial-to-parallel converter
- 16-bit serial I/O shift register
- 16-bit parallel-out storage register
- Recirculating serial shifting
- Recirculating parallel transfer
- Common serial data I/O pin
- Slim 24 lead package

**Ordering Code:** See Section 5

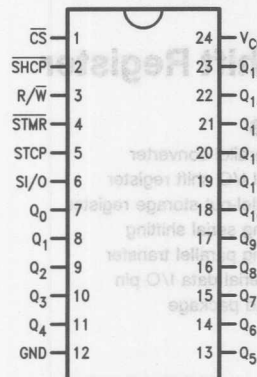
#### Logic Symbols



TL/F/9585-4

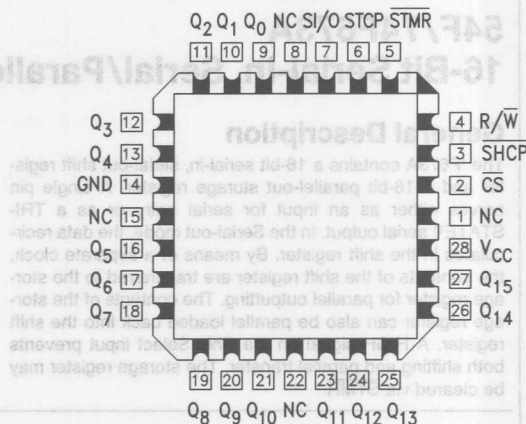


# Pin Assignment for DIP, SOIC and Flatpak



TL/F/9585-2

# Pin Assignment for LCC



TL/F/9585-3

## Unit Loading/Fan Out: See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{SHCP}$	Shift Clock Pulse Input (Active Falling Edge)	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{STMR}$	Store Master Reset Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$\overline{STCP}$	Store Clock Pulse Input	1.0/1.0	20 $\mu A$ / -0.6 mA
$R/\overline{W}$	Read/Write Input	1.0/1.0	20 $\mu A$ / -0.6 mA
$SI/O$	Serial Data Input or	3.5/1.0	70 $\mu A$ / -0.6 mA
	TRI-STATE Serial Output	150/40 (33.3)	-3 mA/24 mA (20 mA)
$Q_0-Q_{15}$	Parallel Data Outputs	50/33.3	-1 mA/20 mA

## Functional Description

The 16-bit shift register operates in one of four modes, as indicated in the Shift Register Operations Table. A HIGH signal on the Chip Select ( $\overline{CS}$ ) input prevents clocking and forces the Serial Input/Output ( $SI/O$ ) TRI-STATE buffer into the high impedance state. During serial shift-out operations, the  $SI/O$  buffer is active (i.e., enabled) and the output data is also recirculated back into the shift register. When parallel loading the shift register from the storage register, serial shifting is inhibited.

The storage register has an asynchronous master reset ( $\overline{STMR}$ ) input that overrides all other inputs and forces the  $Q_0-Q_{15}$  outputs LOW. The storage register is in the Hold mode when either  $\overline{CS}$  or the Read/Write ( $R/\overline{W}$ ) input is HIGH. With  $\overline{CS}$  and  $R/\overline{W}$  both LOW, the storage register is parallel loaded from the shift register.

Shift Register Operations Table

Control Inputs				SI/O Status	Operating Mode
$\overline{CS}$	R/W	SHCP	STCP		
H	X	X	X	High Z	Hold
L	L	X	X	Data In	Serial Load
L	H	$\sim$	L	Data Out	Serial Output with Recirculation
L	H	$\sim$	H	Active	Parallel Load; No Shifting

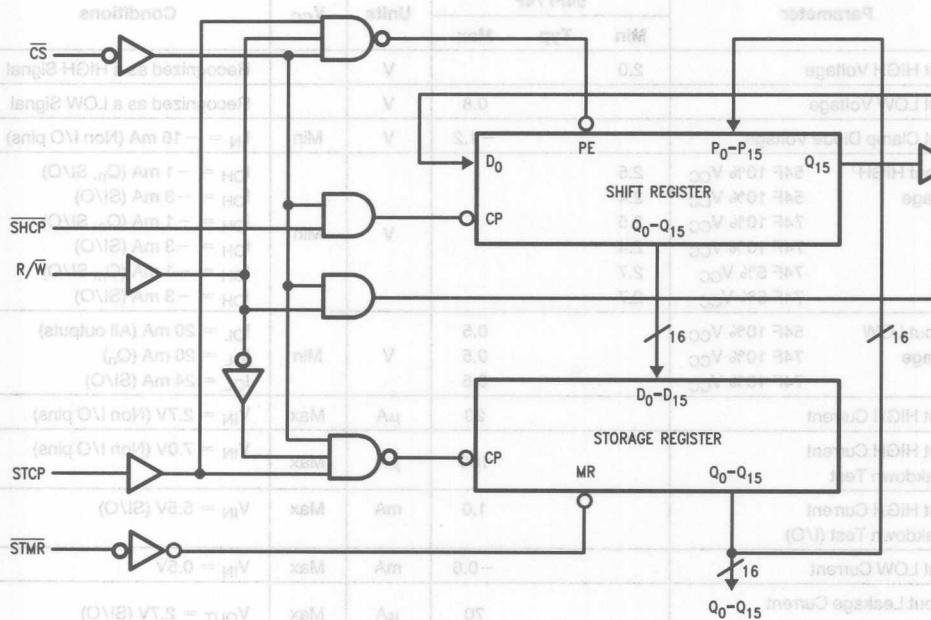
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 $\sim$  = HIGH-to-LOW Transition

Storage Register Operations Table

Control Inputs				Operating Mode
STMR	$\overline{CS}$	R/W	STCP	
L	X	X	X	Reset; Outputs LOW
H	H	X	X	Hold
H	X	H	X	Hold
H	L	L	$\sim$	Parallel Load

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 $\sim$  = LOW-to-HIGH Transition

## Block Diagram



TL/F/9585-5

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	-0.5V to V <sub>CC</sub>
Standard Output TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	-55°C to +125°C
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA (Non I/O pins)
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	I <sub>OH</sub> = -1 mA (Q <sub>n</sub> , SI/O) I <sub>OH</sub> = -3 mA (SI/O) I <sub>OH</sub> = -1 mA (Q <sub>n</sub> , SI/O) I <sub>OH</sub> = -3 mA (SI/O) I <sub>OH</sub> = -1 mA (Q <sub>n</sub> , SI/O) I <sub>OH</sub> = -3 mA (SI/O)
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA (All outputs) I <sub>OL</sub> = 20 mA (Q <sub>n</sub> ) I <sub>OL</sub> = 24 mA (SI/O)
I <sub>IH</sub>	Input HIGH Current			20	μA	Max	V <sub>IN</sub> = 2.7V (Non I/O pins)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			100	μA	Max	V <sub>IN</sub> = 7.0V (Non I/O pins)
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)			1.0	mA	Max	V <sub>IN</sub> = 5.5V (SI/O)
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (SI/O)
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			-650	μA	Max	V <sub>OUT</sub> = 0.5V (SI/O)
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CEX</sub>	Output HIGH Leakage Current			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current		114	172	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		114	172	mA	Max	V <sub>O</sub> = LOW

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	100	130				85		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	3.0	8.0	10.5			2.5	12.0	ns	2-3
$t_{\text{PHL}}$	STCP to $Q_n$	3.0	10.5	13.5			2.5	15.0		
$t_{\text{PHL}}$	Propagation Delay	6.0	16.5	20.5			5.5	22.5	ns	2-3
$t_{\text{PLH}}$	Propagation Delay	4.0	6.5	8.5			3.5	9.5	ns	2-3
$t_{\text{PHL}}$	SHCP to SI/O	4.5	8.0	10.5			4.0	12.0		
$t_{\text{PZH}}$	Output Enable Time	5.0	8.5	11.0			4.0	12.5	ns	2-5
$t_{\text{PZL}}$	CS to SI/O	5.5	9.0	11.5			4.5	13.0		
$t_{\text{PHZ}}$	Output Disable Time	3.5	5.5	7.5			3.0	8.5	ns	2-5
$t_{\text{PLZ}}$	$\overline{\text{CS}}$ to SI/O	3.0	4.5	6.5			2.5	7.5		
$t_{\text{PZH}}$	Output Enable Time	4.5	7.5	9.5			4.0	10.5	ns	2-5
$t_{\text{PZL}}$	R/W to SI/O	4.5	8.0	10.0			4.0	11.5		
$t_{\text{PHZ}}$	Output Disable Time	3.0	5.5	7.0			2.5	8.0	ns	2-5
$t_{\text{PLZ}}$	R/W to SI/O	2.5	4.0	5.5			2.0	6.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	54F/74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $\overline{\text{CS}}$ or R/W to STCP	3.5 6.0				4.0 7.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $\overline{\text{CS}}$ or R/W to STCP	0 0				0 0			
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW SI/O to SHCP	3.0 3.0				3.5 3.5		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW SI/O to SHCP	3.0 3.0				3.5 3.5			



## 54F/74F675A

### 16-Bit Serial-In, Serial/Parallel-Out Shift Register

#### General Description

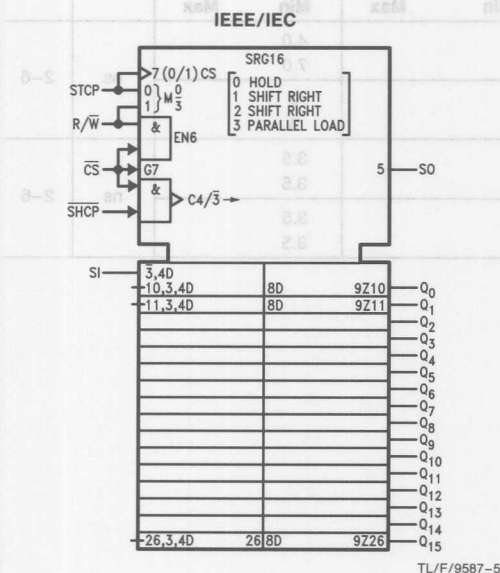
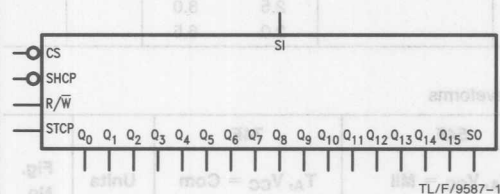
The 'F675A contains a 16-bit serial in/serial out shift register and a 16-bit parallel out storage register. Separate serial input and output pins are provided for expansion to longer words. By means of a separate clock, the contents of the shift register are transferred to the storage register. The contents of the storage register can also be loaded back into the shift register. A HIGH signal on the Chip Select input prevents both shifting and parallel loading.

#### Features

- Serial-to-parallel converter
- 16-Bit serial I/O shift register
- 16-Bit parallel out storage register
- Recirculating parallel transfer
- Expandable for longer words
- Slim 24 lead package
- 'F675A version prevents false clocking through CS or R/W inputs

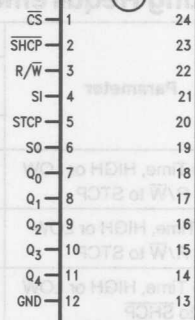
#### Ordering Code: See Section 5

#### Logic Symbols

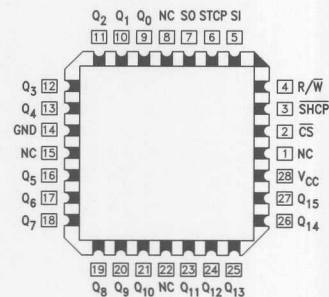


#### Connection Diagrams

##### Pin Assignment for DIP, SOIC and Flatpak



##### Pin Assignment for LCC



# Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
SI	Serial Data Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{SHCP}$	Shift Clock Pulse Input (Active Falling Edge)	1.0/1.0	20 $\mu$ A/ -0.6 mA
STCP	Store Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/ -0.6 mA
R/W	Read/Write Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
SO	Serial Data Output	50/33.3	-1 mA/20 mA
$Q_0-Q_{15}$	Parallel Data Outputs	50/33.3	-1 mA/20 mA

## Functional Description

The 16-Bit shift register operates in one of four modes, as determined by the signals applied to the Chip Select ( $\overline{CS}$ ), Read/Write (R/W) and Store Clock Pulse (STCP) input. State changes are indicated by the falling edge of the Shift Clock Pulse ( $\overline{SHCP}$ ). In the Shift Right mode, data enters  $D_0$  from the Serial Input (SI) pin and exits from  $Q_{15}$  via the Serial Data Output (SO) pin. In the Parallel Load mode, data from the storage register outputs enter the shift register and serial shifting is inhibited.

The storage register is in the Hold mode when either  $\overline{CS}$  or R/W is HIGH. With  $\overline{CS}$  and R/W both LOW, the storage register is parallel loaded from the shift register on the rising edge of STCP.

To prevent false clocking of the shift register,  $\overline{SHCP}$  should be in the LOW state during a LOW-to-HIGH transition of  $\overline{CS}$ . To prevent false clocking of the storage register, STCP should be LOW during a HIGH-to-LOW transition of  $\overline{CS}$  if R/W is LOW, and should also be LOW during a HIGH-to-LOW transition of R/W if  $\overline{CS}$  is LOW.

Shift Register Operations Table

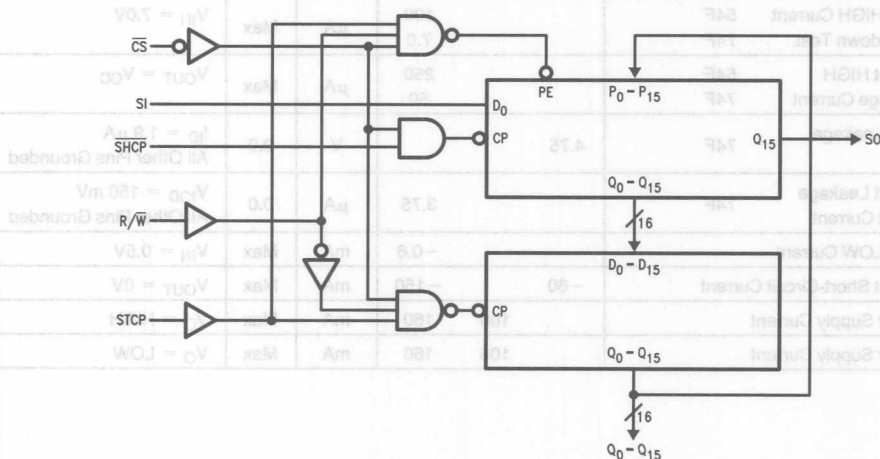
Control Inputs				Operating Mode
$\overline{CS}$	R/W	$\overline{SHCP}$	STCP	
H	X	X	X	Hold
L	L	—	X	Shift Right
L	H	—	L	Shift Right
L	H	—	H	Parallel Load, No Shifting

Storage Register Operations Table

Inputs			Operating Mode
$\overline{CS}$	R/W	STCP	
H	X	X	Hold
L	H	X	Hold
L	L	—	Parallel Load

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
— = LOW-to-HIGH Transition  
— = HIGH-to-LOW Transition

## Logic Diagram



TL/F/9587-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



**Office/Distributors for availability and specifications.**

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IIN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0			V <sub>IN</sub> = 2.7V
		74F		5.0	μA	Max	
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100			V <sub>IN</sub> = 7.0V
		74F		7.0	μA	Max	
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250			V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50	μA	Max	
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		106	160	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		106	160	mA	Max	V <sub>O</sub> = LOW

Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**Functional Description**

The 18-B shift register operates in one of four modes as determined by the signals applied to the Chip Select (CS), Read/Write (R/W), and Store Clock Pulse (STCP) inputs. State changes are indicated by the falling edge of the Shift Clock Pulse (SHCP). In the Shift Right mode, data enters from the Serial Input (SI) pin and exits from Q<sub>15</sub> via the Serial Data Output (SDO) pin in the Parallel Load mode, data from the storage register outputs enter the shift register and serial shifting is inhibited.

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	100	130				85		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	3.0	8.0	10.5			2.5	12.0		
$t_{\text{PHL}}$	STCP to $Q_n$	3.0	10.5	13.5			2.5	15.0	ns	2-3
$t_{\text{PLH}}$	Propagation Delay	4.0	7.0	9.5			3.5	10.5		
$t_{\text{PHL}}$	SHCP to SO	4.5	8.0	10.5			4.0	12.0	ns	2-3

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	3.5				4.0		ns	2-6
$t_s(\text{L})$	$\overline{\text{CS}}$ or R/W to STCP	5.5				6.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0				0		ns	2-6
$t_h(\text{L})$	$\overline{\text{CS}}$ or R/W to STCP	0				0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	3.0				3.5		ns	2-6
$t_s(\text{L})$	SI to $\overline{\text{SHCP}}$	3.0				3.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	3.0				3.5		ns	2-6
$t_h(\text{L})$	SI to $\overline{\text{SHCP}}$	3.0				3.5			
$t_s(\text{H})$	Setup Time, HIGH or LOW	6.5				7.5		ns	2-6
$t_s(\text{L})$	R/W to $\overline{\text{SHCP}}$	9.0				10.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0				0		ns	2-6
$t_h(\text{L})$	R/W to $\overline{\text{SHCP}}$	0				0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	7.0				8.0		ns	2-6
$t_s(\text{L})$	STCP to $\overline{\text{SHCP}}$	7.0				8.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	0				0		ns	2-6
$t_h(\text{L})$	STCP to $\overline{\text{SHCP}}$	0				0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	3.0				3.5		ns	2-6
$t_s(\text{L})$	$\overline{\text{CS}}$ to $\overline{\text{SHCP}}$	3.0				3.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	3.0				3.5		ns	2-6
$t_h(\text{L})$	$\overline{\text{CS}}$ to $\overline{\text{SHCP}}$	3.0				3.5			
$t_w(\text{H})$	$\overline{\text{SHCP}}$ Pulse Width	5.0				6.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	5.0				6.0			
$t_w(\text{H})$	STCP Pulse Width	6.0				7.0		ns	2-6
$t_w(\text{L})$	HIGH or LOW	5.0				6.0			
$t_s(\text{L})$	$\overline{\text{SHCP}}$ to STCP	8.0				9.0		ns	2-6
$t_h(\text{H})$	$\overline{\text{SHCP}}$ to STCP	0.0				0.0		ns	2-6


**54F/74F676**

# **16-Bit Serial/Parallel-In, Serial-Out Shift Register**

## **General Description**

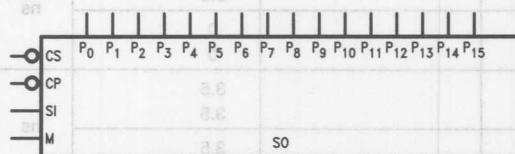
The 'F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the Mode (M) input is HIGH, information present on the parallel data ( $P_0$ – $P_{15}$ ) inputs is entered on the falling edge of the Clock Pulse (CP) input signal. When M is LOW, data is shifted out of the most significant bit position while information present on the Serial (SI) input shifts into the least significant bit position. A HIGH signal on the Chip Select ( $\overline{CS}$ ) input prevents both parallel and serial operations.

## **Features**

- 16-bit parallel-to-serial conversion
- 16-bit serial-in, serial-out
- Chip select control
- Slim 24 lead 300 mil package

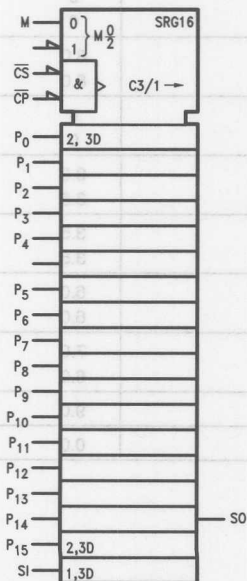
**Ordering Code:** See Section 5

## **Logic Symbols**



TL/F/9588-1

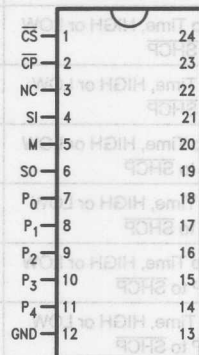
### **IEEE/IEC**



TL/F/9588-4

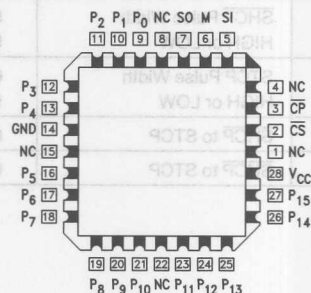
## **Connection Diagrams**

### **Pin Assignment for DIP, SOIC and Flatpak**



TL/F/9588-2

### **Pin Assignment for LCC**



TL/F/9588-3

# Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
P <sub>0</sub> –P <sub>15</sub>	Parallel Data Inputs	1.0/1.0	20 $\mu$ A / –0.6 mA
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/1.0	20 $\mu$ A / –0.6 mA
$\overline{CP}$	Clock Pulse Input (Active LOW)	1.0/1.0	20 $\mu$ A / –0.6 mA
M	Mode Select Input	1.0/1.0	20 $\mu$ A / –0.6 mA
SI	Serial Data Input	1.0/1.0	20 $\mu$ A / –0.6 mA
SO	Serial Output	50/33.3	–1 mA/20 mA

## Functional Description

The 16-bit shift register operates in one of three modes, as indicated in the Shift Register Operations Table.

**HOLD**—a HIGH signal on the Chip Select ( $\overline{CS}$ ) input prevents clocking, and data is stored in the sixteen registers.

**Shift/Serial Load**—data present on the SI pin shifts into the register on the falling edge of  $\overline{CP}$ . Data enters the Q<sub>0</sub> position and shifts toward Q<sub>15</sub> on successive clocks, finally appearing on the SO pin.

**Parallel Load**—data present on P<sub>0</sub>–P<sub>15</sub> are entered into the register on the falling edge of  $\overline{CP}$ . The SO output represents the Q<sub>15</sub> register output.

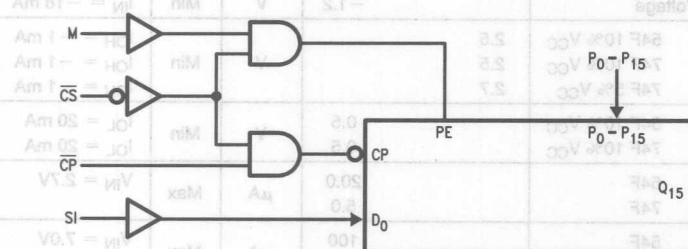
To prevent false clocking,  $\overline{CP}$  must be LOW during a LOW-to-HIGH transition of  $\overline{CS}$ .

Shift Register Operations Table

Control Input			Operating Mode
$\overline{CS}$	M	$\overline{CP}$	
H	X	X	Hold Shift/Serial Load Parallel Load
L	L	$\sim$	
L	H	$\sim$	

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
 $\sim$  = HIGH-to-LOW Transition

## Block Diagram



TL/F/9588-5

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	-0.5V to V <sub>CC</sub>
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA, All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV, All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current			72	mA	Max	

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	-55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	100	110		45		90		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	4.5	9.0	11.0	4.5	17.0	4.5	12.0	ns	2-3
$t_{\text{PHL}}$	$\overline{\text{CP}}$ to $\text{SO}$	5.0	9.0	12.5	5.0	14.5	5.0	13.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	4.0		4.0		4.0		ns	2-6
$t_s(\text{L})$	SI to $\overline{\text{CP}}$	4.0		4.0		4.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	4.0		4.0		4.0		ns	2-6
$t_h(\text{L})$	SI to $\overline{\text{CP}}$	4.0		4.0		4.0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	3.0		3.0		3.0		ns	2-6
$t_s(\text{L})$	$P_n$ to $\overline{\text{CP}}$	3.0		3.0		3.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	4.0		4.0		4.0		ns	2-6
$t_h(\text{L})$	$P_n$ to $\overline{\text{CP}}$	4.0		4.0		4.0			
$t_s(\text{H})$	Setup Time, HIGH or LOW	8.0		8.0		8.0		ns	2-6
$t_s(\text{L})$	M to $\overline{\text{CP}}$	8.0		8.0		8.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0		2.0		2.0		ns	2-6
$t_h(\text{L})$	M to $\overline{\text{CP}}$	2.0		2.0		2.0			
$t_s(\text{L})$	Setup Time, LOW $\overline{\text{CS}}$ to $\overline{\text{CP}}$	10.0		12.0		10.0		ns	2-6
$t_h(\text{H})$	Hold Time, HIGH $\overline{\text{CS}}$ to $\overline{\text{CP}}$	10.0		10.0		10.0			
$t_w(\text{H})$	$\overline{\text{CP}}$ Pulse Width	4.0		5.0		4.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	6.0		9.0		6.0			





# 54F/74F779

## 8-Bit Bidirectional Binary Counter with TRI-STATE® Outputs

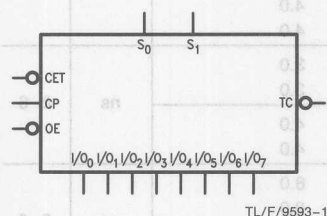
### General Description

The 'F779 is a fully synchronous 8-stage up/down counter with multiplexed TRI-STATE I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pins ( $S_0$ ,  $S_1$ ). The device also features carry lookahead for easy cascading. All state changes are initiated by the rising edge of the clock.

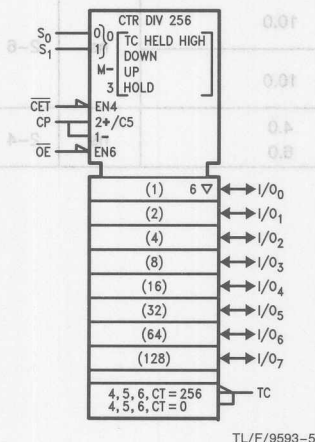
### Features

- Multiplexed TRI-STATE I/O ports
- Built-in lookahead carry capability
- Count frequency 100 MHz typ
- Supply current 80 mA typ

### Logic Symbols

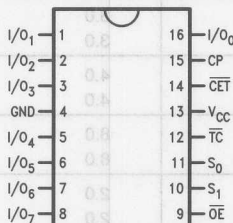


#### IEEE/IEC



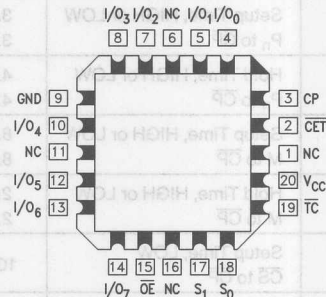
### Connection Diagrams

#### Pin Assignment for DIP, SOIC and Flatpak



TL/F/9593-2

#### Pin Assignment for LCC and PCC



TL/F/9593-3



## 54F/74F784

### 8-Bit Serial/Parallel Multiplier with Adder/Subtractor

#### General Description

The 'F784 is an 8-bit by 1-bit sequential logic element that multiplies two numbers represented in twos complement notation. The device implements Booth's algorithm internally to produce a twos complement product that needs no subsequent correction. In addition to the serial product output (SP), an  $S \pm B$  output is obtained with an internal adder/subtractor stage which adds a B bit to the SP product. Parallel inputs accept and store an 8-bit multiplicand ( $X_0-X_7$ ). The add/subtract ( $\bar{A}/S$ ),  $B_n$  and  $B_{n-1}$  inputs control the internal adder/subtractor stage. The multiplier word is then applied to the Y input in a serial bit stream, least significant bit first. The product is clocked out at the SP output and the product  $\pm B$  at the  $S \pm B$  output delayed by one clock cycle. Both appear least significant bit first.

The K input is used for expansion to longer X words, using two or more 'F784 devices by connecting the output (SP) of

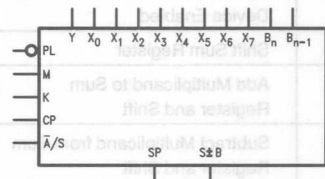
one device to the K input of the other device. The Mode Control (M) input is used to establish the most significant device. An asynchronous Parallel Load (PL) input clears the internal flip-flops to the start condition and enables the X latches to accept new multiplicand data. The Parallel Load (PL) also clears the outputs (SP and  $S \pm B$ ).

#### Features

- Twos complement multiplication
- 8-bit by 1-bit sequential logic element
- Includes product output (SP) and product  $\pm B$  output ( $S \pm B$ )
- Parallel inputs accept and store an 8-bit multiplicand ( $X_0-X_7$ )
- K input is used for expansion to longer X words
- Combines the 'F384 and 'F385 in one chip

**Ordering Code:** See Section 5

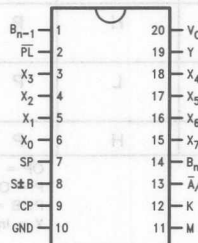
#### Logic Symbol



TL/F/10230-1

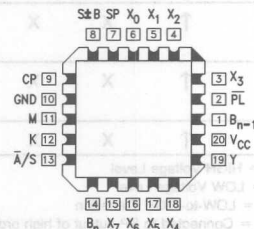
#### Connection Diagrams

Pin Assignment for DIP and SOIC



TL/F/10230-2

Pin Assignment for LCC



TL/F/10230-3

**Input Loading/Fan-Out:** See Section 2

Pin Names	Description	54F/74F (U.L.) High/Low	$I_{IH}/I_{IL}$ $I_{OH}/I_{OL}$
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/ -0.6 mA
K	Serial Expansion Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
M	Mode Control Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
PL	Asynchronous Parallel Load Input (Active LOW)	1.0/2.0	20 $\mu$ A/ -1.2 mA
$X_0-X_7$	Multiplicand Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
Y	Serial Multiplier Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\bar{A}/S$	Add/Subtract	1.0/1.0	20 $\mu$ A/ -0.6 mA
$B_n$	Serial B Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
$B_{n-1}$	Delayed Serial B Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
$S \pm B$	Serial $X \cdot Y \pm B$ Output	50/33.3	-1 mA/20 mA
SP	Serial $X \cdot Y$ Product Output	50/33.3	-1 mA/20 mA

## Functional Description

The 'F784 is a serial-parallel 8-bit multiplier. Also included is an adder/subtractor stage. The X word (multiplicand) is loaded into a register while simultaneously clearing the arithmetic cell flip-flops in preparation for a multiplication. The Y word (multiplier) is clocked in serially. (See Figure A). Expansion capability is provided via the M and K inputs. The K (cascade) input is connected to the  $S_0$  output of the more significant chip. The M (mode) input is used to determine whether the multiplicand is to be treated as a two's complement or unsigned number.

The 'F784 has logic to enable complex arithmetic to be performed. A serial adder/subtractor enables constants to be added to the product. Typically this feature would be used in FFT butterfly networks to reduce package count and power.

Two outputs are provided: the product XY and the product  $XY \pm B$ . Because of the internal adder/subtractor, a speed advantage is gained when using the 'F784 over using a separate adder and multiplier chip. (Refer to Figure B).

During a multiplication operation, the first clock cycle is used to load both the X word (multiplicand) and the first bit

of the Y word (operand) into the input registers. At this time there is no valid data at the SP output so that B bits added will not give the correct sum output. In order to load the first B bit on the same clock as X and Y, a  $B_{n-1}$  input is provided which delays the B data by one clock cycle. Thus, a valid output results.

Inputs			Function
$\bar{A}/S$	$B_n$	$B_{n-1}$	
L	H	$C_n$	Add $C_n$ to product ( $C_n$ loaded at the same time as $Y_n$ )
L	$C_n$	H	Add $C_n$ to product ( $C_n$ must be delayed one clock cycle)
H	H	$C_n$	Subtract $C_n$ from product ( $C_n$ loaded at the same time as $Y_n$ )
H	$C_n$	H	Subtract $C_n$ from product ( $C_n$ must be delayed one clock cycle)

L = LOW Voltage Level H = HIGH Voltage Level  $C_n$  = Constant

Function Table

Inputs						Internal	Outputs		Function
$\bar{P}L$	CP	K	M	$X_i$	Y	$Y_{a-1}$	SP	$S \pm B$	
X	X	L	L	X	X	X	X	X	Most Significant Multiplier Device
X	X	CS	H	X	X	X	X	X	Devices Cascaded in Multiplier String
L	X	X	X	OP	X	L	L	L	Load New Multiplicand and Clear Internal Sum and Carry Registers
H	X	X	X	X	X	X	X	X	Device Enabled
H	$\uparrow$	X	X	X	L	L	P	$P \pm B$	Shift Sum Register
H	$\uparrow$	X	X	X	L	H	P	$P \pm B$	Add Multiplicand to Sum Register and Shift
H	$\uparrow$	X	X	X	H	L	P	$P \pm B$	Subtract Multiplicand from Sum Register and Shift
H	$\uparrow$	X	X	X	H	H	P	$P \pm B$	Shift Sum Register

H = HIGH Voltage Level

L = LOW Voltage Level

$\uparrow$  = LOW-to-HIGH Transition

CS = Connected to SP output of high order device

OP =  $X_i$  latches open for new data ( $i = 0-7$ )

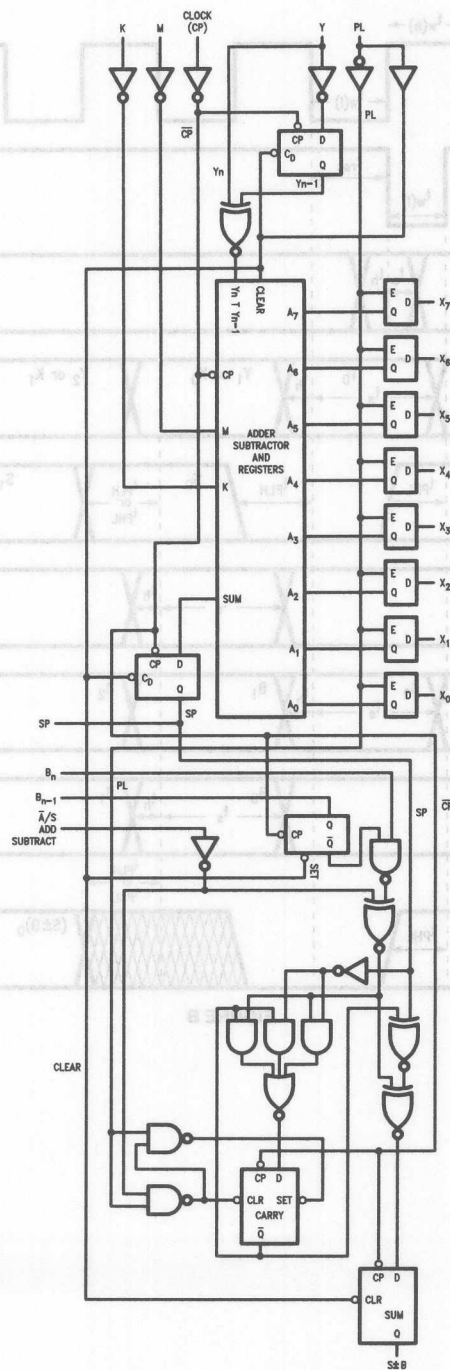
P = Output as required per Booth's algorithm

$P \pm B$  = Product  $\pm$  a constant (delayed one clock cycle)

X = Immaterial

Pin	Description	High/Low	High/Low (V <sub>CC</sub> )
CP	Clock/Pulse Input (Active Rising Edge)	High/Low	1.0V/0.0
K	Serial Expansion Input	High/Low	1.0V/0.0
M	Mode Control Input	High/Low	1.0V/0.0
$\bar{P}L$	Asynchronous Parallel Load Input (Active LOW)	High/Low	1.0V/0.0
$X_{a-1}$	Multiplicand Data Input	High/Low	1.0V/0.0
Y	Serial Multiplier Input	High/Low	1.0V/0.0
$\bar{A}/S$	Add/Subtract	High/Low	1.0V/0.0
$B_n$	Serial B Input	High/Low	1.0V/0.0
$B_{n-1}$	Delayed Serial B Input	High/Low	1.0V/0.0
$S \pm B$	Serial $X \pm Y \pm B$ Output	High/Low	1.0V/0.0
SP	Serial $X \times Y$ Product Output	High/Low	1.0V/0.0

# Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FIGURE A

TL/F/10230-4

## Timing Waveforms

Logic Diagram

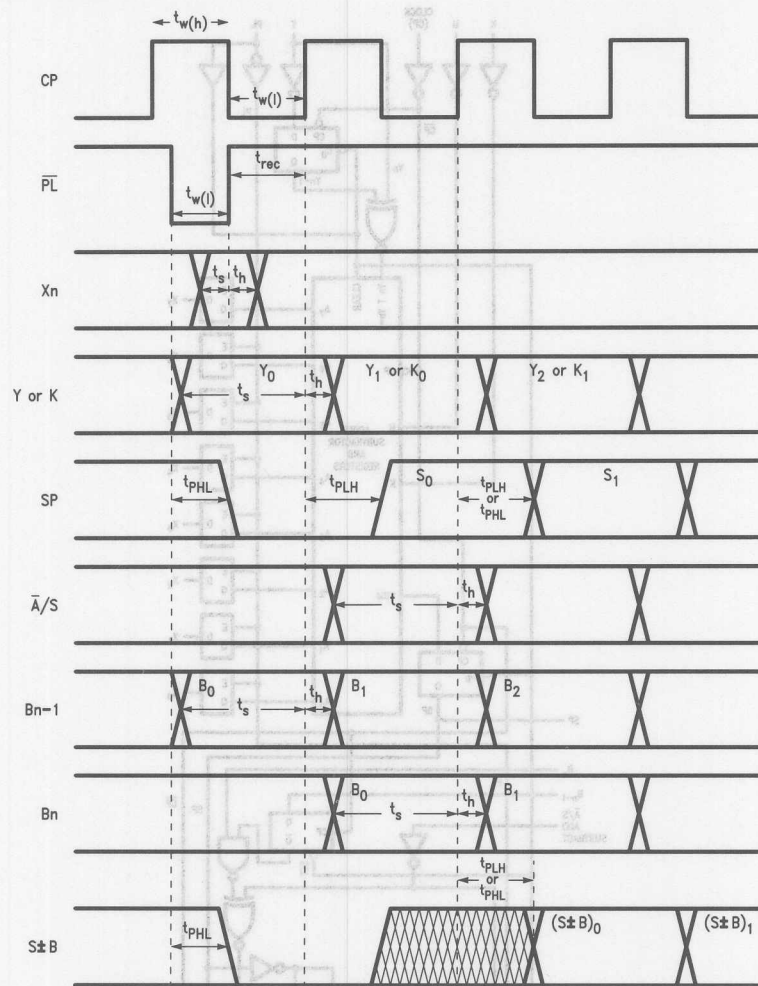


FIGURE B

TL/F/10230-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delay.

FIGURE A

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max)

twice the rated I<sub>OL</sub> (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>GEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V (Except PL)
				−1.2			V <sub>IN</sub> = 0.5V (PL)
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		70	100	mA	Max	V <sub>O</sub> = HIGH



**AC Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	50	65				50		MHz	2-1
t <sub>PHL</sub>	Propagation Delay PL to SP	6.0	10.0	13.0			5.0	14.5	ns	2-3
t <sub>PHL</sub>	Propagation Delay PL to S ± B	5.5	9.5	12.0			4.5	13.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to SP	4.0 4.5	6.5 8.0	9.0 10.5			3.5 4.0	10.0 12.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to S ± B	4.0 4.0	7.0 7.0	9.0 9.0			3.5 3.5	10.0 10.0	ns	2-3

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V			T <sub>A</sub> , V <sub>CC</sub> = Mil		T <sub>A</sub> , V <sub>CC</sub> = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW K to CP	9.0 9.0					10.0 10.0		ns	2-6
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW K to CP	2.0 2.0					2.0 2.0			
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW Y to CP	15.0 15.0					15.0 15.0		ns	2-6
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW Y to CP	2.0 2.0					2.0 2.0			
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW X to PL	3.0 6.0					4.0 7.0		ns	2-6
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW X to PL	2.0 4.0					2.0 4.0			
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW B <sub>n</sub> to CP	7.0 7.0					8.0 8.0		ns	2-6
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW B <sub>n</sub> to CP	0 0					0 0			
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW A/ $\overline{S}$ to CP	12.0 12.0					13.0 13.0		ns	2-6
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW A/ $\overline{S}$ to CP	0 0					0 0			
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW B <sub>n-1</sub> to CP	5.0 5.0					5.0 5.0		ns	2-6
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW B <sub>n-1</sub> to CP	1.0 1.0					2.0 2.0			
t <sub>W</sub> (L)	$\overline{PL}$ Pulse Width, LOW	6.5					7.0		ns	2-4
t <sub>W</sub> (H) t <sub>W</sub> (L)	CP Pulse Width HIGH or LOW	7.0 7.0					7.0 7.0		ns	2-4
t <sub>rec</sub>	Recovery Time $\overline{PL}$ to CP	6.0					10.0		ns	2-6

## 54F/74F794 8-Bit Register with Readback

### General Description

The 'F794 is an 8-bit register with readback capability designed to store data as well as read the register information back onto the data bus. The I/O bus (D bus) has TRI-STATE® outputs. Current sinking capability is 64 mA on both the D and Q busses.

Data is loaded into the registers on the low-to-high transition of the clock (CP). The output enable ( $\overline{OE}$ ) is used to enable data on  $D_0$ - $D_7$ . When  $\overline{OE}$  is low, the output of the registers is enabled on  $D_0$ - $D_7$ , enabling D as an output bus. When

Truth Table

Inputs		Outputs	
CP	$\overline{OE}$	D	Q
L or H or $\downarrow$	L	Q <sub>n</sub>	Q <sub>n</sub>
L or H or $\downarrow$	H	Q <sub>n</sub>	Q <sub>n</sub>
$\uparrow$	L	Q <sub>n</sub>	Q <sub>n</sub>
$\uparrow$	H	Q <sub>n</sub>	Q <sub>n</sub>

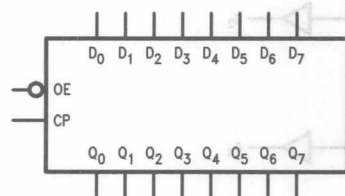
$\overline{OE}$  is high,  $D_0$ - $D_7$  are inputs to the registers configuring D as an input bus.

### Features

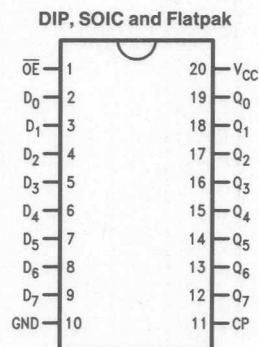
- TRI-STATE outputs on the I/O port
- D and Q output sink capability of 64 mA
- Guaranteed 4000V minimum ESD protection
- Functionally and pin equivalent to the 'LS794

**Ordering Code:** See Section 5

### Logic Symbol



### Connection Diagram



### Input Loading/Fan-Out

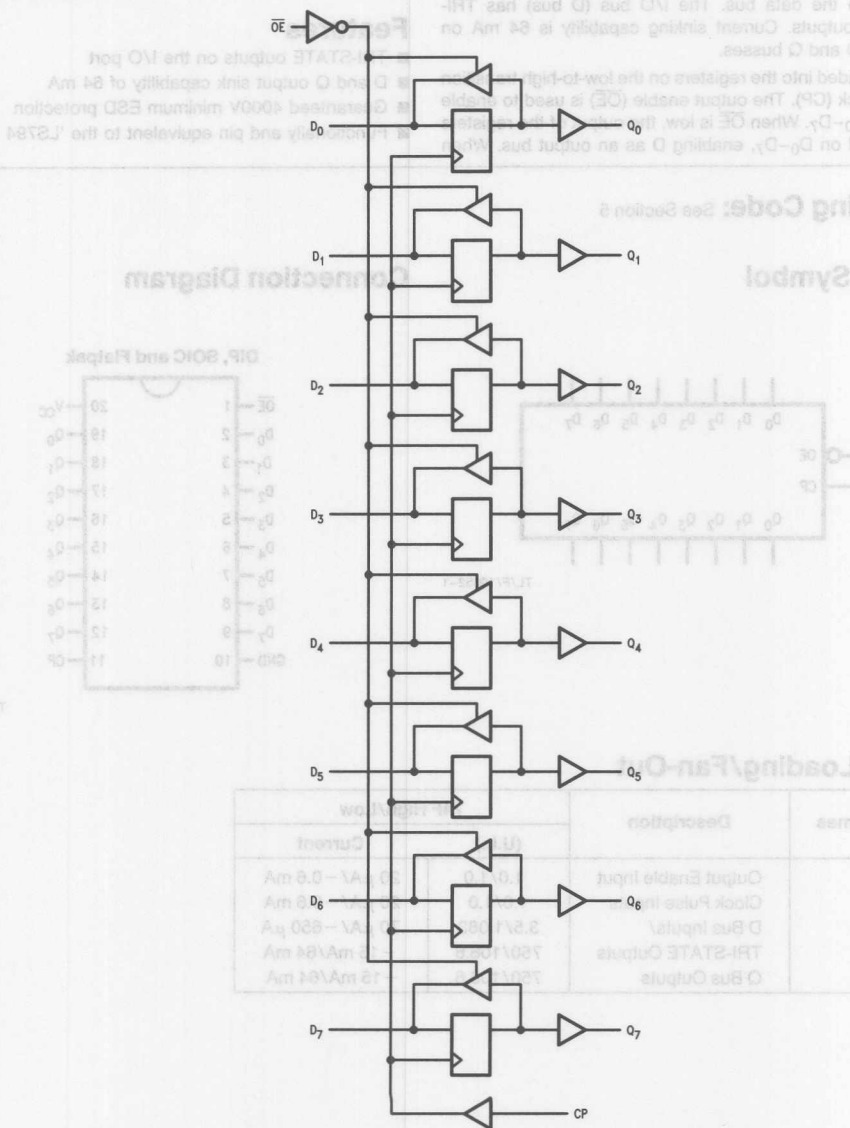
Pin Names	Description	74F High/Low	
		(U.L.)	Current
$\overline{OE}$	Output Enable Input	1.0/1.0	20 $\mu$ A / -0.6 mA
CP	Clock Pulse Inputs	1.0/1.0	20 $\mu$ A / -0.6 mA
$D_0$ - $D_7$	D Bus Inputs/ TRI-STATE Outputs	3.5/1.083	70 $\mu$ A / -650 $\mu$ A
$Q_0$ - $Q_7$	Q Bus Outputs	750/106.6	-15 mA/64 mA

## Truth Table

Inputs		Outputs	
CP	$\overline{OE}$	Q	D
L or H or $\downarrow$	L	$Q_n$	Output, Q
L or H or $\downarrow$	H	$Q_n$	Input
$\uparrow$	L	$Q_n$	Output, Q*
$\uparrow$	H	D	Input

\*In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at  $Q_n$ .

## Logic Diagram



TL/F/10652-3

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to + 150°C
Ambient Temperature under Bias	−55° to + 125°C
Junction Temperature under Bias	−55°C to + 175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to + 7.0V
Input Voltage (Note 2)	−0.5V to + 7.0V
Input Current (Note 2)	−30 mA to + 5.0 mA
ESD Last Passing Voltage (Min)	4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

Voltage Applied to Output	
In HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output	−0.5V to + 5.5V
TRI-STATE Output	−0.5V to + 5.5V
Current Applied to Output in LOW State (Max)	Twice the Rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to + 125°C
Commercial	0°C to 70°C
Supply Voltage	
Military	+ 4.5V to + 5.5V
Commercial	+ 4.5V to + 5.5V

## DC Characteristics over Operating Temperature Range unless otherwise specified

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.4 2.0	2.8 2.44		V	Min	I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −15 mA
V <sub>OL</sub>	Output LOW Voltage		0.45	0.55	V	Min	I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current			20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			100 7.0	μA	Max	V <sub>IN</sub> = 7.0V (OE, CP)
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)			1.0 0.5	mA	Max	V <sub>IN</sub> = 5.5V (D <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current			250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V (OE, CP)

# DC Characteristics over Operating Temperature Range unless other specified (Continued)

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
I <sub>OS</sub>	Output Short-Circuit Current	-100		-225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (Dn)
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			-650	μA	Max	V <sub>OUT</sub> = 0.5V (Dn)
V <sub>ID</sub>	Input Leakage Test 74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Circuit Leakage Current 74F			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>ZZ</sub>	Bus Drainage Test			100	μA	0.0	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current			65	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			80	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current			80	mA	Max	V <sub>O</sub> = HIGH Z

## AC Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil		T <sub>A</sub> , V <sub>CC</sub> = Comm C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f <sub>MAX</sub>	Max. Clock Frequency	90					90		MHz	2-1
t <sub>PLH</sub>	Propagation Delay	2.5		7.0			2.5	8.0	ns	2-3
t <sub>PHL</sub>	CP to Qn	2.5		8.0			2.5	9.0		
t <sub>PZH</sub>	Output Enable Time	2.3		8.5			2.0	9.0	ns	2-5
t <sub>PZL</sub>		2.0		10.0			2.0	10.5		
t <sub>PHZ</sub>	Output Disable Time	1.0		7.0			1.0	8.0	ns	2-5
t <sub>PLZ</sub>		1.0		7.0			1.0	8.0		
t <sub>s</sub> (H)	Setup Time, HIGH or LOW	4.0					4.0		ns	2-6
t <sub>s</sub> (L)	Bus to Clock	4.0					4.0			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	1.5					1.5		ns	2-6
t <sub>h</sub> (L)	Bus to Clock	1.5					1.5			
t <sub>w</sub> (H)	Clock Pulse Width	5.8					5.8		ns	2-14
	HIGH or LOW	5.8					5.8			

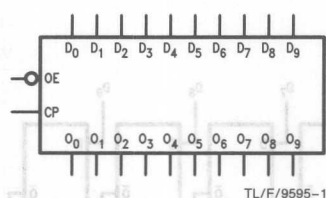
# 54F/74F821 10-Bit D-Type Flip-Flop

## General Description

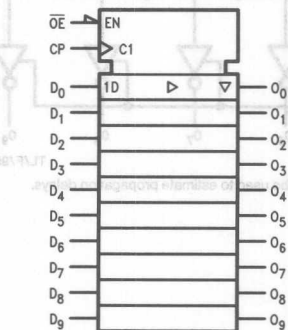
The 'F821 is a 10-bit D-type flip-flop with TRI-STATE® true outputs arranged in a broadside pinout. The 'F821 is functionally and pin compatible with the AMD's Am29821.

**Ordering Code:** See Section 5

## Logic Symbols

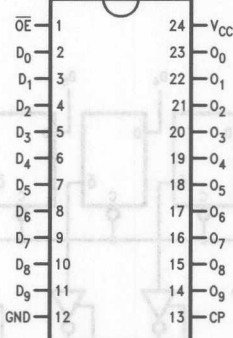


IEEE/IEC



TL/F/9595-5

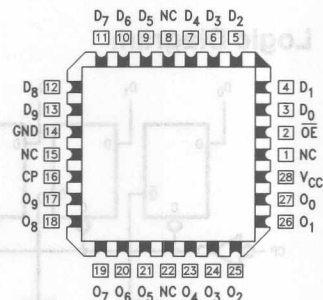
**Pin Assignment  
for DIP, SOIC and Flatpak**



TL/F/9595-2

## Connection Diagrams

**Pin Assignment  
for LCC**



TL/F/9595-3

**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions





Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
D <sub>0</sub> -D <sub>9</sub>	Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
OE	Output Enable	1.0/1.0	20 $\mu$ A/ -0.6 mA
CP	Clock Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
O <sub>0</sub> -O <sub>9</sub>	TRI-STATE Outputs	150/40 (33.3)	-3.0 mA/24 mA (20 mA)




## Functional Description

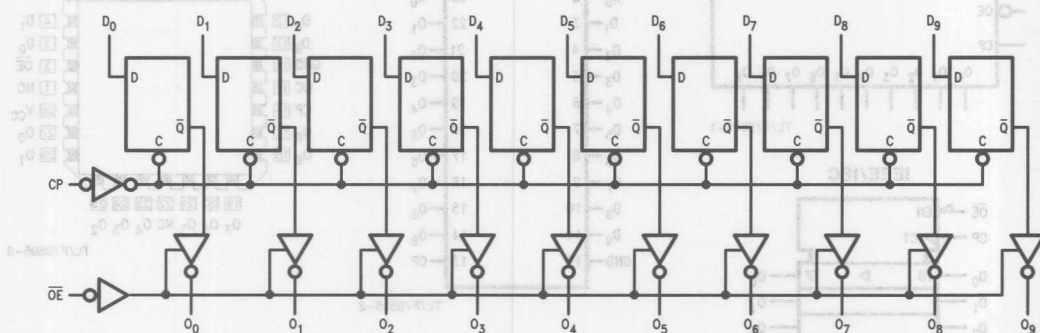
The 'F821 consists of ten D-type edge-triggered flip-flops. This device has TRI-STATE true outputs for bus systems organized in a broadside pinning. The buffered Clock (CP) and buffered Output Enable ( $\overline{OE}$ ) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the  $\overline{OE}$  LOW the content of the flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

### Function Table

Inputs			Internal	Output	Function
$\overline{OE}$	CP	D	$\overline{Q}$	O	
H	H	X	NC	Z	Hold
H	L	X	NC	Z	Hold
H		L	H	Z	Load
H		H	L	Z	Load
L		L	H	L	Data Available
L		H	L	H	Data Available
L	H	X	NC	NC	No Change in Data
L	L	X	NC	NC	No Change in Data

L = LOW Voltage Level  
H = HIGH Voltage Level  
X = Immaterial  
Z = High Impedance  
 = LOW-to-HIGH Transition  
NC = No Change

## Logic Diagram



TL/F/9595-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Pin Names	Description	U.I.	Input (mV)	Output (mV)
$\overline{OE}$	Output Enable	1.0V/0	20 $\mu$ A/-0.8 mA	20 $\mu$ A/-0.8 mA
CP	Clock Input	1.0V/0	20 $\mu$ A/-0.8 mA	20 $\mu$ A/-0.8 mA
D <sub>0</sub> -D <sub>9</sub>	Data Inputs	1.0V/0	20 $\mu$ A/-0.8 mA	20 $\mu$ A/-0.8 mA

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA, All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCZ</sub>	Power Supply Current		78	100	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	100	150		60		70		MHz	2-1
$t_{\text{PLH}}$	Propagation Delay	2.0	6.4	9.5	2.0	10.5	2.0	10.5	ns	2-3
$t_{\text{PHL}}$	CP to $O_n$	2.0	6.2	9.5	2.0	10.5	2.0	10.5		
$t_{\text{PZH}}$	Output Enable Time	2.0	5.8	10.5	2.0	13.0	2.0	11.5	ns	2-5
$t_{\text{PZL}}$	$\overline{OE}$ to $O_n$	2.0	6.3	10.5	2.0	13.0	2.0	11.5		
$t_{\text{PHZ}}$	Output Disable Time	1.5	3.4	7.0	1.0	7.5	1.5	7.5		
$t_{\text{PLZ}}$	$\overline{OE}$ to $O_n$	1.5	3.5	7.0	1.0	7.5	1.5	7.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	2.5		4.0		3.0		ns	2-6
$t_s(\text{L})$	$D_n$ to CP	2.5		4.0		3.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.5		2.5		2.5			
$t_h(\text{L})$	$D_n$ to CP	2.5		2.5		2.5		ns	2-4
$t_w(\text{H})$	CP Pulse Width	5.0		6.0		6.0			
$t_w(\text{L})$	HIGH or LOW	5.0		6.0		6.0			

# 54F/74F823

## 9-Bit D-Type Flip-Flop

### General Description

The 'F823 is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems.

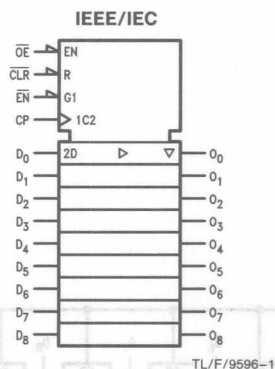
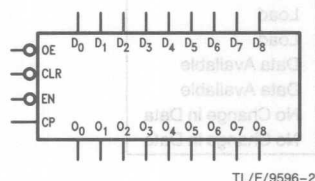
The 'F823 is functionally and pin compatible with AMD's Am29823.

### Features

- TRI-STATE® outputs
- Clock Enable and Clear
- Direct replacement for AMD's Am29823

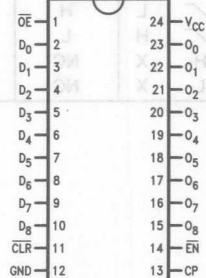
**Ordering Code:** See Section 5

### Logic Symbols



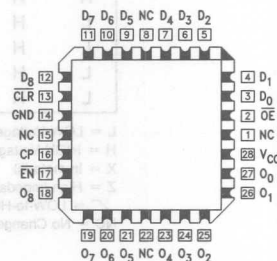
### Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak



TL/F/9596-3

Pin Assignment  
for LCC



TL/F/9596-4

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I <sub>H</sub> /I <sub>L</sub> Output I <sub>O</sub> H/I <sub>O</sub> L
D <sub>0</sub> -D <sub>8</sub>	Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
OE	Output Enable Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
CLR	Clear	1.0/1.0	20 $\mu$ A/ -0.6 mA
CP	Clock Input	1.0/2.0	20 $\mu$ A/ -1.2 mA
EN	Clock Enable	1.0/1.0	20 $\mu$ A/ -0.6 mA
O <sub>0</sub> -O <sub>8</sub>	TRI-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

## Functional Description

The 'F823 device consists of nine D-type edge-triggered flip-flops. It has TRI-STATE true outputs and is organized in broadside pinning. The buffered Clock (CP) and buffered Output Enable ( $\overline{OE}$ ) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the  $\overline{OE}$  LOW the contents of the flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops. In addition to the Clock and Output Enable pins, the 'F823 has Clear ( $\overline{CLR}$ ) and Clock Enable ( $\overline{EN}$ ) pins.

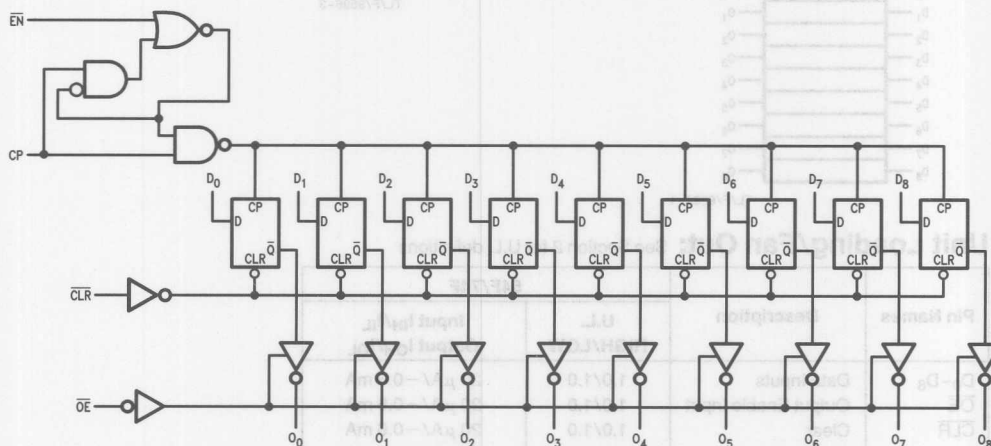
When the  $\overline{CLR}$  is LOW and the  $\overline{OE}$  is LOW, the outputs are LOW. When  $\overline{CLR}$  is HIGH, data can be entered into the flip-flops. When  $\overline{EN}$  is LOW, data on the inputs is transferred to the outputs on the LOW to HIGH clock transition. When the  $\overline{EN}$  is HIGH, the outputs do not change state regardless of the data or clock inputs transitions. This device is ideal for parity bus interfacing in high performance systems.

Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D	$\overline{Q}$	O	
H	H	L	H	X	NC	Z	Hold
H	H	L	L	X	NC	Z	Hold
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	L	X	X	X	H	Z	Clear
L	L	X	X	X	H	L	Clear
H	H	L	—	H	H	Z	Load
H	H	L	—	H	L	Z	Load
L	H	L	—	L	H	L	Data Available
L	H	L	—	H	L	H	Data Available
L	H	L	H	X	NC	NC	No Change in Data
L	H	L	L	X	NC	NC	No Change in Data

L = LOW Voltage Level  
H = HIGH Voltage Level  
X = Immaterial  
Z = High Impedance  
— = LOW-to-HIGH Transition  
NC = No Change

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6 −1.2	mA mA	Max Max	V <sub>IN</sub> = 0.5V (OE, CL <sub>R</sub> , EN) V <sub>IN</sub> = 0.5V (CP)
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Buss Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCZ</sub>	Power Supply Current		75	100	mA	Max	V <sub>O</sub> = HIGH Z



# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$f_{\text{max}}$	Maximum Clock Frequency	100	160		60		70		MHz	2-1
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $O_n$	2.0	5.6	9.5	2.0	10.5	2.0	10.5	ns	2-3
$t_{\text{PHL}}$	Propagation Delay $\overline{\text{CLR}}$ to $O_n$	4.0	7.1	12.0	4.0	13.0	4.0	13.0	ns	2-3
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output Enable Time $\overline{\text{OE}}$ to $O_n$	2.0	5.8	10.5	2.0	13.0	2.0	11.5		
		2.0	5.5	10.5	2.0	13.0	2.0	11.5	ns	2-5
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output Disable Time $\overline{\text{OE}}$ to $O_n$	1.5	2.9	7.0	1.0	7.5	1.5	7.5		
		1.5	2.7	7.0	1.0	7.5	1.5	7.5		

## AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	2.5		4.0		3.0		ns	2-6
$t_s(\text{L})$	$D_n$ to CP	2.5		4.0		3.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.5		2.5		2.5		ns	2-6
$t_h(\text{L})$	$D_n$ to CP	2.5		2.5		2.5			
$t_s(\text{H})$	Setup Time, HIGH or LOW	4.5		5.0		5.0		ns	2-6
$t_s(\text{L})$	$\overline{\text{EN}}$ to CP	2.5		3.0		3.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0		3.0		2.0		ns	2-4
$t_h(\text{L})$	$\overline{\text{EN}}$ to CP	0		1.0		0			
$t_w(\text{H})$	CP Pulse Width	5.0		6.0		6.0		ns	2-4
$t_w(\text{L})$	HIGH or LOW	5.0		6.0		6.0			
$t_w(\text{L})$	$\overline{\text{CLR}}$ Pulse Width, LOW	5.0		5.0		5.0		ns	2-4
$t_{\text{rec}}$	$\overline{\text{CLR}}$ Recovery Time	5.0		5.0		5.0		ns	2-6



## 54F/74F825 8-Bit D-Type Flip-Flop

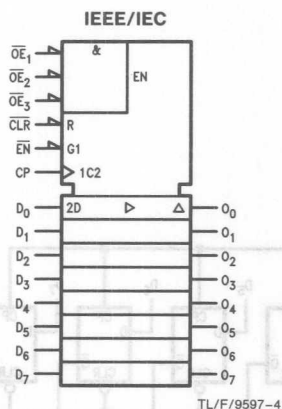
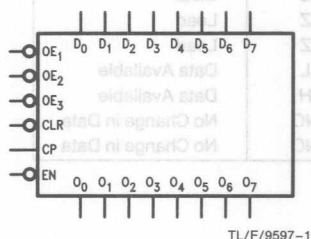
### General Description

The 'F825 is an 8-bit buffered register. It has Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included in the 'F825 are multiple enables that allow multi-user control of the interface.

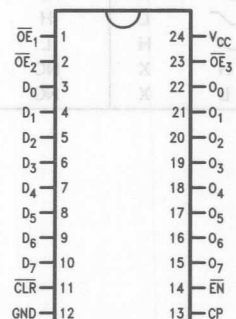
The 'F825 is functionally and pin compatible with AMD's Am29825.

**Ordering Code:** See Section 5

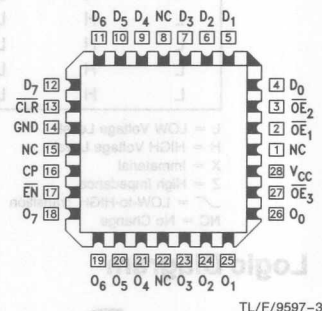
### Logic Symbols



Pin Assignment  
for DIP, SOIC and Flatpak



Pin Assignment  
for LCC



### Features

- TRI-STATE® output
- Clock enable and clear
- Multiple output enables
- Direct replacement for AMD's Am24825

### Connection Diagrams

**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I <sub>IH</sub> /I <sub>IL</sub> Output I <sub>OH</sub> /I <sub>OL</sub>
D <sub>0</sub> -D <sub>7</sub>	Data Inputs	1.0/1.0	20 μA/-0.6 mA
O <sub>0</sub> -O <sub>7</sub>	TRI-STATE Data Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)
OE <sub>1</sub> , OE <sub>2</sub> , OE <sub>3</sub>	Output Enable Input	1.0/1.0	20 μA/-0.6 mA
EN	Clock Enable	1.0/1.0	20 μA/-0.6 mA
CLR	Clear	1.0/1.0	20 μA/-0.6 mA
CP	Clock Input	1.0/2.0	20 μA/-1.2 mA

## Functional Description

The 'F825 consists of eight D-type edge-triggered flip-flops. This device has TRI-STATE true outputs and is organized in broadside pinning. In addition to the clock and output enable pins, the buffered clock (CP) and buffered Output Enable ( $\overline{OE}$ ) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the  $\overline{OE}$  LOW the contents of the flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$

input does not affect the state of the flip-flops. The 'F825 has Clear ( $\overline{CLR}$ ) and Clock Enable ( $\overline{EN}$ ) pins.

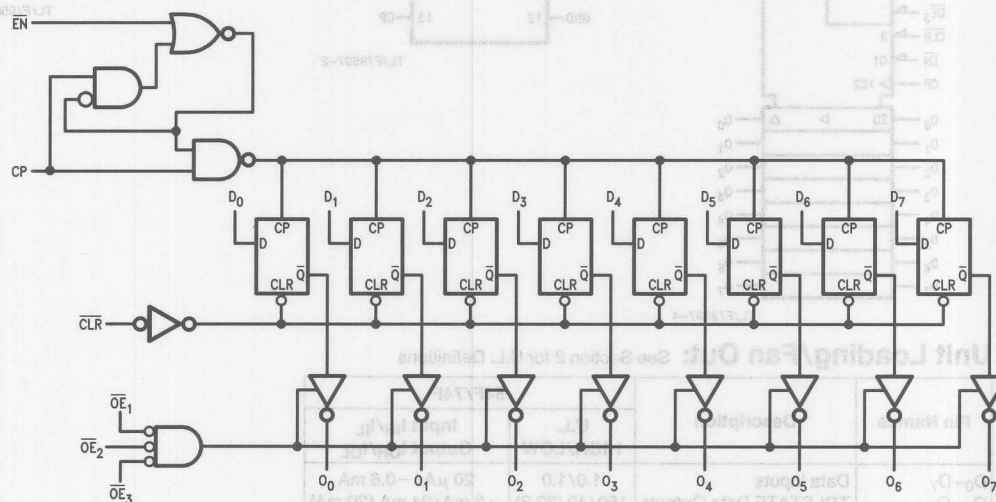
When the  $\overline{CLR}$  is LOW and the  $\overline{OE}$  is LOW the outputs are LOW. When  $\overline{CLR}$  is HIGH, data can be entered into the flip-flops. When  $\overline{EN}$  is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the  $\overline{EN}$  is HIGH the outputs do not change state, regardless of the data or clock input transitions.

Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D	$\overline{Q}$	O	
H	H	L	H	X	NC	Z	Hold
H	H	L	L	X	NC	Z	Hold
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	L	X	X	X	H	Z	Clear
L	L	X	X	X	H	L	Clear
H	H	L	↗	L	H	Z	Load
H	H	L	↗	H	L	Z	Load
L	H	L	↗	L	H	L	Data Available
L	H	L	↗	H	L	H	Data Available
L	H	L	H	X	NC	NC	No Change in Data
L	H	L	L	X	NC	NC	No Change in Data

L = LOW Voltage Level  
H = HIGH Voltage Level  
X = Immaterial  
Z = High Impedance  
↗ = LOW-to-HIGH Transition  
NC = No Change

## Logic Diagram



TL/F/9597-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C

V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
---	----------------

Input Voltage (Note 2)	−0.5V to +7.0V
------------------------	----------------

Input Current (Note 2)	−30 mA to +5.0 mA
------------------------	-------------------

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
---	--------------------------

Standard Output TRI-STATE Output	−0.5V to +5.5V
----------------------------------	----------------

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
--	--------------------------------------

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5			Min	I <sub>OH</sub> = −1 mA
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5		Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0		Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100		Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250		Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Buss Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCZ</sub>	Power Supply Current		75	90	mA	Max	V <sub>O</sub> = HIGH Z

Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	100	160		60		70		MHz	2-1
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to O <sub>n</sub>	2.0	6.5	9.5	2.0	10.5	2.0	10.5	ns	2-3
t <sub>PHL</sub>	Propagation Delay CLR to O <sub>n</sub>	4.0	7.4	12.0	4.0	13.0	4.0	13.0	ns	2-3
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OE to O <sub>n</sub>	2.0	6.5	10.5	2.0	13.0	2.0	11.5	ns	2-5
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OE to O <sub>n</sub>	1.5	3.5	7.0	1.0	7.5	1.5	7.5		

### AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> , V <sub>CC</sub> = Mil		T <sub>A</sub> , V <sub>CC</sub> = Com			
		Min	Max	Min	Max	Min	Max		
t <sub>s</sub> (H)	Setup Time, HIGH or LOW	2.5		4.0		3.0		ns	2-6
t <sub>s</sub> (L)	D <sub>n</sub> to CP	2.5		4.0		3.0			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	2.5		2.5		2.5		ns	2-6
t <sub>h</sub> (L)	D <sub>n</sub> to CP	2.5		2.5		2.5			
t <sub>s</sub> (H)	Setup Time, HIGH or LOW	4.5		5.0		5.0		ns	2-6
t <sub>s</sub> (L)	$\overline{\text{EN}}$ to CP	2.5		3.0		3.0			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	2.0		3.0		1.0		ns	2-4
t <sub>h</sub> (L)	$\overline{\text{EN}}$ to CP	0		2.0		0			
t <sub>w</sub> (H)	CP Pulse Width	5.0		6.0		6.0		ns	2-4
t <sub>w</sub> (L)	HIGH or LOW	5.0		6.0		6.0			
t <sub>w</sub> (L)	$\overline{\text{CLR}}$ Pulse Width, LOW	5.0		5.0		5.0		ns	2-4
t <sub>rec</sub>	$\overline{\text{CLR}}$ Recovery Time	5.0		5.0		5.0		ns	2-6

## 54F/74F827 • 54F/74F828 10-Bit Buffers/Line Drivers

### General Description

The 'F827 and 'F828 10-bit bus buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR output enables for maximum control flexibility.

The 'F827 and 'F828 are functionally- and pin-compatible to AMD's Am29827 and Am29828. The 'F828 is an inverting version of the 'F827.

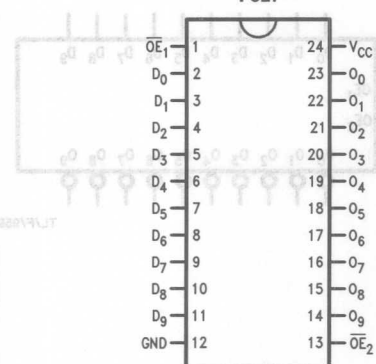
### Features

- TRI-STATE® output
- 'F828 is inverting
- Direct replacement for AMD's Am29827 and Am29828

**Ordering Code:** See Section 5

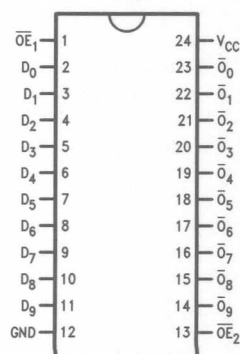
### Connection Diagrams

Pin Assignment for  
DIP, Flatpak and SOIC  
'F827



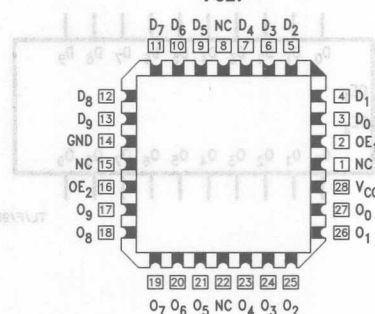
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'F828



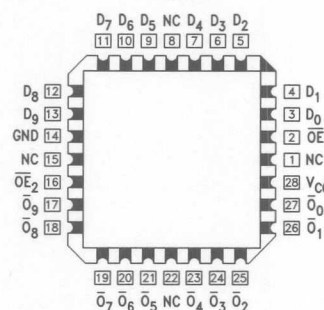
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Pin Assignment  
for LCC  
'F827



TL/F/9598-2

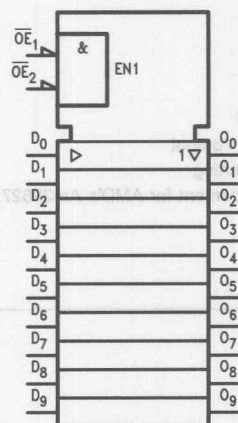
'F828



TL/F/9598-9

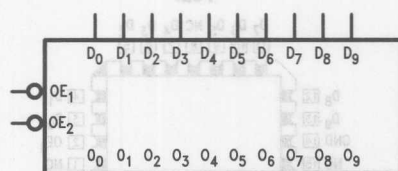


## Logic Symbols

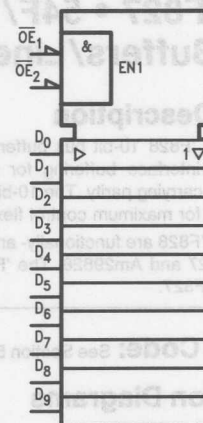
IEEE/IEC  
'F827

TL/F/9598-6

'F827

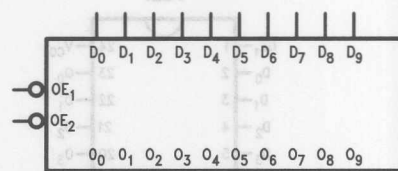


TL/F/9598-3

IEEE/IEC  
'F828

TL/F/9598-7

'F828



TL/F/9598-10

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{OE}_1, \overline{OE}_2$	Output Enable Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
$D_0$ - $D_7$	Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$O_0$ - $O_7$	Data Outputs, TRI-STATE	600/106.6 (80)	-12 mA/64 mA (48 mA)

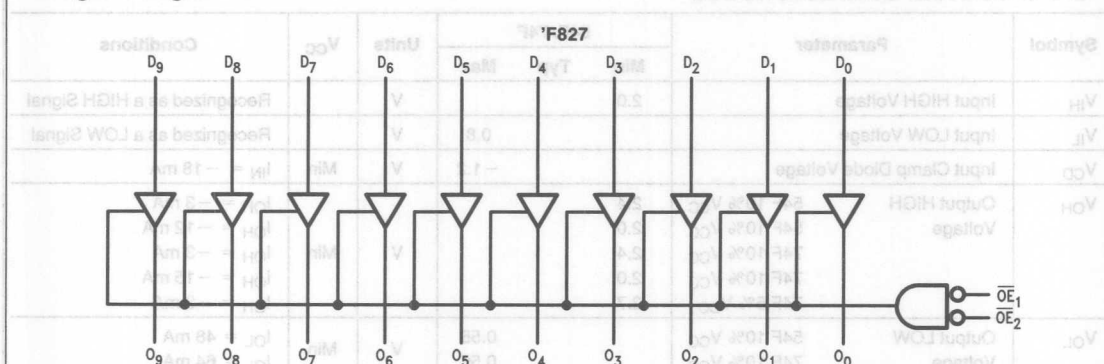
**Functional Description**

The 'F827 and 'F828 are line drivers designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC board density. The devices have TRI-STATE outputs controlled by the Output Enable ( $\overline{OE}$ ) pins. The outputs can sink 64 mA (48 mA mil) and source 15 mA. Input clamp diodes limit high-speed termination effects.

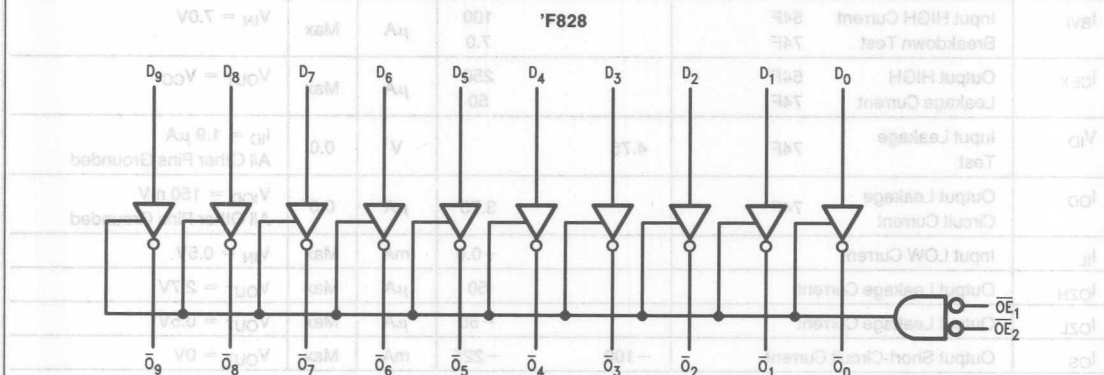
**Function Table**

Inputs		Outputs		Function
$\overline{OE}$	$D_n$	$O_n$		
		'F827	'F828	
L	H	H	L	Transparent
L	L	L	H	Transparent
H	X	Z	Z	High Z

H = HIGH Voltage level  
L = LOW Voltage Level  
Z = High Impedance  
X = Immaterial

**Logic Diagrams**

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	-0.5V to V <sub>CC</sub>
Standard Output TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	-55°C to +125°C
Military	0°C to +70°C
Commercial	
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.4		V	Min	I <sub>OH</sub> = -3 mA
		54F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = -12 mA
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = -3 mA
		74F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = -15 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.55	V	Min	I <sub>OL</sub> = 48 mA
		74F 10% V <sub>CC</sub>		0.55			I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			-50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-100	-225	mA	Max	V <sub>OUT</sub> = 0V

**DC Electrical Characteristics** (Continued)

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current ('F827)		30	45	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current ('F827)		60	90	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current ('F827)		40	60	mA	Max	V <sub>O</sub> = HIGH Z
I <sub>CCH</sub>	Power Supply Current ('F828)		14	20	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current ('F828)		56	85	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current ('F828)		35	50	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	1.0	3.0	5.5	1.0	7.5	1.0	6.5	ns	2-3
t <sub>PHL</sub>	Data to Output ('F827)	1.5	3.3	5.5	1.5	7.0	1.5	6.0		
t <sub>PLH</sub>	Propagation Delay	1.0	3.0	5.0	1.0	6.5	1.0	5.5	ns	2-3
t <sub>PHL</sub>	Data to Output ('F828)	1.0	2.0	4.0	1.0	5.0	1.0	4.0		
t <sub>PZH</sub>	Output Enable Time	3.0	5.7	9.0	2.5	10.0	2.5	9.5	ns	2-5
t <sub>PZL</sub>	OE to O <sub>n</sub>	3.5	6.8	11.5	3.0	12.5	3.0	12.0		
t <sub>PHZ</sub>	Output Disable Time	1.5	3.3	8.0	1.5	9.0	1.5	8.5	ns	2-5
t <sub>PLZ</sub>	OE to O <sub>n</sub>	1.0	3.5	8.0	1.0	9.0	1.0	8.5		

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input/Output HIGH/LOW
D <sub>0</sub> -D <sub>3</sub>	Data Inputs	1.0V/0.1	50 μA/-0.8 mA
O <sub>0</sub> -O <sub>3</sub>	TRI-STATE Outputs	180V/40 (33.3)	-2 mA/2.5 mA (20 mA)
OE	Output Enable Input	1.0V/0.1	50 μA/-0.8 mA
LE	Latch Enable	1.0V/0.1	50 μA/-0.8 mA



## 54F/74F841 10-Bit Transparent Latch

### General Description

The 'F841 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 'F841 is a 10-bit transparent latch, a 10-bit version of the 'F373.

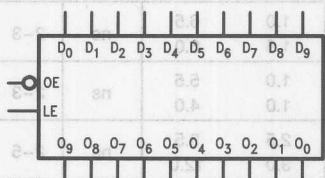
The 'F841 is functionally and pin-compatible to AMD's Am29841.

### Features

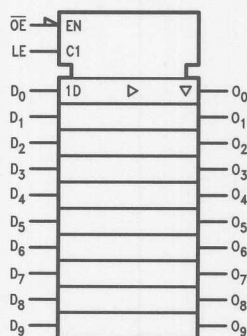
- TRI-STATE® output
- Direct replacement for AMD's Am29841

**Ordering Code:** See Section 5

### Logic Symbols



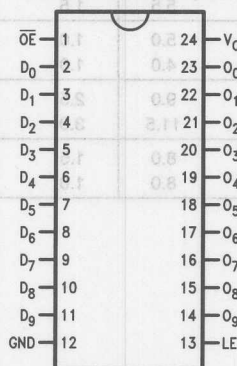
IEEE/IEC



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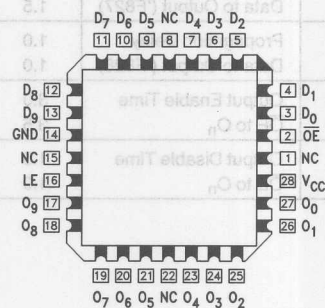
### Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak



TL/F/9599-2

Pin Assignment  
for LCC



TL/F/9599-3

**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
D <sub>0</sub> -D <sub>9</sub>	Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
O <sub>0</sub> -O <sub>9</sub>	TRI-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)
OE	Output Enable Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
LE	Latch Enable	1.0/1.0	20 $\mu$ A/ -0.6 mA

## Functional Description

The 'F841 device consists of ten D-type latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition.

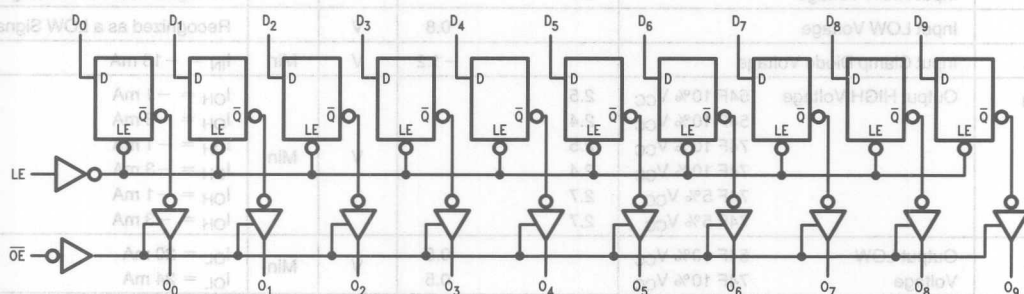
On the LE HIGH-to-LOW transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH the bus output is in the high impedance state.

Function Table

Inputs			Internal	Output	Function
$\overline{OE}$	LE	D	Q	O	
X	X	X	X	Z	High Z
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched
L	X	X	H	H	Preset
L	X	X	L	L	Clear
L	X	X	H	H	Preset
H	L	X	L	Z	Latched
H	L	X	H	Z	Latched

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = HIGH Impedance  
NC = No Change

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCZ</sub>	Power Supply Current		69	92	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to $O_n$	2.5 1.5		8.0 6.5			2.0 1.5	9.0 7.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay LE to $O_n$	5.0 2.0		12.0 7.5			4.5 2.0	13.5 8.0	ns	2-3
$t_{pZH}$ $t_{pZL}$	Output Enable Time $\overline{OE}$ to $O_n$	2.5 2.5		8.5 9.0			2.0 2.0	9.5 10.0	ns	2-5
$t_{pHZ}$ $t_{pLZ}$	Output Disable Time $\overline{OE}$ to $O_n$	1.0 1.0		6.5 6.5			1.0 1.0	7.5 7.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $D_n$ to LE	2.0 2.0				2.5 2.5		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $D_n$ to LE	2.5 3.0				3.0 3.5			
$t_w(\text{H})$	LE Pulse Width, HIGH	4.0				4.0		ns	2-4



## 54F/74F843

### 9-Bit Transparent Latch

#### General Description

The 'F843 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity.

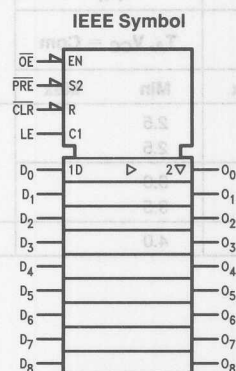
The 'F843 is functionally and pin compatible with AMD's Am29843.

#### Features

- TRI-STATE® output
- Direct replacement for AMD's Am29843

**Ordering Code:** See Section 5

#### Logic Symbols

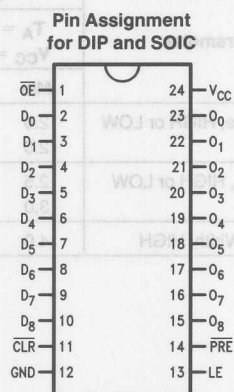


TL/F/9453-6



TL/F/9453-1

#### Connection Diagram



TL/F/9453-2

**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
D <sub>0</sub> -D <sub>8</sub>	Data Inputs	1.0/1.0	20 $\mu$ A / -0.6 mA
OE	Output Enable Input	1.0/1.0	20 $\mu$ A / -0.6 mA
LE	Latch Enable	1.0/1.0	20 $\mu$ A / -0.6 mA
CLR	Clear	1.0/1.0	20 $\mu$ A / -0.6 mA
PRE	Preset	1.0/1.0	20 $\mu$ A / -0.6 mA
O <sub>0</sub> -O <sub>8</sub>	TRI-STATE Data Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

## Functional Description

The 'F843 consists of nine D-type latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH, the bus

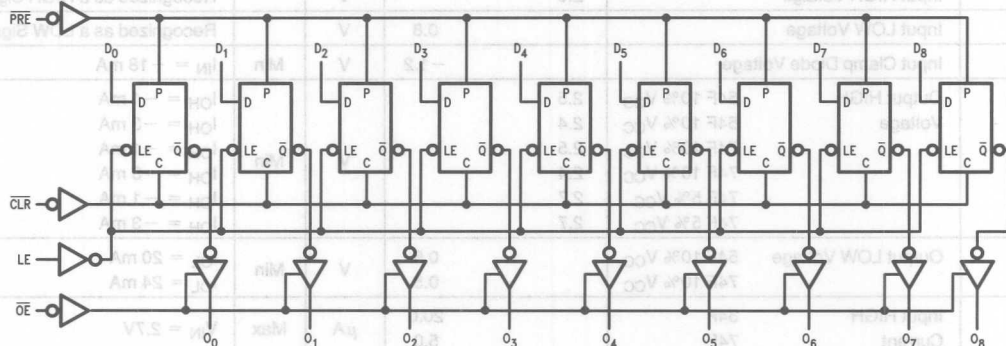
output is in the high impedance state. In addition to the LE and  $\overline{OE}$  pins, the 'F843 has a Clear (CLR) pin and a Preset (PRE). These pins are ideal for parity bus interfacing in high performance systems. When CLR is LOW, the outputs are LOW if  $\overline{OE}$  is LOW. When CLR is HIGH, data can be entered into the latch. When PRE is LOW, the Outputs are HIGH if  $\overline{OE}$  is LOW. Preset overrides CLR.

Function Table

Inputs				Internal	Output	Function
CLR	PRE	$\overline{OE}$	LE	D	Q	
H	H	X	X	X	Z	High Z
H	H	H	H	L	Z	High Z
H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Latched
H	H	L	H	L	L	Transparent
H	H	L	H	H	H	Transparent
H	H	L	L	X	NC	Latched
H	L	L	X	X	H	Preset
L	H	L	X	X	L	Clear
L	L	L	X	X	H	Preset
L	H	H	L	X	L	Latched
H	L	H	L	X	H	Latched

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance  
NC = No Change

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5			V	Min	I <sub>OH</sub> = −1 mA
		54F 10% V <sub>CC</sub>	2.4					I <sub>OH</sub> = −3 mA
		74F 10% V <sub>CC</sub>	2.5					I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.4					I <sub>OH</sub> = −3 mA
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>			0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>			0.5			I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F			20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F			5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F			100	μA	Max	V <sub>IN</sub> = 7.0V
		74F			7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F			50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All other pins grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All other pins grounded
I <sub>IL</sub>	Input LOW Current				−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current				50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current				−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60		−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test				500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CC</sub>	Power Supply Current			65	90	mA	Max	

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to $O_n$	2.5 1.5	5.4 4.2	8.0 6.5			2.0 1.5	9.0 7.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay LE to $O_n$	5.0 2.0	8.5 4.7	12.0 7.5			4.5 2.0	13.5 8.0	ns	2-3
$t_{PLH}$	Propagation Delay PRE to $O_n$	3.0	7.3	10.0			2.5	11.0	ns	2-3
$t_{PHL}$	Propagation Delay CLR to $O_n$	3.0	6.9	10.0			2.5	11.0	ns	2-3
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{OE}$ to $O_n$	2.5 2.5	5.0 6.1	8.5 9.0			2.0 2.0	9.5 10.0	ns	2-3
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{OE}$ to $O_n$	1.0 1.0	3.6 3.4	6.5 6.5			1.0 1.0	7.5 7.5	ns	2-5

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s$ (H) $t_s$ (L)	Setup Time, HIGH or LOW $D_n$ to LE	2.0 2.0				2.5 2.5		ns	2-6
$t_h$ (H) $t_h$ (L)	Hold Time, HIGH or LOW $D_n$ to LE	2.5 3.0				3.0 3.5			
$t_w$ (H)	LE Pulse Width, HIGH	4.0				4.0		ns	2-4
$t_w$ (L)	$\overline{\text{PRE}}$ Pulse Width, LOW	5.0				5.0		ns	2-4
$t_w$ (L)	$\overline{\text{CLR}}$ Pulse Width, LOW	5.0				5.0		ns	2-4
$t_{\text{rec}}$	$\overline{\text{PRE}}$ Recovery Time	10.0				10.0		ns	2-6
$t_{\text{rec}}$	$\overline{\text{CLR}}$ Recovery Time	12.0				13.0		ns	2-6

Pin Names	Description	U.L.	Input/Output
PRE	Preset	1.0V/0	20 $\mu\text{A}$ - 0.8 mA
CLR	Clear	1.0V/0	20 $\mu\text{A}$ - 0.8 mA
LE	Latch Enable	1.0V/0	20 $\mu\text{A}$ - 0.8 mA
$\overline{OE}$ - $\overline{OE}_2$	Output Enable	1.0V/0	20 $\mu\text{A}$ - 0.8 mA
$O_0$ - $O_7$	Data Output	1.0V/0	20 $\mu\text{A}$ - 0.8 mA
$D_0$ - $D_7$	Data Input	1.0V/0	20 $\mu\text{A}$ - 0.8 mA



# 54F/74F845

## 8-Bit Transparent Latch

### General Description

The 'F845 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity.

The 'F845 is functionally- and pin-compatible with AMD's Am29845.

### Features

- TRI-STATE® outputs
- Direct replacement for AMD's Am29845

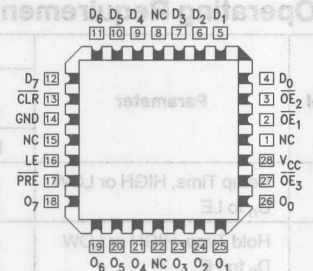
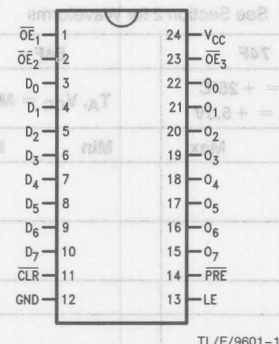
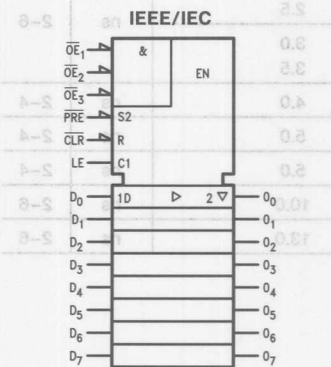
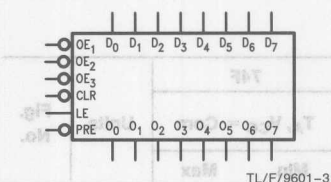
**Ordering Code:** See Section 5

### Logic Symbols

### Connection Diagrams

Pin Assignment  
for DIP, SOIC and Flatpak

Pin Assignment  
for LCC



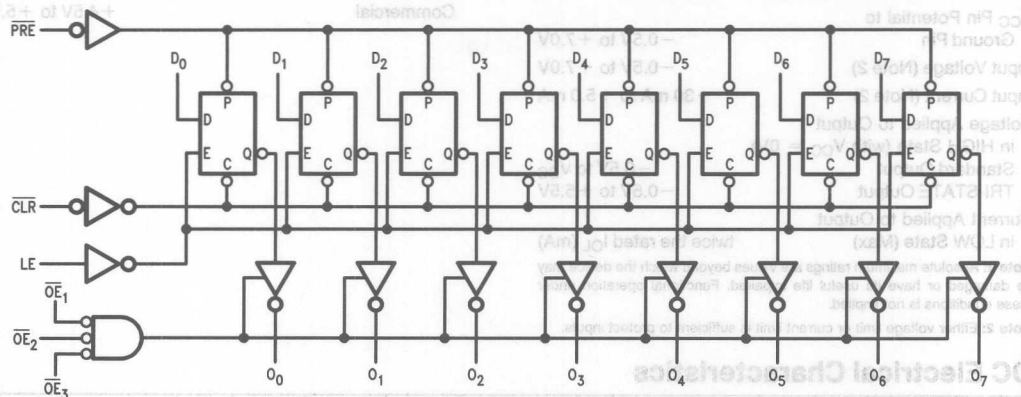
**Unit Loading/Fan Out:** See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$D_0-D_7$	Data Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
$O_0-O_7$	Data Outputs	150/40 (33.3)	-3.0 $\mu A$ / 24 mA (20 mA)
$OE_1-OE_3$	Output Enables	1.0/1.0	20 $\mu A$ / -0.6 mA
LE	Latch Enable	1.0/1.0	20 $\mu A$ / -0.6 mA
CLR	Clear	1.0/1.0	20 $\mu A$ / -0.6 mA
PRE	Preset	1.0/1.0	20 $\mu A$ / -0.6 mA

## Functional Description

The 'F845 consists of eight D-type latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation as the output transition follows the data in transition.

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

Inputs					Internal	Output	Function
CLR	PRE	OE	LE	D	Q	O	
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched
H	L	H	L	X	H	Z	Latched

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance  
NC = No Change

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCZ</sub>	Power Supply Current		63	85	mA	Max	V <sub>O</sub> = HIGH Z

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay D <sub>n</sub> to O <sub>n</sub>	2.5	4.8	8.0			2.0	9.0	ns	2-3
t <sub>PHL</sub>	Propagation Delay LE to O <sub>n</sub>	1.5	3.6	6.5			1.5	7.0	ns	2-3
t <sub>PLH</sub>	Propagation Delay PRE to O <sub>n</sub>	5.0	8.1	12.0			4.5	13.5	ns	2-3
t <sub>PHL</sub>	Propagation Delay CLR to O <sub>n</sub>	2.0	4.4	7.5			2.0	8.0	ns	2-3
t <sub>PLH</sub>	Propagation Delay PRE to O <sub>n</sub>	3.0	5.9	10.0			2.5	11.0	ns	2-3
t <sub>PHL</sub>	Propagation Delay CLR to O <sub>n</sub>	3.0	6.5	10.0			2.5	11.0	ns	2-3
t <sub>PZH</sub>	Output Enable Time OE to O <sub>n</sub>	2.5	5.8	9.5			2.0	10.5	ns	2-5
t <sub>PZL</sub>	Output Disable Time OE to O <sub>n</sub>	2.5	7.6	12.0			2.0	13.0	ns	2-5
t <sub>PHZ</sub>	Output Disable Time OE to O <sub>n</sub>	1.0	3.1	7.5			1.0	8.5	ns	2-5
t <sub>PLZ</sub>	Output Disable Time OE to O <sub>n</sub>	1.0	2.8	6.5			1.0	7.5	ns	2-5

Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> , V <sub>CC</sub> = Mil		T <sub>A</sub> , V <sub>CC</sub> = Com		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t <sub>s</sub> (H)	Setup Time, HIGH or LOW	2.0				2.5		ns	2-6
t <sub>s</sub> (L)	D <sub>n</sub> to LE	2.0				2.5			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	2.5				3.0		ns	2-6
t <sub>h</sub> (L)	D <sub>n</sub> to LE	3.0				3.5			
t <sub>w</sub> (H)	LE Pulse Width, HIGH	4.0				4.0		ns	2-4
t <sub>w</sub> (L)	$\overline{\text{PRE}}$ Pulse Width, LOW	5.0				5.0		ns	2-4
t <sub>w</sub> (L)	$\overline{\text{CLR}}$ Pulse Width, LOW	5.0				5.0		ns	2-4
t <sub>rec</sub>	$\overline{\text{PRE}}$ Recovery Time	10.0				10.0		ns	2-6
t <sub>rec</sub>	$\overline{\text{CLR}}$ Recovery Time	12.0				13.0		ns	2-6



## 54F/74F899 9-Bit Latchable Transceiver with Parity Generator/Checker

### General Description

The 'F899 is a 9-bit to 9-bit parity transceiver with transparent latches. The device can operate as a feed-through transceiver or it can generate/check parity from the 8-bit data busses in either direction. It has a guaranteed current sinking capability of 24 mA at the A-bus and 64 mA at the B-bus.

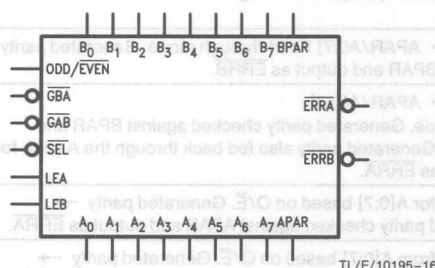
The 'F899 features independent latch enables for the A-to-B direction and the B-to-A direction, a select pin for ODD/EVEN parity, and separate error signal output pins for checking parity.

### Features

- Latchable transceiver with output sink of 24 mA at the A-bus and 64 mA at the B-bus
- Option to select generate parity and check or "feed-through" data/parity in directions A-to-B or B-to-A
- Independent latch enables for A-to-B and B-to-A directions
- Select pin for ODD/EVEN parity
- ERRRA and ERRRB output pins for parity checking
- Ability to simultaneously generate and check parity
- May be used in systems applications in place of the 'F543 and 'F280
- May be used in system applications in place of the 'F657 and 'F373 (no need to change T/R to check parity)
- Guaranteed 4000V min ESD protection

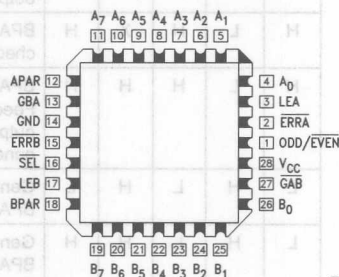
**Ordering Code:** See Section 5

### Logic Symbol



### Connection Diagram

Pin Assignment for PCC



**Input Loading/Fan-Out:** See Section 2

Pin Names	Description	54F/74F HIGH/LOW	
		U.L. HIGH/LOW	Input I <sub>IH</sub> /I <sub>IL</sub> Output I <sub>OH</sub> /I <sub>OL</sub>
A <sub>0</sub> -A <sub>7</sub>	Data Inputs/ Data Outputs	1.0/1.0	20 μA/-0.6 mA -3 mA/24 mA
B <sub>0</sub> -B <sub>7</sub>	Data Inputs/ Data Outputs	1.0/1.0	20 μA/-0.6 mA -12 mA/64 mA
APAR	A Bus Parity Input/Output	1.0/1.0	20 μA/-0.6 mA -3 mA/24 mA
BPAR	B Bus Parity Input/Output	1.0/1.0	20 μA/-0.6 mA -12 mA/64 mA
ODD/EVEN	Parity Select Input	1.0/1.0	20 μA/-0.6 mA
GBA, GAB	Output Enable Inputs	1.0/1.0	20 μA/-0.6 mA
SEL	Mode Select Input	1.0/1.0	20 μA/-0.6 mA
LEA, LEB	Latch Enable Inputs	1.0/1.0	20 μA/-0.6 mA
ERRA, ERRB	Error Signal Outputs	50/33.3	-1 mA/20 mA



Pin Names	Description
A <sub>0</sub> –A <sub>7</sub>	A Bus Data Inputs/Data Outputs
B <sub>0</sub> –B <sub>7</sub>	B Bus Data Inputs/Data Outputs
APAR, BPAR	A and B Bus Parity Inputs
ODD/EVEN	ODD/EVEN Parity Select, Active LOW for EVEN Parity
G <sub>BA</sub> , G <sub>AB</sub>	Output Enables for A or B Bus, Active LOW
SEL	Select Pin for Feed-Through or Generate Mode, LOW for Generate Mode
LEA, LEB	Latch Enables for A and B Latches, HIGH for Transparent Mode
ERRA, ERRB	Error Signals for Checking Generated Parity with Parity In, LOW if Error Occurs

## Functional Description

The 'F899 has three principal modes of operation which are outlined below. These modes apply to both the A-to-B and B-to-A directions.

- Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEB (LEA) is HIGH and the Mode Select (SEL) is LOW, the parity generated from B[0:7] (A[0:7]) can be checked and monitored by ERRB (ERRA).
- Bus A (B) communicates to Bus B (A) in a feed-through mode if SEL is HIGH. Parity is still generated and checked as ERRA and ERRB in the feed-through mode (can be used as an interrupt to signal a data/parity bit error to the CPU).
- Independent Latch Enables (LEA and LEB) allow other permutations of generating/checking (see Function Table below).

Function Table

Inputs					Operation
GAB	GBA	SEL	LEA	LEB	
H	H	X	X	X	Busses A and B are TRI-STATE®.
H	L	L	L	H	Generates parity from B[0:7] based on O/E (Note 1). Generated parity → APAR. Generated parity checked against BPAR and output as ERRB.
H	L	L	H	H	Generates parity from B[0:7] based on O/E. Generated parity → APAR. Generated parity checked against BPAR and output as ERRB. Generated parity also fed back through the A latch for generate/check as ERRA.
H	L	L	X	L	Generates parity from B latch data based on O/E. Generated parity → APAR. Generated parity checked against latched BPAR and output as ERRB.
H	L	H	X	H	BPAR/B[0:7] → APAR/A[0:7] Feed-through mode. Generated parity checked against BPAR and output as ERRB.
H	L	H	H	H	BPAR/B[0:7] → APAR/A[0:7] Feed-through mode. Generated parity checked against BPAR and output as ERRB. Generated parity also fed back through the A latch for generate/check as ERRA.
L	H	L	H	L	Generates parity for A[0:7] based on O/E. Generated parity → BPAR. Generated parity checked against APAR and output as ERRA.
L	H	L	H	H	Generates parity from A[0:7] based on O/E. Generated parity → BPAR. Generated parity checked against APAR and output as ERRA. Generated parity also fed back through the B latch for generate/check as ERRB.
L	H	L	L	X	Generates parity from A latch data based on O/E. Generated parity → BPAR. Generated parity checked against latched APAR and output as ERRA.
L	H	H	H	L	APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as ERRA.
L	H	H	H	H	APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as ERRA. Generated parity also fed back through the B latch for generate/check as ERRB.

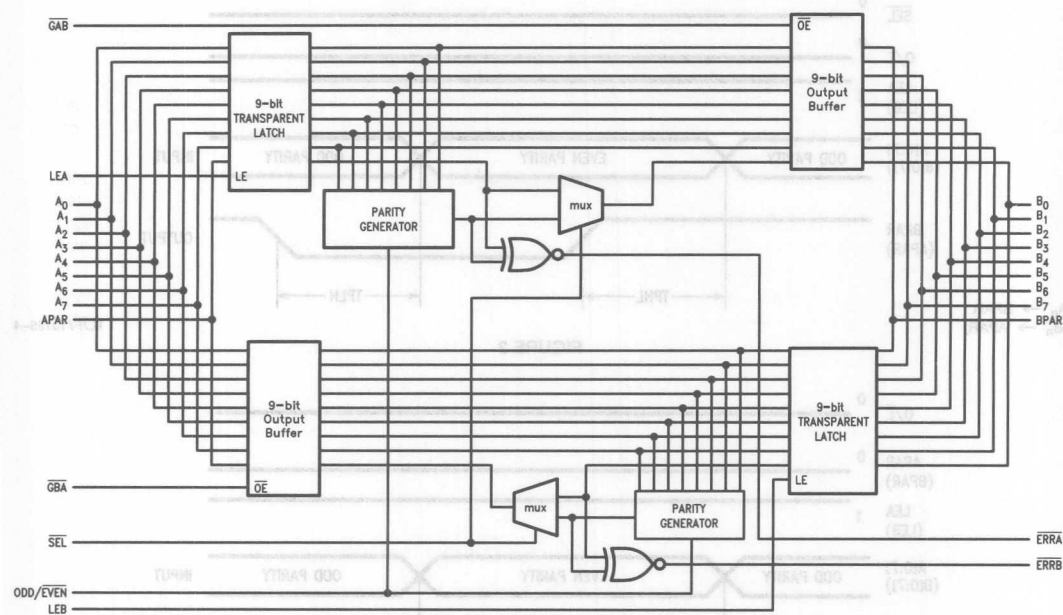
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

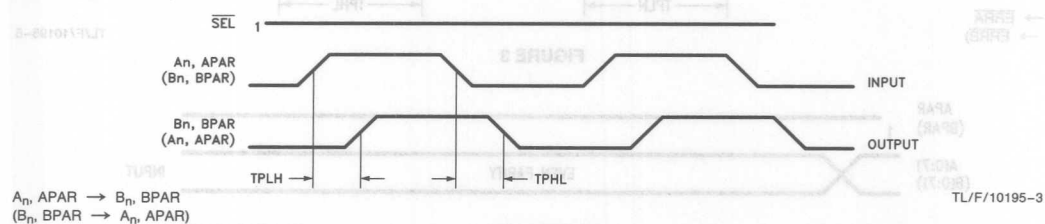
Note 1: O/E = ODD/EVEN

## Functional Block Diagram



TL/F/10195-2

## AC Path



TL/F/10195-3

FIGURE 1

## AC Path (Continued)

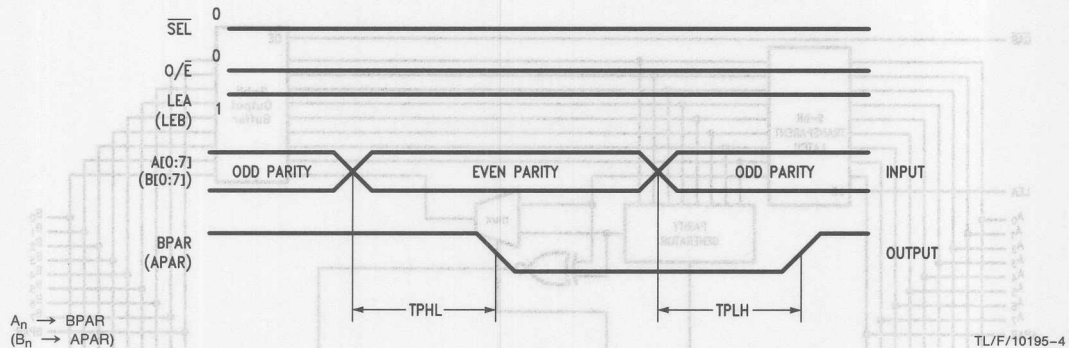


FIGURE 2

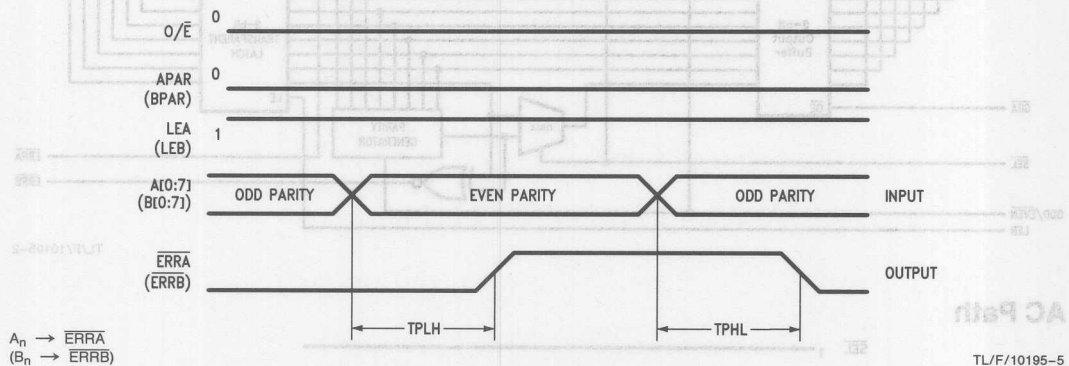


FIGURE 3

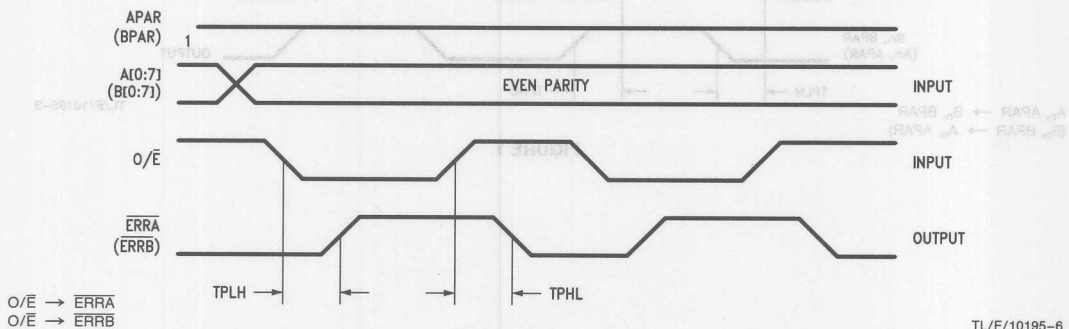


FIGURE 4

## AC Path (Continued)

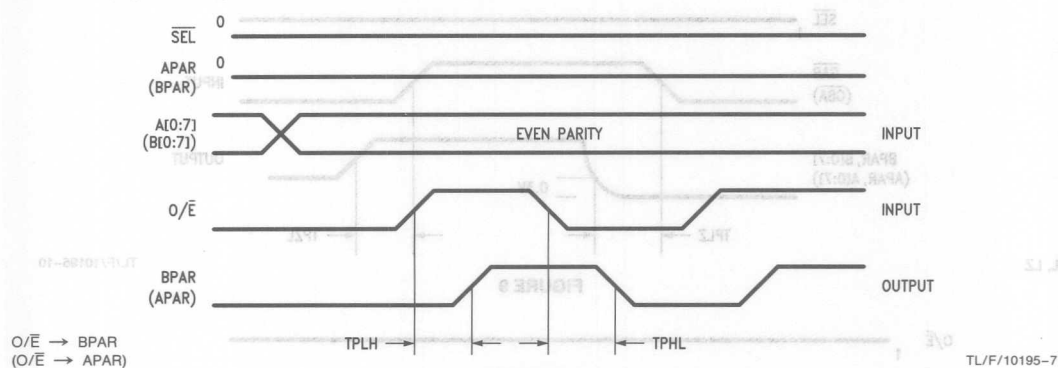


FIGURE 5

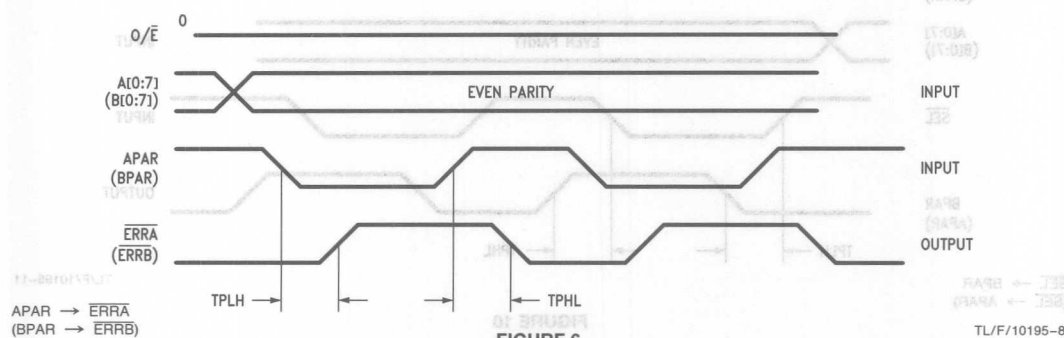


FIGURE 6

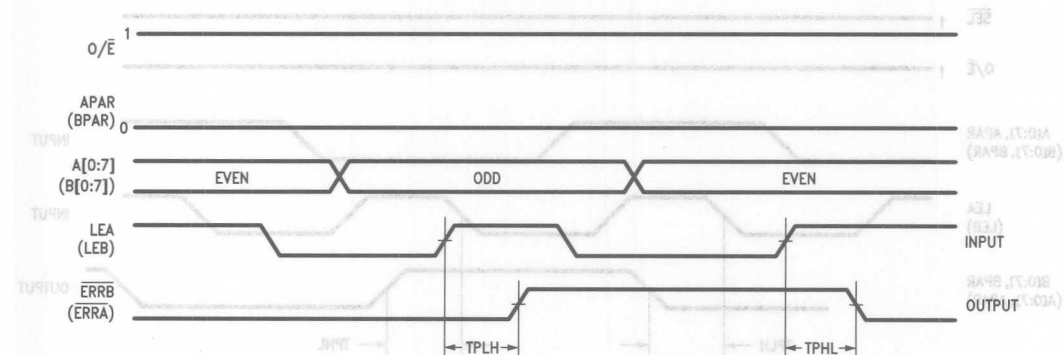


FIGURE 7

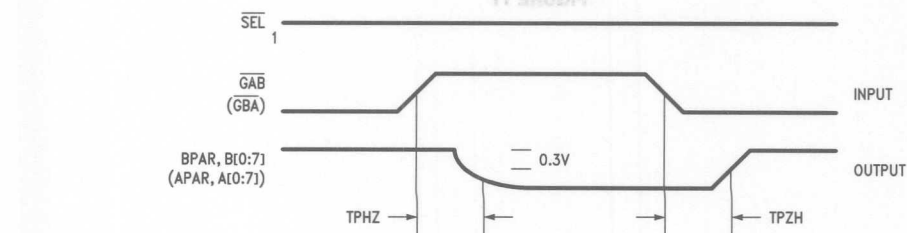


FIGURE 8

## AC Path (Continued)

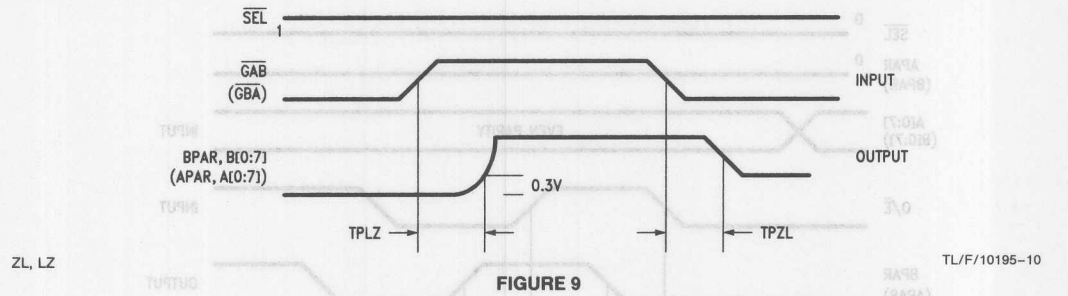


FIGURE 9

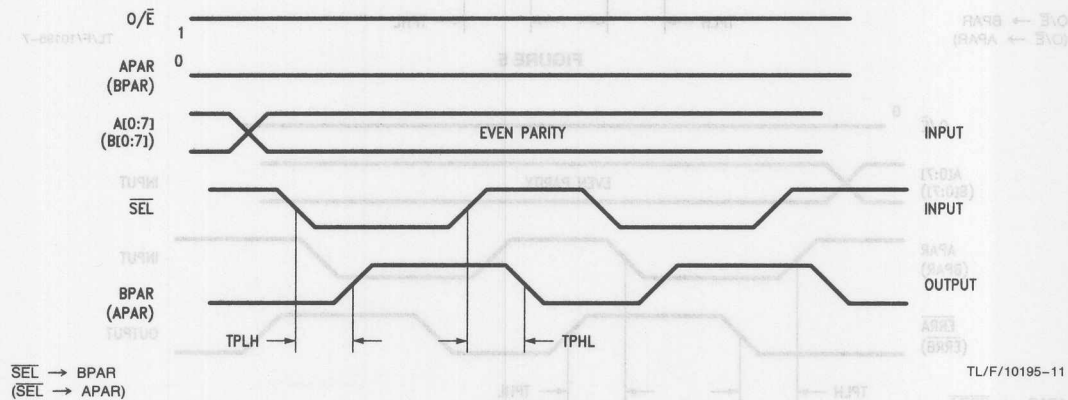


FIGURE 10

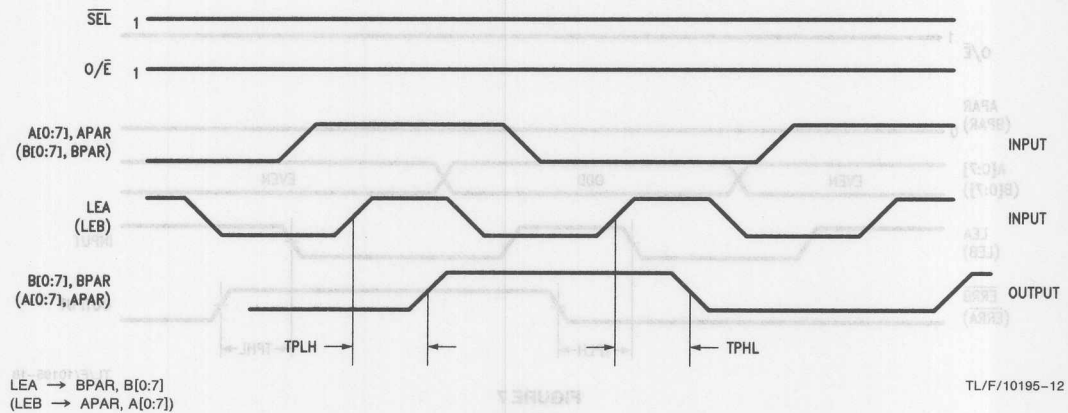


FIGURE 11





## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max)	Twice the Rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

## Recommended Operating Conditions

Free Air Ambient Temperature	−55°C to +125°C
Military	0°C to +70°C
Commercial	
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub>	54F/74F			Units	Conditions
			Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage		2.0			V	Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V	Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage	Min			−1.2	V	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	Min	2.5		V	I <sub>OH</sub> = −1 mA
		54F 10% V <sub>CC</sub>	Min	2.4			I <sub>OH</sub> = −3 mA
		54F 10% V <sub>CC</sub>	Min	2.0			I <sub>OH</sub> = −12 mA (B <sub>n</sub> , B <sub>PAR</sub> )
		74F 10% V <sub>CC</sub>		2.5			I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>		2.4			I <sub>OH</sub> = −3 mA
		74F 10% V <sub>CC</sub>		2.0			I <sub>OH</sub> = −15 mA (B <sub>n</sub> , B <sub>PAR</sub> )
		74F 5% V <sub>CC</sub>		2.7			I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>	Min		0.5	V	I <sub>OL</sub> = 20 mA
		54F 10% V <sub>CC</sub>	Min		0.55		(A <sub>n</sub> , APAR, <u>ERRA</u> , <u>ERRB</u> )
		74F 10% V <sub>CC</sub>			0.5		I <sub>OL</sub> = 48 mA (B <sub>n</sub> , B <sub>PAR</sub> )
		74F 5% V <sub>CC</sub>			0.5		I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>			0.55		(A <sub>n</sub> , APAR, <u>ERRA</u> , <u>ERRB</u> )
V <sub>TH</sub>	Input Threshold Voltage			1.45		V	±0.1V, Sweep Edge Rate must be > 1V/50 ns
V <sub>OLV</sub>	Negative Ground Bounce Voltage			1.0		V	Observed on “quiet” output during simultaneous switching of remaining outputs
V <sub>OLP</sub>	Positive Ground Bounce Voltage			1.0		V	Observed on “quiet” output during simultaneous switching of remaining outputs
I <sub>IL</sub>	Input Low Current	Max			−0.6	mA	V <sub>IN</sub> = 0.5V
I <sub>IH</sub>	Input HIGH Current	54F		20.0		μA	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100		μA	V <sub>IN</sub> = 7.0V (ODD/EVEN, <u>GAB</u> , <u>GAB</u> , <u>SEL</u> , LEA, LEB)
		74F		7.0			
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)	54F		1.0		mA	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> , APAR, B <sub>PAR</sub> )
		74F		0.5			

## DC Electrical Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub>	54F/74F			Units	Conditions
			Min	Typ	Max		
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input Low Current	Max			-0.6	mA	V <sub>IN</sub> = 0.5V
I <sub>IH</sub> <sup>+</sup> I <sub>OZH</sub>	Output Leakage Current Current	Max			70	μA	V <sub>I/O</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> , APAR, BPAR)
I <sub>IL</sub> <sup>+</sup> I <sub>OZL</sub>	Output Leakage Current	Max			-650	μA	V <sub>I/O</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> , APAR, BPAR)
I <sub>OS</sub>	Output Short-Circuit Current	Max	-60		-150	mA	V <sub>OUT</sub> = 0V (A <sub>n</sub> , APAR, ERR <sub>A</sub> , ERR <sub>B</sub> ) V <sub>OUT</sub> = 0V (B <sub>n</sub> , BPAR)
		Max	-100		-225		
I <sub>ZZ</sub>	Bus Drainage Test	0.0V			500	μA	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current	Max		132	155	mA	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current	Max		178	210	mA	V <sub>O</sub> = LOW, GAB = LOW, GBA = HIGH, V <sub>IL</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current	Max		160	190	mA	V <sub>O</sub> = HIGH Z

## AC Electrical Characteristics

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> , APAR to B <sub>n</sub> , BPAR	4.0	7.5	13.0			4.0	14.0	ns	899-1
		4.0	8.5	13.0			4.0	14.0		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> , B <sub>n</sub> to BPAR, APAR	7.5	12.0	17.0			7.5	18.0	ns	899-2
		7.5	12.5	17.0			7.5	18.0		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> , B <sub>n</sub> to <u>ERRA</u> , <u>ERRB</u>	7.5	12.0	17.0			7.5	18.0	ns	899-3
		7.5	12.5	17.0			7.5	18.0		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay ODD/ <u>EVEN</u> to <u>ERRA</u> , <u>ERRB</u>	4.5	7.5	11.0			4.5	12.0	ns	899-4
		4.5	8.0	11.0			4.5	12.0		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay ODD/ <u>EVEN</u> to APAR, BPAR	4.5	7.5	11.5			4.5	12.5	ns	899-5
		4.5	8.5	11.5			4.5	12.5		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay APAR, BPAR to <u>ERRA</u> , <u>ERRB</u>	5.5	9.0	13.0			5.5	14.0	ns	899-6
		5.5	9.5	13.0			5.5	14.0		
t <sub>PLH</sub> t <sub>PHL</sub>	LEA/LEB to <u>ERRA</u> / <u>ERRB</u>	9.5	13.0	17.5			7.5	18.0	ns	899-7
		9.7		17.5			7.5	18.0		

		$C_L = 50 \text{ pF}$			$C_L = 50 \text{ pF}$		$C_L = 50 \text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	3.0	6.0	10.0			3.0	11.0	ns	899-10
$t_{PHL}$	SEL to APAR, BPAR	3.0	7.0	10.0			3.0	11.0		
$t_{PLH}$	Propagation Delay	3.5	7.0	10.0			3.5	11.0	ns	899-11
$t_{PHL}$	LEB to $A_n$ , APAR	3.5	8.0	10.0			3.5	11.0		
$t_{PLH}$	Propagation Delay	3.5	6.5	10.0			3.5	11.0	ns	899-11
$t_{PHL}$	LEA to $B_n$ , BPAR	3.5	7.5	10.0			3.5	11.0		
$t_{PZH}$	Output Enable Time	1.0	4.5	10.0			1.0	11.0	ns	899-8, 9
$t_{PZL}$	$\overline{GBA}$ or $\overline{GAB}$ to $A_n$ , APAR or $B_n$ , BPAR	1.0	6.5	10.0			1.0	11.0		
$t_{PHZ}$	Output Disable Time	1.0	4.0	7.0			1.0	8.0	ns	899-8, 9
$t_{PLZ}$	$\overline{GBA}$ or $\overline{GAB}$ to $A_n$ , APAR or $B_n$ , BPAR	1.0	4.0	7.0			1.0	8.0		
$t_s(H)$	Setup Time, HIGH or LOW	5.0	1.6				5.0		ns	899-12, 13
$t_s(L)$	$A_n$ , $B_n$ to LEA, LEB	5.0	1.8				5.0			
$t_h(H)$	Hold Time, HIGH or LOW	0	-1.7				0		ns	899-12, 13
$t_h(L)$	$A_n$ , $B_n$ to LEA, LEB	0	-1.5				0			
$t_w$	Pulse Width for LEA, LEB	6.0	2.0				6.0		ns	899-14

# AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50 \text{ pF}$			$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50 \text{ pF}$			Units	Fig. No.
		Min	Typ	Max	Min	Max	Max		
$t_{PLH}$	Propagation Delay	4.0	7.5	13.0			4.0	ns	899-1
$t_{PHL}$	$A_n$ APAR to $B_n$ BPAR	4.0	8.5	13.0			4.0		
$t_{PLH}$	Propagation Delay	7.5	12.0	17.0			7.5	ns	899-2
$t_{PHL}$	$A_n$ $B_n$ to BPAR, APAR	7.5	12.5	17.0			7.5		
$t_{PLH}$	Propagation Delay	7.5	12.0	17.0			7.5	ns	899-3
$t_{PHL}$	$A_n$ $B_n$ to $\overline{ERRA}$ , $\overline{ERRB}$	7.5	12.5	17.0			7.5		
$t_{PLH}$	Propagation Delay	4.5	7.5	11.0			4.5	ns	899-4
$t_{PHL}$	ODD/EVEN to $\overline{ERRA}$ , $\overline{ERRB}$	4.5	8.0	11.0			4.5		
$t_{PLH}$	Propagation Delay	4.5	7.5	11.5			4.5	ns	899-5
$t_{PHL}$	ODD/EVEN to APAR, BPAR	4.5	8.5	11.5			4.5		
$t_{PLH}$	Propagation Delay	6.5	8.0	13.0			6.5	ns	899-6
$t_{PHL}$	APAR, BPAR to $\overline{ERRA}$ , $\overline{ERRB}$	6.5	9.5	13.0			6.5		
$t_{PLH}$	LEA/LEB to	9.5	13.0	17.5			9.5	ns	899-7
$t_{PHL}$	$\overline{ERRA}$ , $\overline{ERRB}$	9.5	17.5				9.5		

## 54F/74F968 1 Mbit Dynamic RAM Controller

### General Description

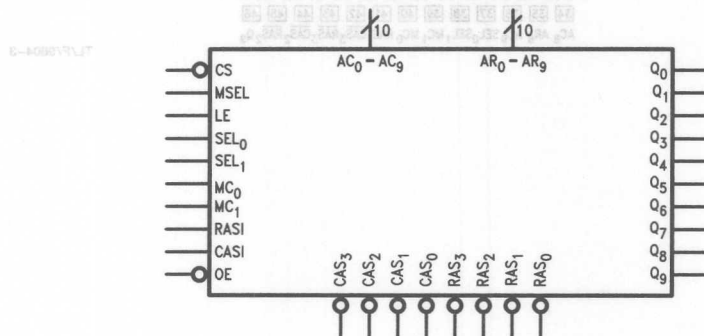
The 'F968 is a high performance memory controller, replacing many SSI and MSI devices by grouping several unique functions. It provides two 10-bit address latches and two 10-bit counters for row and column address generation during refresh. A 2-bit bank select latch for row and column address generation during refresh and a 2-bit bank select latch for the two high order address bits are provided to select one of the four RAS and CAS outputs.

### Features

- Provides control for 16k, 64k, 256k or 1 Mbit DRAM systems
- Outputs directly drive up to 88 DRAMs
- Chip select for easy expansion
- Provides memory refresh with error correction mode
- 52-pin plastic leaded chip carrier

**Ordering Code:** See Section 5

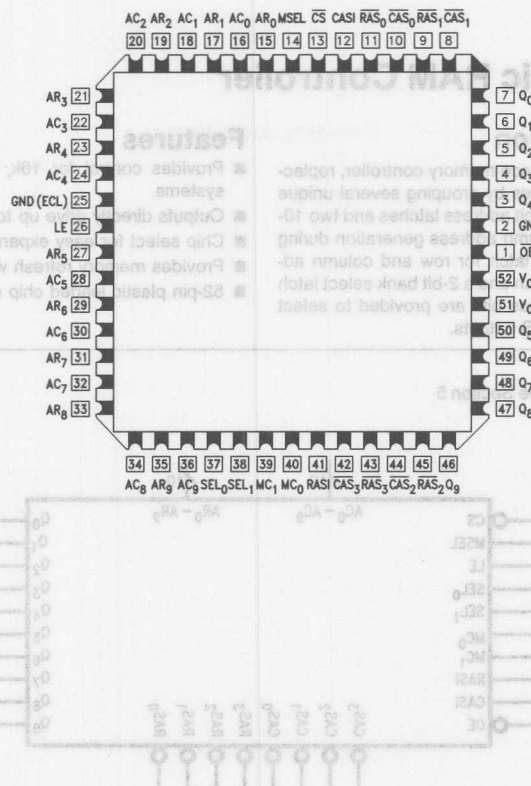
### Logic Symbol



TL/F/9604-1

# Connection Diagram

## Pin Assignment for PCC



TL/F/9604-3

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
AC <sub>0</sub> –AC <sub>9</sub>	Column Address Inputs	1.0/1.0	20 $\mu$ A/–0.6 mA
AR <sub>0</sub> –AR <sub>9</sub>	Row Address Inputs	1.0/1.0	20 $\mu$ A/–0.6 mA
MC <sub>0</sub> , MC <sub>1</sub>	Mode Control Inputs	1.0/1.0	20 $\mu$ A/–0.6 mA
CS	Chip Select Input	1.0/1.0	20 $\mu$ A/–0.6 mA
MSEL	Multiplexer Select Input	1.0/1.0	20 $\mu$ A/–0.6 mA
LE	Latch Enable Input	1.0/1.0	20 $\mu$ A/–0.6 mA
SEL <sub>0</sub> , SEL <sub>1</sub>	Bank Select Inputs	1.0/1.0	20 $\mu$ A/–0.6 mA
RASI	Row Address Strobe In	1.0/1.0	20 $\mu$ A/–0.6 mA
CASI	Column Address Strobe In	1.0/1.0	20 $\mu$ A/–0.6 mA
OE	Output Enable	1.0/1.0	20 $\mu$ A/–0.6 mA
RAS <sub>0</sub> –RAS <sub>3</sub>	Row Address Strobe Outputs	150/1.667	–3 mA/1.0 mA
CAS <sub>0</sub> –CAS <sub>3</sub>	Column Address Strobe Outputs	150/1.667	–3 mA/1.0 mA
Q <sub>0</sub> –Q <sub>9</sub>	Address Outputs	150/1.667	–3 mA/1.0 mA

**Pin Description**

Name	I/O	Description
AR <sub>0</sub> –AR <sub>9</sub> AC <sub>0</sub> –AC <sub>9</sub>	I	<b>Address Inputs.</b> AR <sub>0</sub> –AR <sub>9</sub> are latched in as the 10-bit Row Address for the RAM. These inputs drive Q <sub>0</sub> –Q <sub>9</sub> when the 'F968 is in the Read/Write mode and MSEL is LOW. AC <sub>0</sub> –AC <sub>9</sub> are latched in as the Column Address, and will drive Q <sub>0</sub> –Q <sub>9</sub> when MSEL is HIGH and the 'F968 is in the Read/Write mode. The addresses are latched with the Latch Enable (LE) signal.
SEL <sub>0</sub> –SEL <sub>1</sub>	I	<b>Bank Select.</b> These two inputs are normally the two higher order address bits, and are used in the Read/Write mode to select which bank of memory will be receiving the RAS <sub>n</sub> and CAS <sub>n</sub> signals after RASI and CASI go HIGH.
LE	I	<b>Latch Enable.</b> This active-HIGH input causes the Row, Column and Bank Select latches to become transparent, allowing the latches to accept new input data. A LOW input on LE latches the input data, assuming it meets the setup and hold time requirements.
MSEL	I	<b>Multiplexer Select.</b> This input determines whether the Row or Column Address will be sent to the memory address inputs. When MSEL is HIGH the Column Address is selected, while the Row Address is selected when MSEL is LOW. The address may come from either the address latch or refresh address counter depending on MC <sub>0</sub> , MC <sub>1</sub> .
CS	I	<b>Chip Select.</b> This active-LOW input is used to enable the 'F968. When CS is active, the 'F968 operates normally in all four modes. When CS goes HIGH, the device will not enter the Read/Write mode. This allows other devices to access the same memory that the 'F968 is controlling (e.g., DMA controller).
OE	I	<b>Output Enable.</b> This active-LOW input enables/disables the output signals. When OE is HIGH, the outputs of the 'F968 enter the high impedance state. The OE signal allows more than one 'F968 to control the same memory, thus providing an easy method to expand the memory size.
MC <sub>0</sub> , MC <sub>1</sub>	I	<b>Mode Control.</b> These inputs are used to specify which of the four operating modes the 'F968 should be using. The description of the four operating modes is given in the Mode Control Function Table.
Q <sub>0</sub> –Q <sub>9</sub>	O	<b>Address Outputs.</b> These address outputs will feed the DRAM address inputs and provide drive for memory systems up to 500 pF in capacitance.
RASI	I	<b>Row Address Strobe Input.</b> During normal memory cycles, the decoded RAS <sub>n</sub> output (RAS <sub>0</sub> , RAS <sub>1</sub> , RAS <sub>2</sub> or RAS <sub>3</sub> ) is forced LOW after receipt of RASI. In either refresh mode, all four RAS <sub>n</sub> outputs will go LOW following RASI going HIGH.
RAS <sub>0</sub> –RAS <sub>3</sub>	O	<b>Row Address Strobe.</b> Each one of the Row Address Strobe outputs provides a RAS <sub>n</sub> signal to one of the four banks of dynamic memory. Each will go LOW only when selected by SEL <sub>0</sub> and SEL <sub>1</sub> and only after RASI goes HIGH. All four go LOW in response to RASI in either of the Refresh modes.
CASI	I	<b>Column Address Strobe Input.</b> This input going active will cause the selected CAS <sub>n</sub> output to be forced LOW.
CAS <sub>0</sub> –CAS <sub>3</sub>	O	<b>Column Address Strobe.</b> During normal Read/Write cycles the two select bits (SEL <sub>0</sub> , SEL <sub>1</sub> ) determine which CAS <sub>n</sub> output will go active following CASI going HIGH. When memory error correction is performed, only the CAS <sub>n</sub> signal selected by CNTR <sub>0</sub> and CNTR <sub>1</sub> will be active. For non-error correction cycles, all four CAS <sub>n</sub> outputs remain HIGH.



## Functional Description

The 74F968 is a 1 Mbit DRAM controller which is functionally equivalent to AMD's Am29368. The 74F968 provides row/column address multiplexing, refresh address generation and bank selection for up to four banks of RAMs.

Twenty-two (22) address bits ( $AR_0-AR_9$ ,  $AC_0-AC_9$  and bank select addresses  $SEL_0$  and  $SEL_1$ ) are presented to the controller. These addresses are latched by a 22-bit latch. A 22-bit counter generates the refresh address.

A 10-bit multiplexer selects the output address between the input row address, column address, refresh counter row address, column address, or zero (clear). Four RAS and four CAS outputs select the appropriate bank of RAMs and strobe in the row and column addresses.

It should be noted that the counters are cleared ( $MC_0$ ,  $MC_1 = 1, 1$ ) on the next RAS<sub>i</sub> transition, but the Q outputs are asynchronously cleared through the multiplexer.

Mode Control Function Table

$MC_1$	$MC_0$	Operating Mode
L	L	<b>Refresh without Error Correction</b> — Refresh cycles are performed with only the Row Counter being used to generate addresses. In this mode, all four $RAS_n$ outputs are active while the four $CAS_n$ signals are kept HIGH.
L	H	<b>Refresh with Error Correction/Initialize</b> — During this mode, refresh cycles are done with both the Row and Column counters generating the addresses. MSEL is used to select between the Row and Column counter. All four $RAS_n$ outputs go active in response to RAS <sub>i</sub> , while only one $CAS_n$ output goes LOW in response to CAS <sub>i</sub> . The Bank Counter keeps track of which $CAS_n$ output will go active. This mode of operation is possible when supported by an error detection/correction circuit such as the 'F632.
H	L	<b>Read/Write</b> — This mode is used to perform Read/Write cycles. Both the Row and Column addresses are latched and multiplexed to the address output lines using MSEL; $SEL_0$ and $SEL_1$ are decoded to determine which $RAS_n$ and $CAS_n$ will be active.
H	H	<b>Clear Refresh Counter</b> — This mode will clear the three refresh counters (Row, Column and Bank) on the HIGH-to-LOW transition of RAS <sub>i</sub> , putting them at the start of the refresh sequence. In this mode, all four $RAS_n$ outputs are driven LOW upon receipt of RAS <sub>i</sub> so that DRAM wake-up cycles are performed. This mode also asynchronously clears the $Q_n$ outputs.

H = HIGH Voltage Level

L = LOW Voltage Level

Address Output Function Table

CS	$MC_1$	$MC_0$	MSEL	Mode	MUX Output
L	L	L	X	Refresh without Error Correction	Row Counter Address
	L	H	H	Refresh with Error Correction	Column Counter Address
	L	L	L	Refresh with Error Correction	Row Counter Address
	H	L	H	Read/Write	Column Address Latch
H	L	L	L	Read/Write	Row Address Latch
	H	H	X	Clear Refresh Counter	Zero
	L	L	X	Refresh without Error Correction	Row Counter Address
	L	H	H	Refresh with Error Correction	Column Counter Address
H	H	L	X	Read/Write	Zero
	H	H	X	Clear Refresh Counter	Zero

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

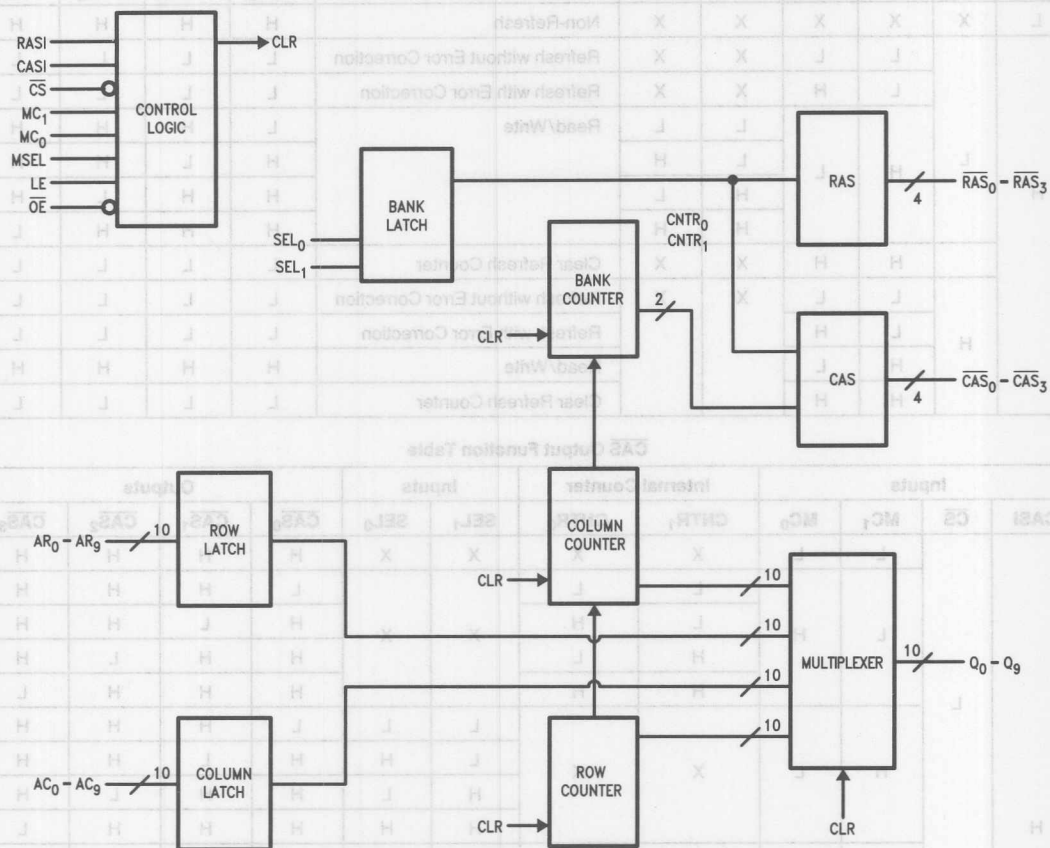
RAS Output Function Table

RAS <sub>I</sub>	$\overline{CS}$	MC <sub>1</sub>	MC <sub>0</sub>	SEL <sub>1</sub>	SEL <sub>0</sub>	Mode	RAS <sub>0</sub>	RAS <sub>1</sub>	RAS <sub>2</sub>	RAS <sub>3</sub>
L	X	X	X	X	X	Non-Refresh	H	H	H	H
H	L	L	L	X	X	Refresh without Error Correction	L	L	L	L
		L	H	X	X	Refresh with Error Correction	L	L	L	L
		H	L	L	L	Read/Write	L	H	H	H
				L	H		H	L	H	H
				H	L		H	H	L	H
				H	H		H	H	H	L
		H	H	X	X	Clear Refresh Counter	L	L	L	L
	H	L	L	X	X	Refresh without Error Correction	L	L	L	L
		L	H			Refresh with Error Correction	L	L	L	L
		H	L			Read/Write	H	H	H	H
		H	H			Clear Refresh Counter	L	L	L	L

CAS Output Function Table

Inputs				Internal Counter		Inputs		Outputs			
CAS <sub>I</sub>	$\overline{CS}$	MC <sub>1</sub>	MC <sub>0</sub>	CNTR <sub>1</sub>	CNTR <sub>0</sub>	SEL <sub>1</sub>	SEL <sub>0</sub>	CAS <sub>0</sub>	CAS <sub>1</sub>	CAS <sub>2</sub>	CAS <sub>3</sub>
H	L	L	L	X	X	X	X	H	H	H	H
		L	L	L	L	X	X	L	H	H	H
		L	H	L	H			H	L	H	H
		L	H	H	L			H	H	L	H
		L	H	H	H			H	H	H	L
		H	L	X	X	L	L	L	H	H	H
		H	L	X	H	L	H	H	L	H	H
		H	L	H	L	H	L	H	H	L	H
	H	H	H	X	X	X	X	H	H	H	H
		L	L	X	X	X	X	H	H	H	H
		L	L	L	L	X	X	L	H	H	H
		L	H	L	H			H	L	H	H
		L	H	H	L			H	H	L	H
		L	H	H	H			H	H	H	L
		H	L	X	X	X	X	H	H	H	H
		H	H	X	X	X	X	H	H	H	H
L	X	X	X	X	X	X	X	H	H	H	H

## Block Diagram



TL/F/9604-4

## Memory Cycle Timing

The relationship between the 'F968 specifications and system timing requirements is shown in Figures 1-6. T<sub>1</sub>, T<sub>2</sub> and T<sub>3</sub> represent the minimum timing requirements at the 'F968 inputs to guarantee that the RAM timing requirements are met and that maximum system performance is achieved.

The minimum requirement for T<sub>1</sub>, T<sub>2</sub> and T<sub>3</sub> are as follows:

$$T_1 \text{ Min} = t_{\text{ASR}} + t_{\text{skew}}$$

$$T_2 \text{ Min} = t_{\text{RAH}} + t_{\text{skew}}$$

$$T_3 \text{ Min} = T_2 + t_{\text{skew}} + t_{\text{ASC}}$$

See RAM data sheet for applicable values for  $t_{\text{RAH}}$ ,  $t_{\text{ASC}}$  and  $t_{\text{ASR}}$ .

## Memory Cycle Timing (Continued)

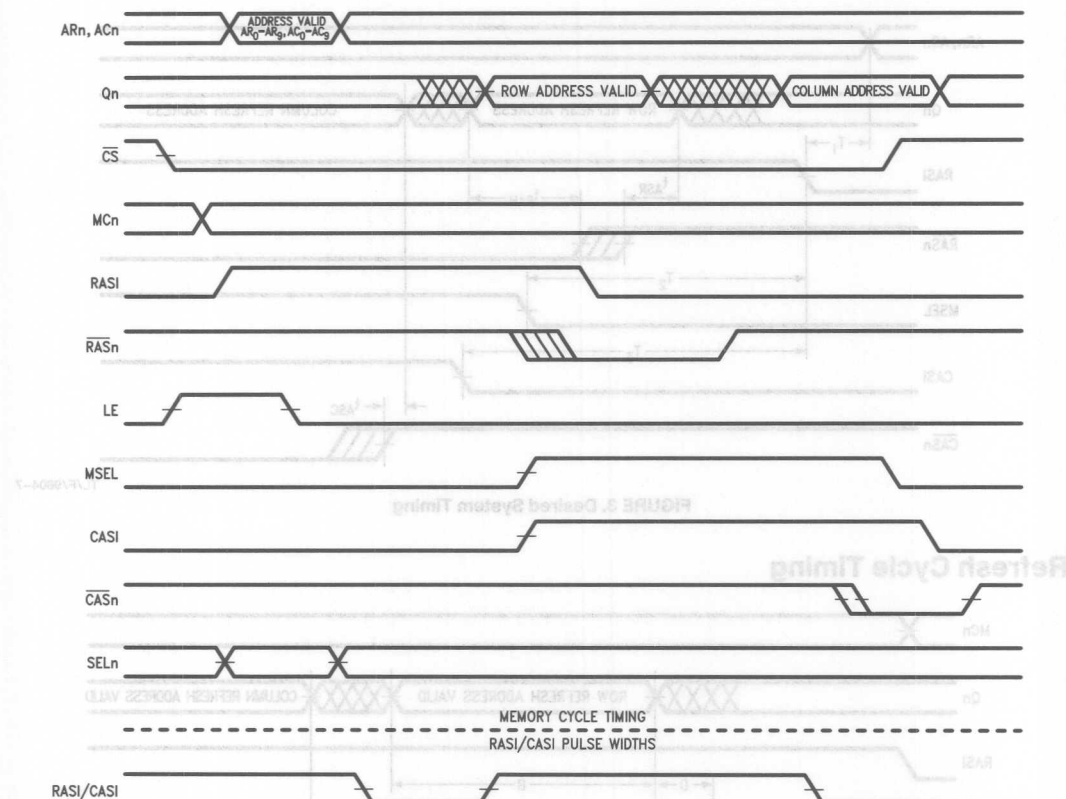
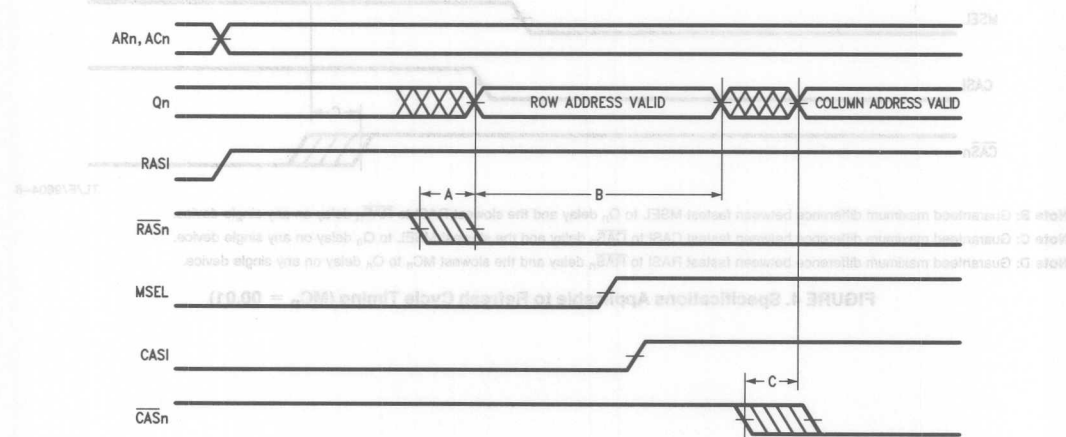


FIGURE 1. Dynamic Memory Controller Timing

TL/F/9604-5



- Note A:** Guaranteed maximum difference between fastest RASi to  $\overline{\text{RAS}}_n$  delay and the slowest  $A_n$  to  $Q_n$  delay on any single device.  
**Note B:** Guaranteed maximum difference between fastest MSEL to  $Q_n$  delay and the slowest RASi to  $\overline{\text{RAS}}_n$  delay on any single device.  
**Note C:** Guaranteed maximum difference between fastest CASi to  $\overline{\text{CAS}}_n$  delay and the slowest MSEL to  $Q_n$  delay on any single device.

FIGURE 2. Specifications Applicable to Memory Cycle Timing ( $\text{MC}_n = 1,0$ )

TL/F/9604-6

## Memory Cycle Timing (Continued)

Memory Cycle Timing (Continued)

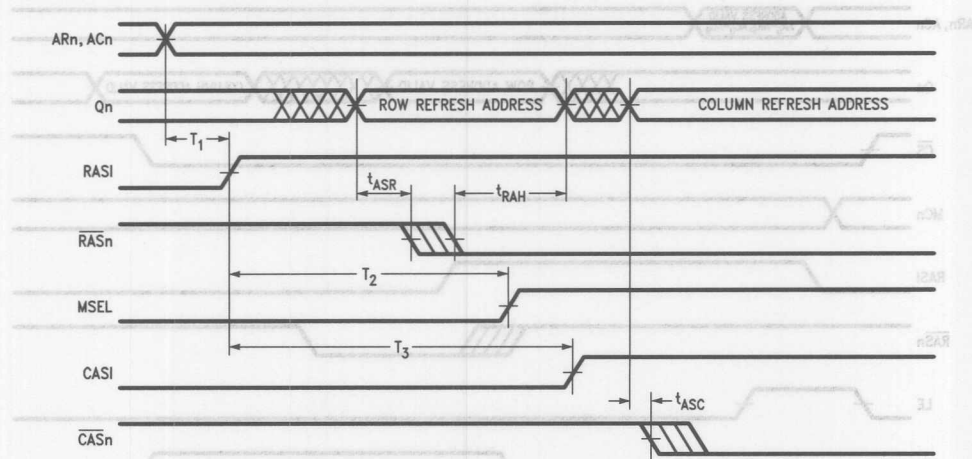
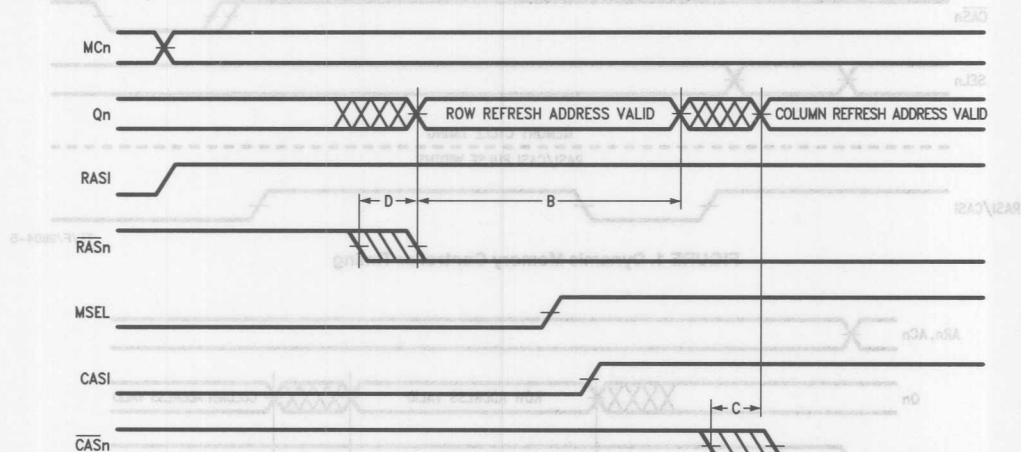


FIGURE 3. Desired System Timing

TL/F/9604-7

## Refresh Cycle Timing



TL/F/9604-8

**Note B:** Guaranteed maximum difference between fastest MSEL to  $Q_n$  delay and the slowest RASi to  $RAS_n$  delay on any single device.

**Note C:** Guaranteed maximum difference between fastest CASi to  $CAS_n$  delay and the slowest MSEL to  $Q_n$  delay on any single device.

**Note D:** Guaranteed maximum difference between fastest RASi to  $RAS_n$  delay and the slowest  $MC_n$  to  $Q_n$  delay on any single device.

FIGURE 4. Specifications Applicable to Refresh Cycle Timing ( $MC_n = 00,01$ )

TL/F/9604-9

**Note A:** Guaranteed maximum difference between fastest RASi to  $RAS_n$  delay and the slowest  $MC_n$  to  $Q_n$  delay on any single device.

**Note B:** Guaranteed maximum difference between fastest MSEL to  $Q_n$  delay and the slowest RASi to  $RAS_n$  delay on any single device.

**Note C:** Guaranteed maximum difference between fastest CASi to  $CAS_n$  delay and the slowest MSEL to  $Q_n$  delay on any single device.

FIGURE 5. Specifications Applicable to Memory Cycle Timing ( $MC_n = 10$ )

## Refresh Cycle Timing (Continued)

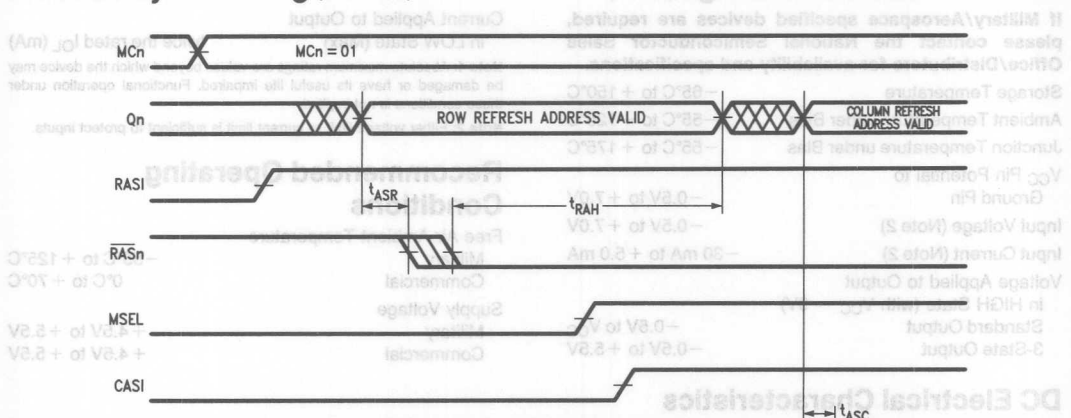


FIGURE 5. Designed Timing—Refresh with Error Correction

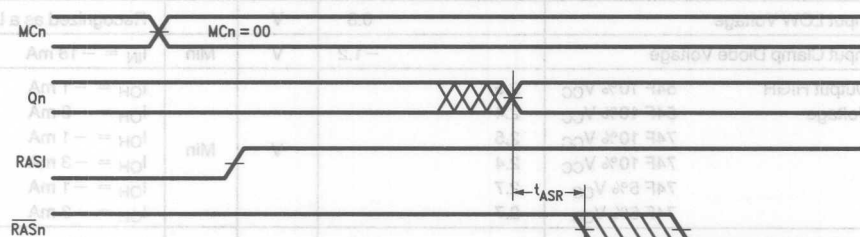


FIGURE 6. Desired Timing—Refresh without Error Correction

Symbol	Min	Typ	Max	Units	V <sub>CC</sub>	Comments
$t_{RAH}$	0.5	0.5	0.5	ns		Row Address Valid
$t_{ASC}$	0.5	0.5	0.5	ns		Column Address Valid
$t_{RAS}$	0.5	0.5	0.5	ns		Row Address Strobe
$t_{CAS}$	0.5	0.5	0.5	ns		Column Address Strobe
$t_{MCn}$	0.5	0.5	0.5	ns		Master Chip Enable
$t_{Qn}$	0.5	0.5	0.5	ns		Data Output
$t_{MSEL}$	0.5	0.5	0.5	ns		Memory Select



## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output	−0.5V to V <sub>CC</sub>
3-State Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max)

twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 1.0 mA
		54F 10% V <sub>CC</sub>		0.8			I <sub>OL</sub> = 12 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 1.0 mA
		74F 10% V <sub>CC</sub>		0.8			I <sub>OL</sub> = 12 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−60	−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Buss Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current			300	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			300	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current			300	mA	Max	V <sub>O</sub> = HIGH Z

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F									Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 500\text{ pF}^*$					
		Min	Typ	Max	Min	Max	Min	Typ	Max			
$t_{PLH}$ $t_{PHL}$	Propagation Delay AR to $Q_n$	3.0 3.0	7.0 7.0	11.0 11.0	2.5 2.5	12.0 12.0		19.0 22.0		ns	2-3	
$t_{PLH}$ $t_{PHL}$	Propagation Delay AC to $Q_n$	3.0 3.0	7.0 7.0	11.0 11.0	2.5 2.5	12.0 12.0		19.0 22.0		ns	2-3	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $RAS_1$ to $RAS_n$	3.5 3.5	8.0 7.0	12.0 12.0	3.0 3.0	13.0 13.0		23.0 20.0		ns	2-3	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $CAS_1$ to $CAS_n$	1.0 1.0	6.0 4.0	8.0 8.0	1.0 1.0	8.5 8.5		19.0 17.0		ns	2-3	
$t_{PLH}$ $t_{PHL}$	Propagation Delay MSEL to $Q_n$	3.0 3.0	9.0 8.0	13.0 13.0	2.5 2.5	14.0 14.0		24.0 21.0		ns	2-3	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $MC_n$ to $Q_n$	4.0 4.0	10.0 9.0	15.0 15.0	3.5 3.5	16.0 16.0		25.0 22.0		ns	2-3	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $MC_n$ to $RAS_n$	3.5 3.5	11.0 8.0	17.5 17.5	3.0 3.0	18.5 18.5		24.0 22.0		ns	2-3	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $MC_n$ to $CAS_n$	4.0 4.0	8.0 9.0	12.5 12.5	3.5 3.5	13.5 13.5		23.0 21.0		ns	2-3	
$t_{PLH}$ $t_{PHL}$	Propagation Delay LE to $RAS_n$	4.0 4.0	10.0 9.0	15.0 15.0	3.5 3.5	16.0 16.0		25.0 24.0		ns	2-3	
$t_{PLH}$ $t_{PHL}$	Propagation Delay LE to $CAS_n$	5.0 5.0	9.0 9.0	13.5 13.5	4.5 4.5	14.5 14.5		24.0 24.0		ns	2-3	
$t_{PLH}$ $t_{PHL}$	Propagation Delay LE to $Q_n$	3.5 3.5	8.0 7.0	12.0 12.0	3.0 3.0	13.0 13.0		23.0 22.0		ns	2-3	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{CS}$ to $Q_n$	3.0 3.0	10.0 8.0	14.5 14.5	3.0 3.0	15.5 15.5		25.0 23.0		ns	2-3	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{CS}$ to $RAS_n$	3.5 3.5	8.0 8.0	13.0 13.0	3.0 3.0	14.0 14.0		23.0 23.0		ns	2-3	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{CS}$ to $CAS_n$	4.0 4.0	8.0 8.0	11.5 11.5	3.5 3.5	12.5 12.5		23.0 23.0		ns	2-3	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $SEL_n$ to $RAS_n$	4.0 4.0	9.0 8.0	15.5 15.5	3.5 3.5	16.0 16.0		24.0 23.0		ns	2-3	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $SEL_n$ to $CAS_n$	4.5 4.5	9.0 9.0	14.5 14.5	4.0 4.0	15.5 15.5		24.0 24.0		ns	2-3	

\*These values are given for typical derivative with a 500 pF load; these are not guaranteed specifications.

# AC Electrical Characteristics (Continued): See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F						Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$				
		Min	Typ	Max	Min	Max			
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{OE}$ to $Q_n$	1.0 1.0	5.0 4.0	9.5 9.5	1.0 1.0	10.0 10.0	ns	2-5	
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{OE}$ to $Q_n$	1.0 1.0	5.0 6.0	9.5 9.5	1.0 1.0	10.0 10.0	ns	2-5	
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{OE}$ to $\overline{RAS}_n$	1.0 1.0	5.0 4.0	9.5 9.5	1.0 1.0	10.0 10.0	ns	2-5	
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{OE}$ to $\overline{RAS}_n$	1.0 1.0	5.0 6.0	9.5 9.5	1.0 1.0	10.0 10.0	ns	2-5	
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{OE}$ to $\overline{CAS}_n$	1.0 1.0	5.0 4.0	9.5 9.5	1.0 1.0	10.0 10.0	ns	2-5	
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{OE}$ to $\overline{CAS}_n$	1.0 1.0	5.0 6.0	9.5 9.5	1.0 1.0	10.0 10.0	ns	2-5	

## AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F				Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> , V <sub>CC</sub> = Com			
		Min	Max	Min	Max		
t <sub>s</sub> (H)	Setup Time, HIGH or LOW	5.0		5.0		ns	2-6
t <sub>s</sub> (L)	A <sub>n</sub> to LE	5.0		5.0			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	5.0		5.0		ns	2-6
t <sub>h</sub> (L)	A <sub>n</sub> to LE	5.0		5.0			
t <sub>s</sub> (H)	Setup Time, HIGH or LOW	5.0		5.0		ns	2-6
t <sub>s</sub> (L)	SEL to LE	5.0		5.0			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	5.0		5.0		ns	2-6
t <sub>h</sub> (L)	SEL to LE	5.0		5.0			
t <sub>w</sub> (H)	Pulse Width, HIGH or LOW	15.0		15.0		ns	2-4
t <sub>w</sub> (L)	$\overline{CAS}_n, \overline{RAS}_n$	15.0		15.0			
t <sub>skew</sub>	Q <sub>n</sub> to $\overline{CAS}_n, \overline{RAS}_n$	10.0		10.0		ns	

\*These values are given for typical behavior with a 500 pF load; these are not guaranteed specifications.



# 54F/74F2241•54F/74F2244 Octal Buffers/Line Drivers with 25Ω Series Resistors in Outputs

## General Description

The 'F2241 and 'F2244 are octal buffers and line drivers designed to drive the capacitive inputs of MOS memory drivers, address drivers, clock drivers and bus-oriented transmitters/receivers.

The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

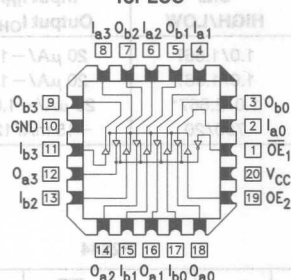
## Features

- TRI-STATE® outputs drive bus lines or buffer memory address registers
- 12 mA source current
- 25Ω series resistors in outputs eliminate the need for external resistors.
- Designed to drive the capacitive inputs of MOS devices
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

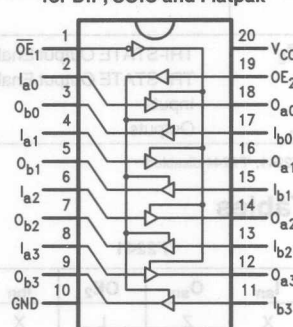
## Connection Diagrams

Pin Assignment  
for LCC



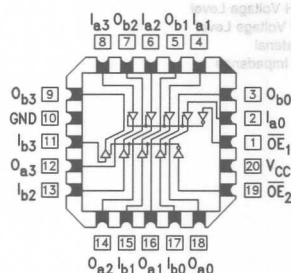
'F2241

Pin Assignment  
for DIP, SOIC and Flatpak

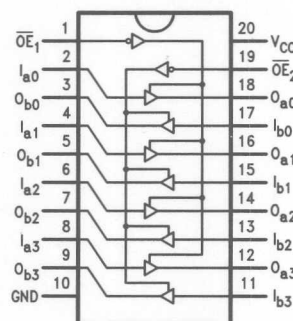


TL/F/9499-2

'F2244

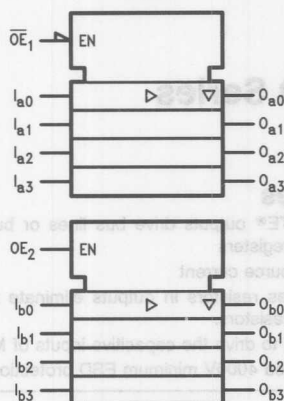


TL/F/9499-3

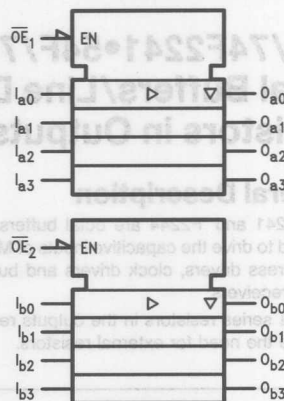


TL/F/9499-4

## Logic Symbols

IEEE/IEC  
'F2241

TL/F/9499-5

IEEE/IEC  
'F2244

TL/F/9499-6

## Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{OE}_1, \overline{OE}_2$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.667	20 $\mu$ A/ -1 mA
$OE_2$	TRI-STATE Output Enable Input (Active HIGH)	1.0/1.667	20 $\mu$ A/ -1 mA
$I_{an}, I_{bn}$	Inputs	1.0/2.667*	20 $\mu$ A/ -1.6 mA
$O_{an}, O_{bn}$	Outputs	750/20	-15 mA/12 mA

\*Worst-case 'F2241, 'F2244 disabled

## Truth Tables

'F2241

$\overline{OE}_1$	$I_{an}$	$O_{an}$	$OE_2$	$I_{bn}$	$O_{bn}$
H	X	Z	L	X	Z
L	H	H	H	H	H
L	L	L	H	L	L

'F2244

$\overline{OE}_1$	$I_{an}$	$O_{an}$	$\overline{OE}_2$	$I_{bn}$	$O_{bn}$
H	X	Z	H	X	Z
L	H	H	L	H	H
L	L	L	L	L	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

ESD Last Passing Voltage (Min) 4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	−55°C to +125°C
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.4 2.0 2.4 2.0 2.7		V	Min	I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −12 mA I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −15 mA I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage		0.50 0.75		V	Min	I <sub>OL</sub> = 1 mA I <sub>OL</sub> = 12 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All other pins grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All other pins grounded
I <sub>IL</sub>	Input LOW Current			−1.0 −1.6	mA	Max	V <sub>IN</sub> = 0.5V ( $\overline{OE}_1$ , $\overline{OE}_2$ , OE <sub>2</sub> ) V <sub>IN</sub> = 0.5V (I <sub>n</sub> )
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		−100	−225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		40	60	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		60	90	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		60	90	mA	Max	V <sub>O</sub> = HIGH Z



# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	1.5		7.0	2.0	6.5	1.5	7.0	ns	2-3
$t_{PHL}$	Data to Output	2.5		8.0	2.0	7.0	2.0	8.0		
$t_{PZH}$	Output Enable Time	1.5		9.0	2.0	7.0	1.0	9.5	ns	2-5
$t_{PZL}$		2.5		11.5	2.0	8.5	2.5	12.0		
$t_{PHZ}$	Output Disable Time	1.5		9.0	2.0	7.0	1.0	9.5		
$t_{PLZ}$		1.5		8.5	2.0	7.5	1.5	9.5		

Note 2: ESD voltage limit or current limit is sufficient to protect inputs.  
Note 3: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.  
Note 4: ESD Last Passing Voltage (Min) 4000V  
Current Applied to Output in LOW State (Max) twice the rated  $I_{OL}$  (mA)

## DC Electrical Characteristics

Symbol	Parameter	Units	$V_{CC}$	74F		
				Min	Typ	Max
$V_{IH}$	Input HIGH Voltage	V		2.0		
$V_{IL}$	Input LOW Voltage	V		0.8		
$V_{CD}$	Input Clamp Diode Voltage	V	Min	-1.5		
$V_{OH}$	Output HIGH Voltage	V	Min	2.4		
				2.4		
				2.4		
				2.4		
				2.4		
				2.4		
$V_{OL}$	Output LOW Voltage	V	Min	0.80		
				0.75		
$I_{IH}$	Input HIGH Current	$\mu\text{A}$	Max	50.0		
				8.0		
$I_{AIL}$	Input LOW Current	$\mu\text{A}$	Max	100		
				7.0		
$I_{OZH}$	Output HIGH Leakage Current	$\mu\text{A}$	Max	250		
				20		
$V_{ID}$	Input Leakage Test	V	0.0	4.75		
$I_{OD}$	Output Leakage Current	$\mu\text{A}$	0.0	3.75		
$I_{IL}$	Input LOW Current	mA	Max	-1.0		
				-1.6		
$I_{OZH}$	Output Leakage Current	$\mu\text{A}$	Max	50		
$I_{OLZ}$	Output Leakage Current	$\mu\text{A}$	Max	-50		
$I_{OS}$	Output Short-Circuit Current	mA	Max	-250		
				-100		
$I_{OCH}$	Power Supply Current	mA	Max	40		
$I_{OCL}$	Power Supply Current	mA	Max	60		
$I_{OCS}$	Power Supply Current	mA	Max	60		



54F/74F2243

## Quad Bus Transceiver with 25Ω Series Resistors in the Outputs

### General Description

The 'F2243 is a quad bus transmitter/receiver which can be used for 4-line asynchronous 2-way data communications between data busses. It is designed to drive the capacitive inputs of MOS memory drivers, address drivers, clock drivers, and bus-oriented transmitters/receivers.

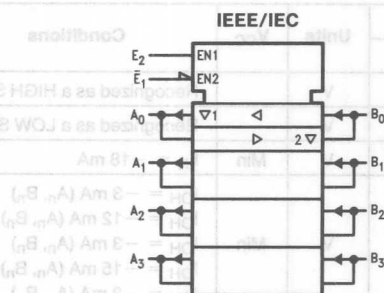
The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

### Features

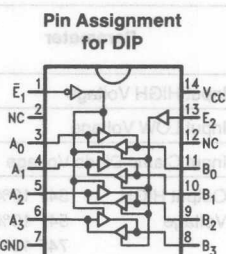
- 25Ω series resistors in outputs eliminate the need for external resistors
- 2-Way asynchronous data bus communication
- TRI-STATE® outputs
- 12 mA source current
- Designed to drive the capacitive inputs of MOS devices
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 5

### Logic Symbol



### Connection Diagram



TL/F/9530-2

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\bar{E}_1$	Enable Input (Active LOW)	1.0/1.67	20 $\mu$ A / -1 mA
$E_2$	Enable Input (Active HIGH)	1.0/1.67	20 $\mu$ A / -1 mA
$A_n, B_n$	Inputs Outputs	3.5/2.67 750/20	70 $\mu$ A / -1.6 mA -15 mA/12 mA

### Truth Table

Inputs		Inputs/Outputs	
$\bar{E}_1$	$E_2$	$A_n$	$B_n$
L	L	Input	$B = A$
L	H	N/A	N/A
H	L	Z	Z
H	H	$A = B$	Input

H = HIGH Voltage Level  
L = LOW Voltage Level  
Z = High Impedance  
N/A = Not Allowed

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA

Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
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ESD Last Passing Voltage (Min)	4000V
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**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.4		V	Min	I <sub>OH</sub> = -3 mA (A <sub>n</sub> , B <sub>n</sub> )
		54F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = -12 mA (A <sub>n</sub> , B <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = -3 mA (A <sub>n</sub> , B <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = -15 mA (A <sub>n</sub> , B <sub>n</sub> )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -3 mA (A <sub>n</sub> , B <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage		0.50		V	Min	I <sub>OL</sub> = 1 mA (A <sub>n</sub> , B <sub>n</sub> )
			0.75				I <sub>OL</sub> = 12 mA (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current		20		μA	Max	V <sub>IN</sub> = 2.7V (E <sub>1</sub> , E <sub>2</sub> )
I <sub>BVI</sub>	Input HIGH Current Breakdown Test		100		μA	Max	V <sub>IN</sub> = 7.0V (E <sub>1</sub> , E <sub>2</sub> )
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)		1.0		mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub>	Input LOW Current		-1.0		mA	Max	V <sub>IN</sub> = 0.5V (E <sub>1</sub> , E <sub>2</sub> )
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current		70		μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current		-1.6		mA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current	-100	-225		mA	Max	V <sub>OUT</sub> = 0V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current		250		μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>CCH</sub>	Power Supply Current		64	80	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		64	90	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		71	90	mA	Max	V <sub>O</sub> = HIGH Z

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V





## 54F/74F2620 • 54F/74F2623

### Inverting Octal Bus Transceiver with 25Ω Series Resistors in the Outputs

#### General Description

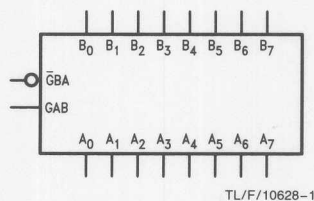
These devices are octal bus transceivers designed for asynchronous two-way data flow between the A and B busses. These devices are functionally equivalent to the 'F620 and 'F623. The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors. Both busses are capable of sinking 12 mA, sourcing 15 mA, and have TRI-STATE outputs. Dual enable pins (GAB,  $\overline{\text{GAB}}$ ) allow data transmission from the A bus to the B bus or from the B bus to the A bus. The 'F2620 is an inverting option of the 'F2623.

#### Features

- 25Ω series resistors in the outputs eliminate the need for external resistors.
- Designed for asynchronous two-way data flow between busses
- Outputs sink 12 mA and source 15 mA
- Dual enable inputs control direction of data flow
- Guaranteed 4000V minimum ESD protection
- 'F2620 is an inverting option of the 'F2623

#### Ordering Code: See Section 5

#### Logic Symbol

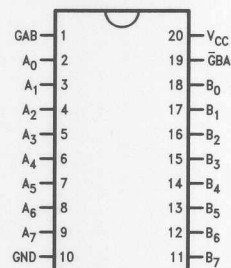


#### Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{\text{GAB}}, \text{GAB}$	Enable Inputs	1.0/1.0	20 $\mu\text{A}$ / -0.6 mA
$A_0-A_7$	A Inputs or TRI-STATE Outputs	3.5/0.667	70 $\mu\text{A}$ / -0.4 mA - 15 mA / 12 mA
$B_0-B_7$	B Inputs or TRI-STATE Outputs	3.5/0.667	70 $\mu\text{A}$ / -0.4 mA - 15 mA / 12 mA

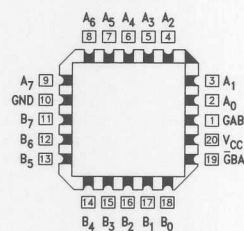
#### Connection Diagrams

##### Pin Assignment for DIP, SOIC and Flatpak



TL/F/10628-2

##### Pin Assignment for LCC



TL/F/10628-3

## Functional Description

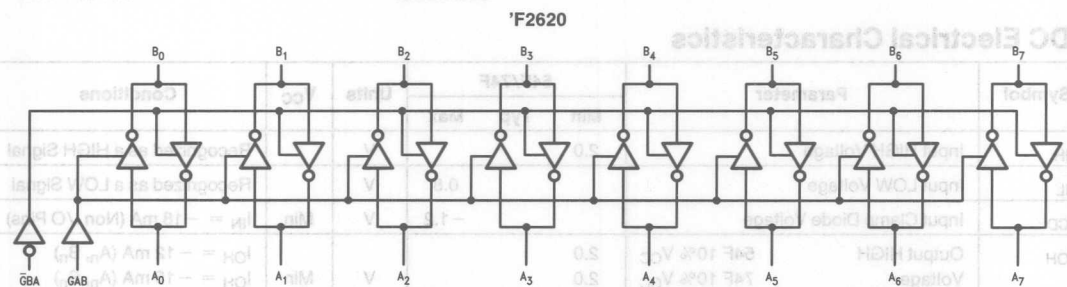
The enable inputs GAB and  $\overline{\text{GBA}}$  control whether data is transmitted from the A bus to the B bus or from the B bus to the A bus. If both  $\overline{\text{GBA}}$  and GAB are disabled ( $\overline{\text{GBA}}$  HIGH and GAB low), the outputs are in the high impedance state and data is stored at the A and B busses. When  $\overline{\text{GBA}}$  is active (LOW), B data is sent to the A bus. When GAB is active (HIGH), data from the A bus is sent to the B bus. If both enable inputs are active ( $\overline{\text{GBA}}$  LOW and GAB HIGH) B data is sent to the A bus while A data is sent to the B bus.

### Function Table

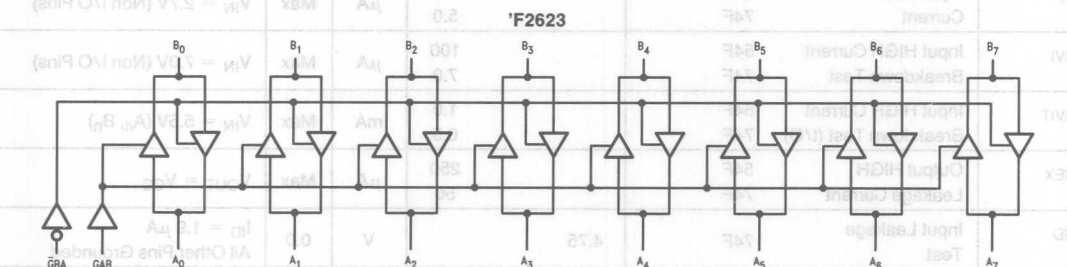
Enable Inputs		Operation	
$\overline{\text{GBA}}$	GAB	'F2620	'F2623
L	L	$\overline{\text{B}}$ Data to A Bus	B Data to A Bus
H	H	$\overline{\text{A}}$ Data to B Bus	A Data to B Bus
H	L	Z	Z
L	H	$\overline{\text{B}}$ Data to A Bus, $\overline{\text{A}}$ Data to B Bus	B Data to A Bus, A Data to B Bus

H = HIGH Voltage Level  
L = LOW Voltage Level  
Z = High Impedance

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

Voltage Applied to Output  
in HIGH State (with V<sub>CC</sub> = 0V)  
Standard Output −0.5V to V<sub>CC</sub>  
TRI-STATE Output −0.5V to +5.5V  
Current Applied to Output  
in LOW State (Max) twice the rated I<sub>OL</sub> (mA)  
ESD Last Passing Voltage (Min) 4000V

**Recommended Operating Conditions**

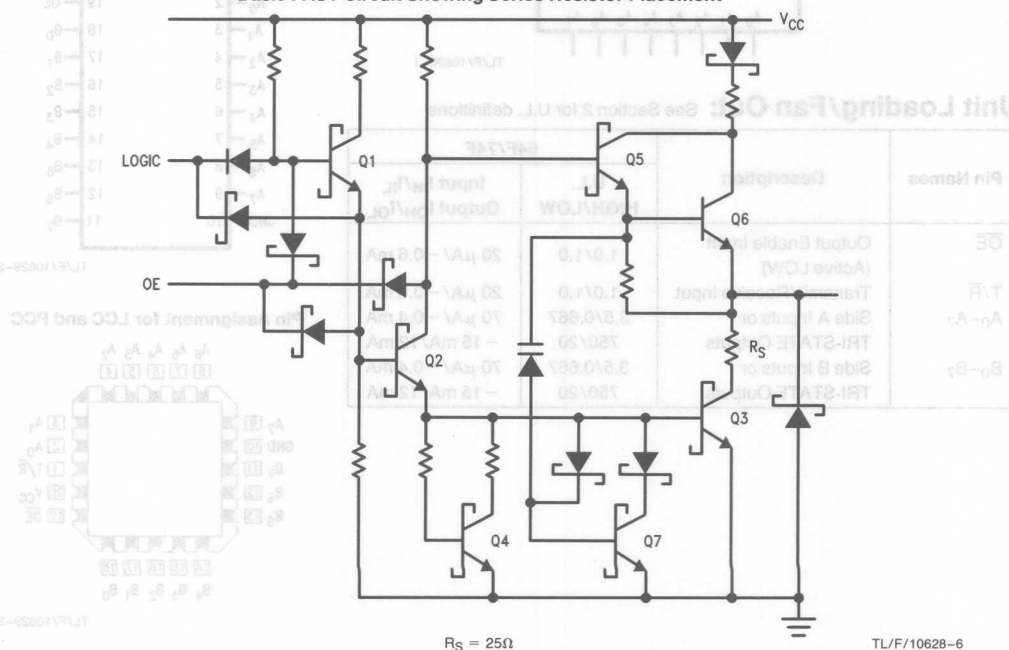
Free Air Ambient Temperature	−55°C to +125°C
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA (Non I/O Pins)
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>	2.0 2.0		V	Min	I <sub>OH</sub> = −12 mA (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OH</sub> = −15 mA (A <sub>n</sub> , B <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage			0.5 0.75	V	Min	I <sub>OL</sub> = 1.0 mA (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OL</sub> = 12 mA (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V (Non I/O Pins)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V (Non I/O Pins)
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)	54F 74F		1.0 0.5	mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V (Non I/O Pins)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			−650	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current		−100	−225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current ('F2620)			82	mA	Max	V <sub>O</sub> = HIGH, V <sub>IN</sub> = 0.2V
I <sub>CCL</sub>	Power Supply Current ('F2620)			82	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current ('F2620)			95	mA	Max	V <sub>O</sub> = HIGH Z
I <sub>CCH</sub>	Power Supply Current ('F2623)			82	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current ('F2623)			82	mA	Max	V <sub>O</sub> = LOW, V <sub>IN</sub> = 0.2V
I <sub>CCZ</sub>	Power Supply Current ('F2623)			95	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay A Input to B Output ('F2620)	2.5 3.0		7.5 8.0			2.0 3.0	8.0 8.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay B Input to A Output ('F2620)	2.5 3.0		7.5 8.0			2.0 3.0	8.0 8.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay A Input to B Output ('F2623)	1.5 2.5		6.5 7.5			1.5 2.5	7.5 8.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay B Input to A Output ('F2623)	1.5 2.5		6.5 7.5			1.5 2.5	7.5 8.0	ns	2-3
$t_{PZH}$ $t_{PZL}$	Enable Time $\overline{\text{G}}\text{BA Input to A Output}$	2.0 2.5		7.0 8.0			2.0 2.0	8.0 8.5	ns	2-5
$t_{PHZ}$ $t_{PLZ}$	Disable Time $\overline{\text{G}}\text{BA Input to A Output}$	1.5 1.0		6.5 5.5			1.5 1.0	7.5 5.5		
$t_{PZH}$ $t_{PZL}$	Enable Time GAB Input to B Output ('F2620)	2.0 3.0		7.5 8.0			2.0 2.0	8.5 8.5	ns	2-5
$t_{PHZ}$ $t_{PLZ}$	Disable Time GAB Input to B Output ('F2620)	2.5 2.0		8.0 7.5			2.0 2.0	9.0 8.0		
$t_{PZH}$ $t_{PZL}$	Enable Time GAB Input to B Output ('F2623)	2.0 2.5		7.5 8.0			2.0 2.0	8.5 8.5	ns	2-5
$t_{PHZ}$ $t_{PLZ}$	Disable Time GAB Input to B Output ('F2623)	2.0 2.0		8.0 8.0			2.0 2.0	9.0 8.0		

**Basic FAST Circuit Showing Series Resistor Placement**



# 54F/74F2640 • 54F/74F2643 • 54F/74F2645 Octal Bus Transceiver with 25Ω Series Resistors in the Outputs

## General Description

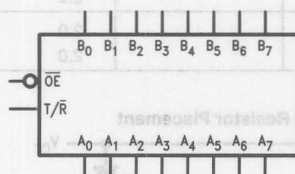
These devices are octal bus transceivers designed for asynchronous two-way data flow between the A and B busses. These devices are functionally equivalent to the 'F640, 'F643, and 'F645. The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors. Both busses are capable of sinking 12 mA, sourcing 15 mA, have TRI-STATE outputs, and a common output enable pin. The direction of data flow is determined by the transmit/receive (T/R) input. The 'F2640 is an inverting version of the 'F2645. The 'F2643 has a noninverting A bus and an inverting B bus. The 'F2645 is a low power version of the 'F245 with 25Ω series resistors in the outputs.

## Features

- 25Ω series resistors in the outputs eliminates the need for external resistors
- Designed for asynchronous two-way data flow between busses
- Outputs sink 12 mA and source 15 mA
- Transmit/receive (T/R) input controls the direction of data flow
- Guaranteed 4000V minimum ESD protection
- 'F2645 is a low power version of the 'F245 with 25Ω series resistors in the outputs
- 'F2640 is an inverting option of the 'F2645
- 'F2643 has noninverting A bus and inverting B bus

**Ordering Code:** See Section 5

## Logic Symbol



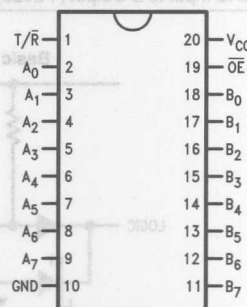
TL/F/10629-1

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A / -0.6 mA
T/ $\overline{R}$	Transmit/Receive Input	1.0/1.0	20 $\mu$ A / -0.6 mA
A <sub>0</sub> -A <sub>7</sub>	Side A Inputs or TRI-STATE Outputs	3.5/0.667	70 $\mu$ A / -0.4 mA -15 mA/12 mA
B <sub>0</sub> -B <sub>7</sub>	Side B Inputs or TRI-STATE Outputs	3.5/0.667	70 $\mu$ A / -0.4 mA -15 mA/12 mA

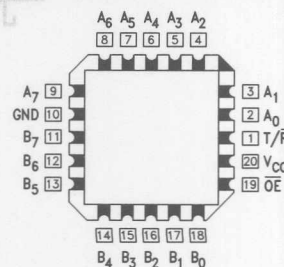
## Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak



TL/F/10629-2

Pin Assignment for LCC and PCC



TL/F/10629-3

## Functional Description

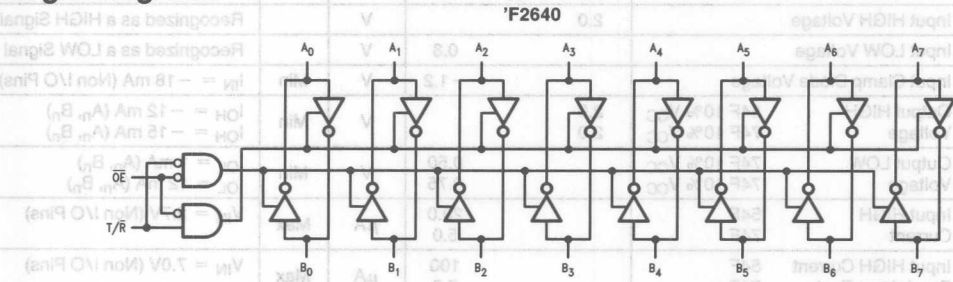
The output enable ( $\overline{OE}$ ) is active LOW. If the device is disabled ( $\overline{OE}$  HIGH), the outputs are in the high impedance state. The transmit/receive input ( $T/\overline{R}$ ) controls whether data is transmitted from the A bus to the B bus or from the B bus to the A bus. When  $T/\overline{R}$  is LOW, B data is sent to the A bus. If  $T/\overline{R}$  is HIGH, A data is sent to the B bus.

## Function Table

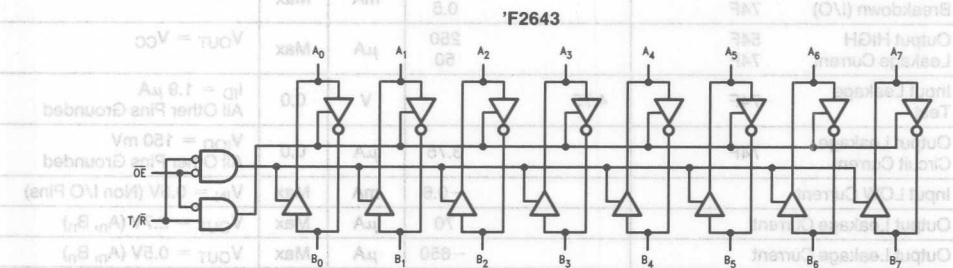
Inputs		Outputs		
$\overline{OE}$	$T/\overline{R}$	'F2640	'F2643	'F2645
L	L	Bus B data to Bus A	Bus B data to Bus A	Bus B data to Bus A
L	H	Bus A data to Bus B	Bus A data to Bus B	Bus A data to Bus B
H	X	Z	Z	Z

H = High voltage level  
L = Low voltage level  
X = Don't care  
Z = High-impedance state

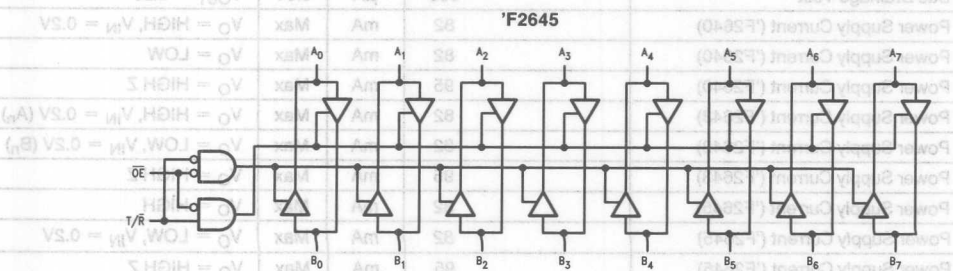
## Logic Diagrams



TL/F/10629-4



TL/F/10629-5



TL/F/10629-6

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output	−0.5V to +5.5V
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

ESD Last Passing Voltage (Min) 4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	−55°C to +125°C
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA (Non I/O Pins)
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>	2.0 2.0		V	Min	I <sub>OH</sub> = −12 mA (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OH</sub> = −15 mA (A <sub>n</sub> , B <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.50 0.75	V	Min	I <sub>OL</sub> = 1 mA (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OL</sub> = 12 mA (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V (Non I/O Pins)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V (Non I/O Pins)
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)	54F 74F		1.0 0.5	mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V (Non I/O Pins)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			−650	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current		−100	−225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25
I <sub>CCH</sub>	Power Supply Current ('F2640)			82	mA	Max	V <sub>O</sub> = HIGH, V <sub>IN</sub> = 0.2V
I <sub>CCL</sub>	Power Supply Current ('F2640)			82	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current ('F2640)			95	mA	Max	V <sub>O</sub> = HIGH Z
I <sub>CCH</sub>	Power Supply Current ('F2643)			82	mA	Max	V <sub>O</sub> = HIGH, V <sub>IN</sub> = 0.2V (A <sub>n</sub> )
I <sub>CCL</sub>	Power Supply Current ('F2643)			82	mA	Max	V <sub>O</sub> = LOW, V <sub>IN</sub> = 0.2V (B <sub>n</sub> )
I <sub>CCZ</sub>	Power Supply Current ('F2643)			95	mA	Max	V <sub>O</sub> = HIGH Z
I <sub>CCH</sub>	Power Supply Current ('F2645)			82	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current ('F2645)			82	mA	Max	V <sub>O</sub> = LOW, V <sub>IN</sub> = 0.2V
I <sub>CCZ</sub>	Power Supply Current ('F2645)			95	mA	Max	V <sub>O</sub> = HIGH Z

**'F2640 AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay A Input to B Output	2.5		7.5			2.0	8.0	ns	2-3
		2.5		7.5			2.5	7.5		
$t_{PLH}$ $t_{PHL}$	Propagation Delay B Input to A Output	2.5		7.5			2.0	8.0	ns	2-3
		2.5		7.5			2.5	7.5		
$t_{PZH}$ $t_{PZL}$	Enable Time $\overline{OE}$ Input to A Output	2.5		7.5			2.0	9.0	ns	2-5
		2.5		8.0			2.0	8.5		
$t_{PHZ}$ $t_{PLZ}$	Disable Time $\overline{OE}$ Input to A Output	1.5		7.0			1.0	7.5	ns	2-5
		1.5		6.0			1.5	6.0		
$t_{PZH}$ $t_{PZL}$	Enable Time $\overline{OE}$ Input to B Output	2.5		7.5			2.0	9.0	ns	2-5
		2.5		8.0			2.0	8.5		
$t_{PHZ}$ $t_{PLZ}$	Disable Time $\overline{OE}$ Input to B Output	1.5		6.5			1.0	7.5	ns	2-5
		1.5		6.0			1.5	6.0		

**'F2643 AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

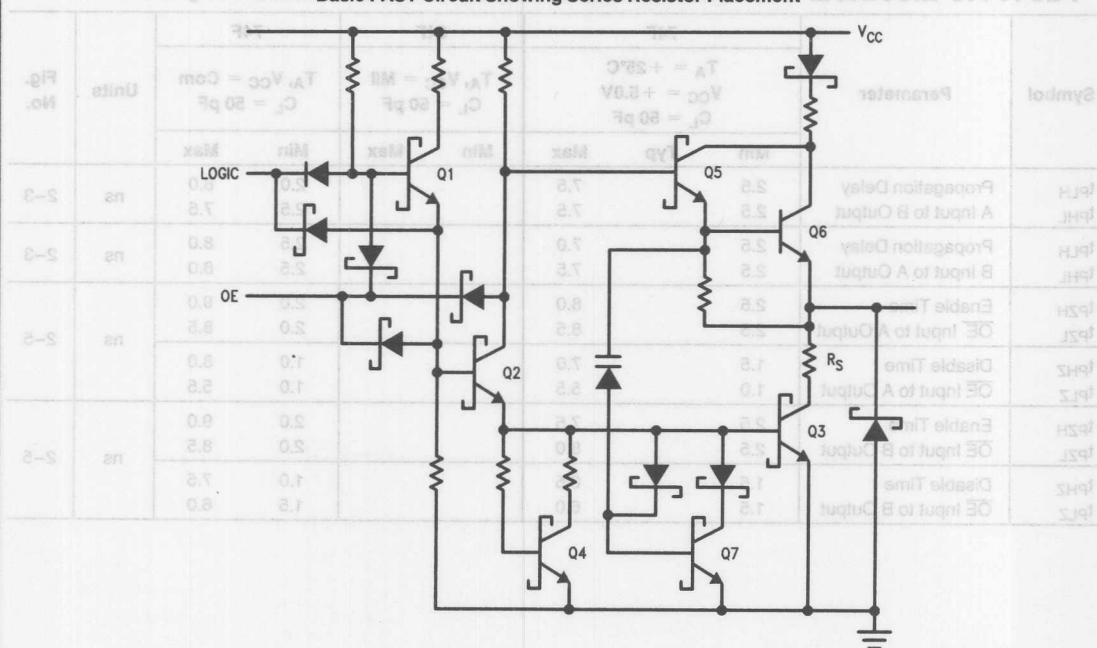
Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay A Input to B Output	2.5		7.5			2.0	8.0	ns	2-3
		2.5		7.5			2.5	7.5		
$t_{PLH}$ $t_{PHL}$	Propagation Delay B Input to A Output	2.5		7.0			2.5	8.0	ns	2-3
		2.5		7.5			2.5	8.0		
$t_{PZH}$ $t_{PZL}$	Enable Time $\overline{OE}$ Input to A Output	2.5		8.0			2.0	9.0	ns	2-5
		2.5		8.5			2.0	8.5		
$t_{PHZ}$ $t_{PLZ}$	Disable Time $\overline{OE}$ Input to A Output	1.5		7.0			1.0	8.0	ns	2-5
		1.0		5.5			1.0	5.5		
$t_{PZH}$ $t_{PZL}$	Enable Time $\overline{OE}$ Input to B Output	2.5		7.5			2.0	9.0	ns	2-5
		2.5		8.0			2.0	8.5		
$t_{PHZ}$ $t_{PLZ}$	Disable Time $\overline{OE}$ Input to B Output	1.5		6.5			1.0	7.5	ns	2-5
		1.5		6.0			1.5	6.0		



**'F2645 AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay A Input to B Output	1.5 2.5		6.0 7.5			1.5 2.5	7.0 8.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay B Input to A Output	1.5 2.5		6.0 7.5			1.5 2.5	7.0 8.0	ns	2-3
$t_{pZH}$ $t_{pZL}$	Enable Time $\overline{\text{OE}}$ Input to A Output	2.5 2.5		8.0 8.5			2.0 2.0	9.0 8.5	ns	2-5
$t_{PHZ}$ $t_{PLZ}$	Disable Time $\overline{\text{OE}}$ Input to A Output	1.5 1.0		7.0 5.5			1.0 1.0	8.0 5.5		
$t_{pZH}$ $t_{pZL}$	Enable Time $\overline{\text{OE}}$ Input to B Output	2.5 2.5		7.5 8.5			2.0 2.5	9.5 9.0	ns	2-5
$t_{PHZ}$ $t_{PLZ}$	Disable Time $\overline{\text{OE}}$ Input to B Output	1.5 1.0		6.5 6.5			1.0 1.0	7.5 6.5		

Basic FAST Circuit Showing Series Resistor Placement



TL/F/10629-7

# 29F52•29F53

## 8-Bit Registered Transceiver

### General Description

The 29F52 and 29F53 are 8-bit registered transceivers. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and TRI-STATE® output enable signals are provided for each register. The A<sub>0</sub>–A<sub>7</sub> output pins are guaranteed to sink 24 mA (20 mA mil.) while the B<sub>0</sub>–B<sub>7</sub> output pins are designed for 64 mA.

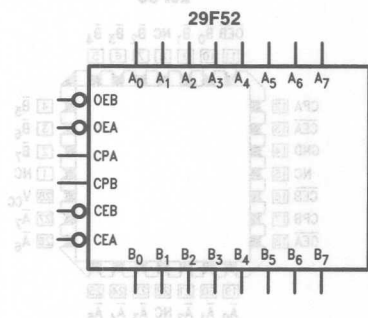
The 29F53 is an inverting option of the 29F52. Both transceivers are AMD Am2952/2953 functional equivalents.

### Features

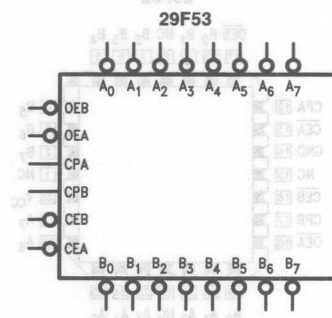
- 8-bit registered transceivers
- Separate clock, clock enable and TRI-STATE output enable provided for each register
- AMD Am2952/2953 functional equivalents
- Both inverting and non-inverting options available
- 24-Pin slimline package

**Ordering Code:** See Section 5

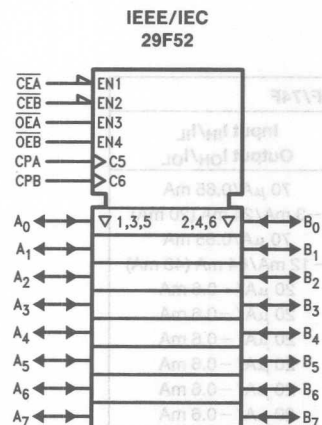
### Logic Symbols



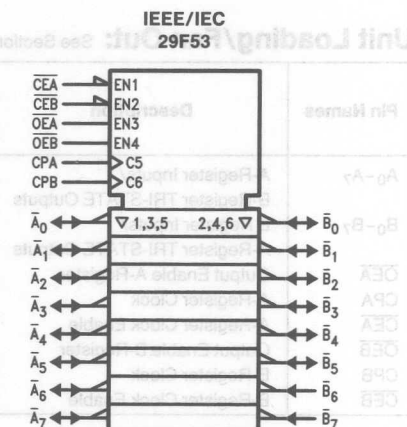
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TL/F/9606-7



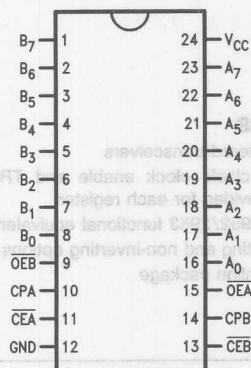
TL/F/9606-4



TL/F/9606-5

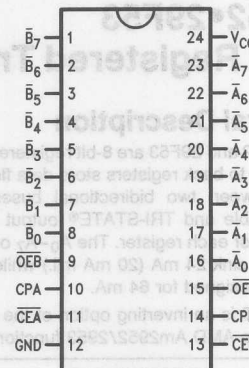
## Connection Diagrams (Continued)

**Pin Assignment  
for DIP, SOIC and Flatpak  
29F52**



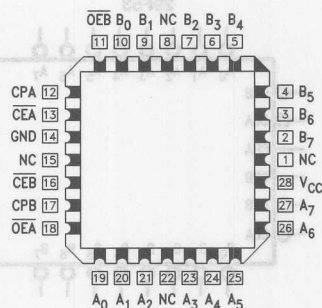
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**Pin Assignment  
for DIP, SOIC and Flatpak  
29F53**



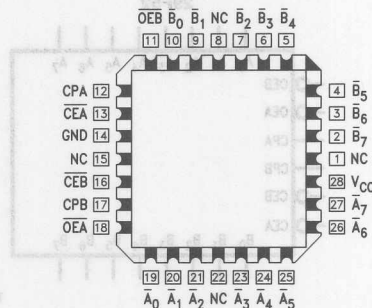
TL/F/9606-8

**Pin Assignment  
for LCC and PCC  
29F52**



TL/F/9606-3

**Pin Assignment  
for LCC and PCC  
29F53**



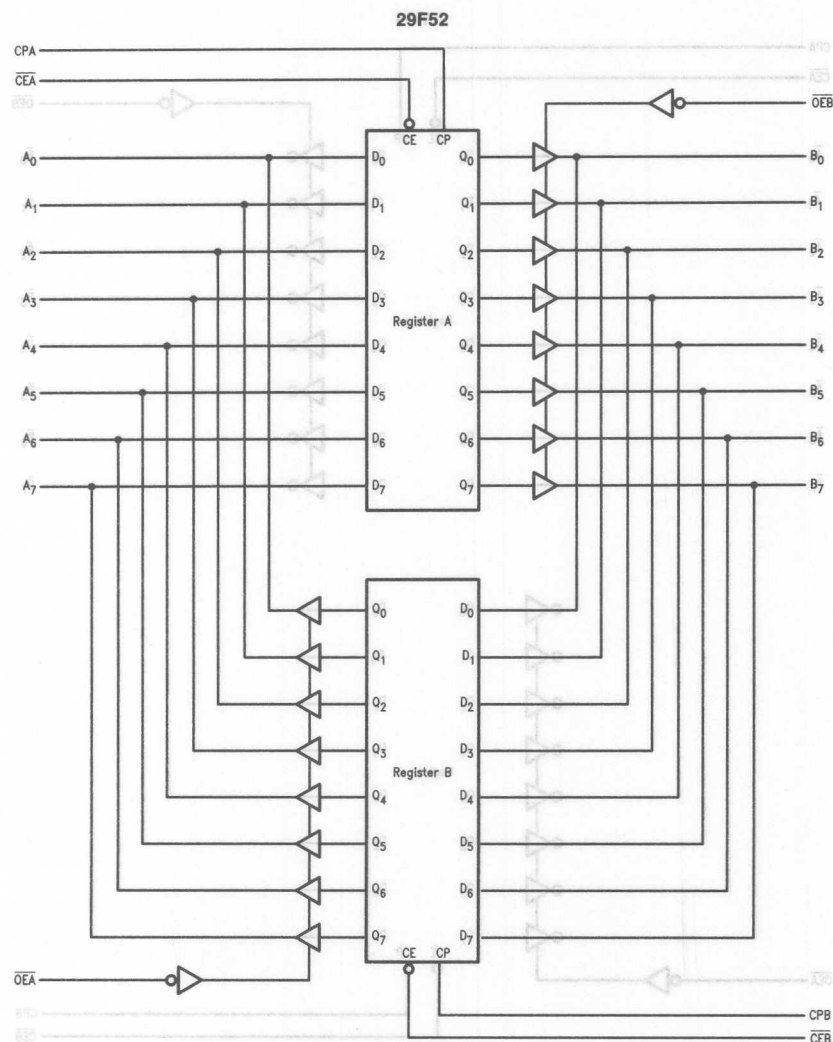
TL/F/9606-9

## Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_0-A_7$	A-Register Inputs/ B-Register TRI-STATE Outputs	3.5/1.083	70 $\mu$ A/0.65 mA
$B_0-B_7$	B-Register Inputs/ A-Register TRI-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)
$\overline{OEA}$	Output Enable A-Register	3.5/1.083	70 $\mu$ A/0.65 mA
CPA	A-Register Clock	600/106.6 (80)	-12 mA/64 mA (48 mA)
CEA	A-Register Clock Enable	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{OEB}$	Output Enable B-Register	1.0/1.0	20 $\mu$ A/-0.6 mA
CPB	B-Register Clock	1.0/1.0	20 $\mu$ A/-0.6 mA
CEB	B-Register Clock Enable	1.0/1.0	20 $\mu$ A/-0.6 mA

# Block Diagrams

Block Diagrams (Continued)



TL/F/9606-6

TL/F/9606-6

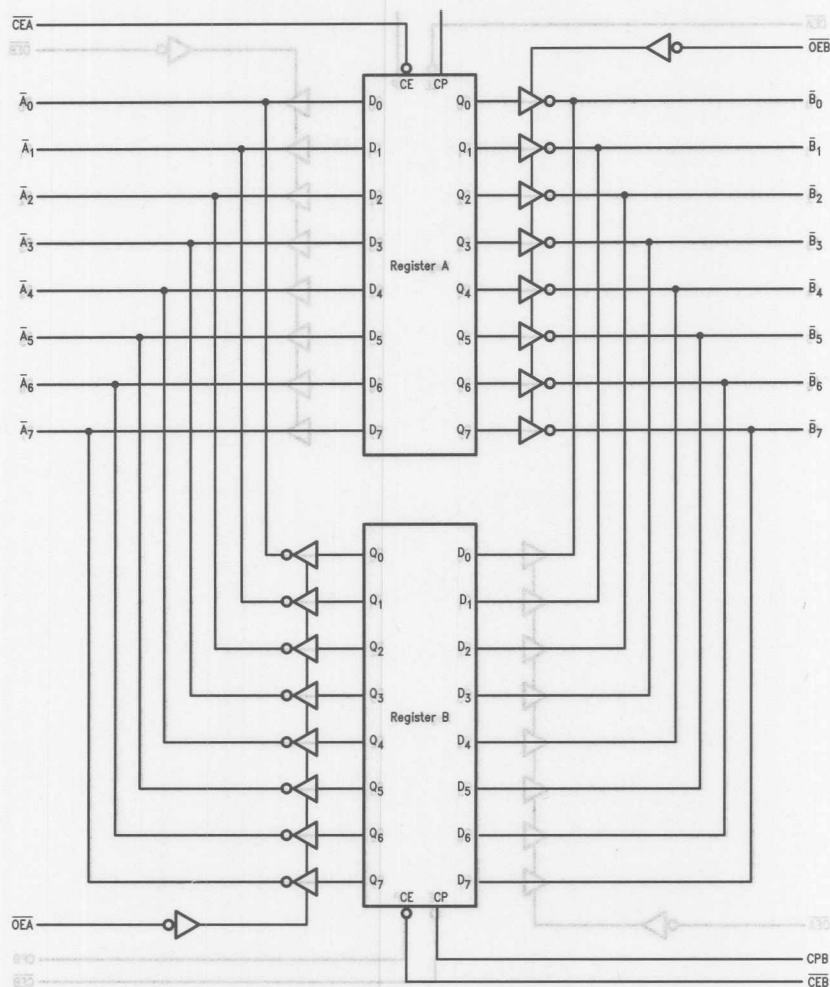
Register Function Table (Applies to A or B Register)

Function	Internal Q	Inputs		
		CE	CP	D
Hold Data	NC	H	X	X
Load Data	L	L	~	L
	H	L	~	H

Output Control

Function	Internal Q	Y-Output	
		29F52	29F53
Disable Outputs	X	Z	Z
Enable Outputs	L	L	L
	H	L	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Indeterminate  
 Z = HIGH Impedance  
 ~ = LOW-to-HIGH Transition  
 NC = No Change



0-30000000

TL/F/9606-10

Output Control

OE	Internal Q	Y-Output		Function
		29F52	29F53	
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = HIGH Impedance

/ = LOW-to-HIGH Transition

NC = No Change

Register Function Table (Applies to A or B Register)

Inputs			Internal Q	Function
D	CP	CE		
X	X	H	NC	Hold Data
L	/	L	L	Load Data
H	/	L	H	

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	–0.5V to V <sub>CC</sub>
Standard Output TRI-STATE Output	–0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	–55°C to +125°C
Military	–55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			–1.2	V	Min	I <sub>IN</sub> = –18 mA (Non I/O Pins)
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = –1 mA (A <sub>n</sub> )
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = –3 mA (A <sub>n</sub> , B <sub>n</sub> )
		54F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = –12 mA (B <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.5			Min	I <sub>OH</sub> = –1 mA (A <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = –3 mA (A <sub>n</sub> , B <sub>n</sub> )
		74F 10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = –15 mA (B <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	74F 5% V <sub>CC</sub>	2.7				I <sub>OL</sub> = –1 mA (A <sub>n</sub> )
		74F 5% V <sub>CC</sub>	2.7				I <sub>OL</sub> = –3 mA (A <sub>n</sub> , B <sub>n</sub> )
		54F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA (A <sub>n</sub> )
		54F 10% V <sub>CC</sub>		0.55		Min	I <sub>OL</sub> = 48 mA (B <sub>n</sub> )
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA (A <sub>n</sub> )
		74F 10% V <sub>CC</sub>		0.55			I <sub>OL</sub> = 64 mA (B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current			20	μA	Max	V <sub>IN</sub> = 2.7V (Non-I/O Pins)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			100	μA	Max	V <sub>IN</sub> = 7.0V (Non-I/O Pins)
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)			1.0	mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub>	Input LOW Current			–0.6	mA	Max	V <sub>IN</sub> = 0.5V (Non-I/O Pins)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			–650	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current	–60	–150	–225	mA	Max	V <sub>OUT</sub> = 0V (A <sub>n</sub> ) V <sub>OUT</sub> = 0V (B <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub> (A <sub>n</sub> , B <sub>n</sub> )
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CCH</sub>	Power Supply Current		130	190	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			190	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current			190	mA	Max	V <sub>O</sub> = HIGH Z



**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	3.0	5.5	7.5			2.5	8.5	ns	2-3
$t_{PHL}$	CPA or CPB to $A_n$ or $B_n$	4.0	7.0	9.0			3.5	10.0		
$t_{PZH}$	Output Enable Time	2.5	5.5	7.5			2.0	8.5	ns	2-5
$t_{PZL}$	$\overline{OE}A$ or $\overline{OE}B$ to $A_n$ or $B_n$	3.5	7.0	9.5			3.0	10.5		
$t_{PHZ}$	Output Disable Time	2.5	6.5	9.0			2.0	10.0	ns	2-5
$t_{PLZ}$	$\overline{OE}A$ or $\overline{OE}B$ to $A_n$ or $B_n$	2.5	5.5	7.5			2.0	8.5		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	4.0				4.5		ns	2-6
$t_s(\text{L})$	$A_n$ or $B_n$ to CPA or CPB	4.0				4.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0				2.5		ns	2-6
$t_h(\text{L})$	$A_n$ or $B_n$ to CPA or CPB	2.0				2.5			
$t_s(\text{H})$	Setup Time, HIGH or LOW	1.0				1.5		ns	2-6
$t_s(\text{L})$	$\overline{\text{CEA}}$ or $\overline{\text{CEB}}$ to CPA or CPB	4.0				4.5			
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0				2.5		ns	2-6
$t_h(\text{L})$	$\overline{\text{CEA}}$ or $\overline{\text{CEB}}$ to CPA or CPB	2.0				2.5			
$t_w(\text{H})$	Pulse Width, HIGH or LOW	3.0				3.5		ns	2-4
$t_w(\text{L})$	CPA or CPB	3.0				3.5			



29F68

## Dynamic RAM Controller

### General Description

The 29F68 is a high-performance memory controller, replacing many SSI and MSI devices by grouping several unique functions. It provides two 9-bit address latches and two 9-bit counters for row and column address generation during refresh. A 2-bit bank select latch for row and column address generation during refresh, and a 2-bit bank select latch for the two high order address bits are provided to select one of the four RAS and CAS outputs.

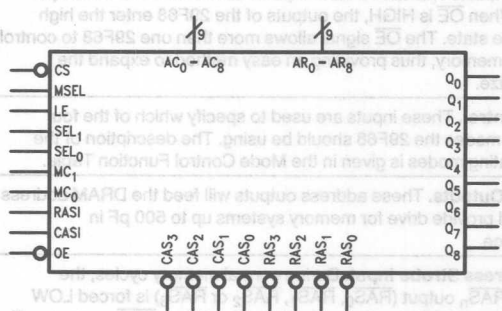
The 29F68 is functionally equivalent to AMD's Am2968 and Motorola's MC74F2968.

### Features

- High-performance memory controller
- Replaces many SSI and MSI devices by grouping several unique functions
- Functionally equivalent to AMD's Am2968 and Motorola's MC74F2968
- Provides control for 16K, 64K, or 256K dynamic RAM systems
- Outputs directly drive up to 88 DRAMs
- Highest order two address bits select one of four banks of RAMs
- Chip Select for easy expansion
- Provides memory refresh with error correction mode

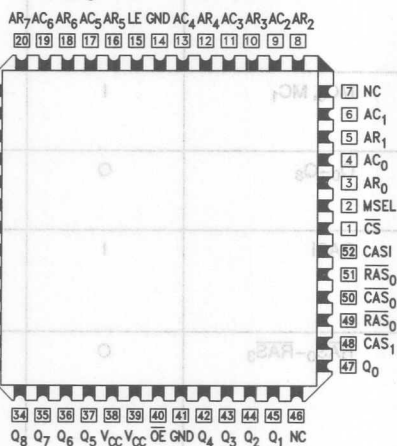
### Ordering Code: See Section 5

### Logic Symbol



### Connection Diagram

#### Pin Assignment for LCC and PCC



## Pin Description

Name	I/O	Description
AR <sub>0</sub> –AR <sub>8</sub> AC <sub>0</sub> –AC <sub>8</sub>	I	<b>Address Inputs.</b> AR <sub>0</sub> –AR <sub>8</sub> are latched in as the 9-bit Row Address for the RAM. These inputs drive Q <sub>0</sub> –Q <sub>8</sub> when the 29F68 is in the Read/Write mode and MSEL is LOW. AC <sub>0</sub> –AC <sub>8</sub> are latched in as the Column Address, and will drive Q <sub>0</sub> –Q <sub>8</sub> when MSEL is HIGH and the 29F68 is in the Read/Write mode. The addresses are latched with the Latch Enable (LE) signal.
SEL <sub>0</sub> –SEL <sub>1</sub>	I	<b>Bank Select.</b> These two inputs are normally the two higher order address bits, and are used in the Read/Write mode to select which bank of memory will be receiving the RAS <sub>n</sub> and CAS <sub>n</sub> signals after RAS <sub>i</sub> and CAS <sub>i</sub> go HIGH.
LE	I	<b>Latch Enable.</b> This active-HIGH input causes the Row, Column and Bank Select latches to become transparent, allowing the latches to accept new input data. A LOW input on LE latches the input data, assuming it meets the setup and hold time requirements.
MSEL	I	<b>Multiplexer Select.</b> This input determines whether the Row or Column Address will be sent to the memory address inputs. When MSEL is HIGH the Column Address is selected, while the Row Address is selected when MSEL is LOW. The address may come from either the address latch or refresh address counter depending on MC <sub>0</sub> , MC <sub>1</sub> .
$\overline{\text{CS}}$	I	<b>Chip Select.</b> This active-LOW input is used to enable the 29F68. When $\overline{\text{CS}}$ is active, the 29F68 operates normally in all four modes. When $\overline{\text{CS}}$ goes HIGH, the device will not enter the Read/Write mode. This allows other devices to access the same memory that the 29F68 is controlling (e.g., DMA controller).
$\overline{\text{OE}}$	I	<b>Output Enable.</b> This active-LOW input enables/disables the output signals. When $\overline{\text{OE}}$ is HIGH, the outputs of the 29F68 enter the high impedance state. The $\overline{\text{OE}}$ signal allows more than one 29F68 to control the same memory, thus providing an easy method to expand the memory size.
MC <sub>0</sub> , MC <sub>1</sub>	I	<b>Mode Control.</b> These inputs are used to specify which of the four operating modes the 29F68 should be using. The description of the four operating modes is given in the Mode Control Function Table.
Q <sub>0</sub> –Q <sub>8</sub>	O	<b>Address Outputs.</b> These address outputs will feed the DRAM address inputs and provide drive for memory systems up to 500 pF in capacitance.
RAS <sub>i</sub>	I	<b>Row Address Strobe Input.</b> During normal memory cycles, the decoded RAS <sub>n</sub> output (RAS <sub>0</sub> , RAS <sub>1</sub> , RAS <sub>2</sub> or RAS <sub>3</sub> ) is forced LOW after receipt of RAS <sub>i</sub> . In either refresh mode, all four RAS <sub>n</sub> outputs will go LOW following RAS <sub>i</sub> going HIGH.
$\overline{\text{RAS}}_0$ – $\overline{\text{RAS}}_3$	O	<b>Row Address Strobe.</b> Each one of the Row Address Strobe outputs provides a $\overline{\text{RAS}}_n$ signal to one of the four banks of dynamic memory. Each will go LOW only when selected by SEL <sub>0</sub> and SEL <sub>1</sub> and only after RAS <sub>i</sub> goes HIGH. All four go LOW in response to RAS <sub>i</sub> in either of the Refresh modes.
CAS <sub>i</sub>	I	<b>Column Address Strobe Input.</b> This input going active will cause the selected CAS <sub>n</sub> output to be forced LOW.
$\overline{\text{CAS}}_0$ – $\overline{\text{CAS}}_3$	O	<b>Column Address Strobe.</b> During normal Read/Write cycles the two select bits (SEL <sub>0</sub> , SEL <sub>1</sub> ) determine which $\overline{\text{CAS}}_n$ output will go active following CAS <sub>i</sub> going HIGH. When memory error correction is performed, only the $\overline{\text{CAS}}_n$ signal selected by CNTR <sub>0</sub> and CNTR <sub>1</sub> will be active. For non-error correction cycles, all four $\overline{\text{CAS}}_n$ outputs remain HIGH.

## Functional Description

The 29F68 is designed to be used with 16k, 64k, or 256k dynamic RAMs and is functionally equivalent to AMD's AM2968. The 29F68 provides row/column address multiplexing, refresh address generation and bank selection for up to four banks of RAMs.

Twenty (20) address bits ( $AR_0-AR_8$ ,  $AC_0-AC_8$ , and bank select addresses  $SEL_0$  and  $SEL_1$ ) are presented to the controller. These addresses are latched by a 20-bit latch. A 20-bit counter generates the refresh address.

A 9-bit multiplexer selects the output address between the input row address, column address, refresh counter row address, column address, or zero (clear). Four RAS and four CAS outputs select the appropriate bank of RAMs and strobe in the row and column addresses.

It should be noted that the counters are cleared ( $MC_0$ ,  $MC_1 = 1,1$ ) on the next RAS<sub>i</sub> transition, but the Q outputs are asynchronously cleared through the multiplexer.

Mode Control Function Table

$MC_1$	$MC_0$	Operating Mode
0	0	<b>Refresh without Error Correction.</b> Refresh cycles are performed with only the Row Counter being used to generate addresses. In this mode, all four $RAS_n$ outputs are active while the four $CAS_n$ signals are kept HIGH.
0	1	<b>Refresh with Error Correction/Initialize</b> —During this mode, refresh cycles are done with both the Row and Column counters generating the addresses. MSEL is used to select between the Row and Column counter. All four $RAS_n$ outputs go active in response to RAS <sub>i</sub> , while only one $CAS_n$ output goes LOW in response to CAS <sub>i</sub> . The Bank Counter keeps track of which $CAS_n$ output will go active. This mode is also used on system power-up so that the memory can be written with a known data pattern.
1	0	<b>Read/Write</b> — This mode is used to perform Read/Write cycles. Both the Row and Column addresses are latched and multiplexed to the address output lines using MSEL; $SEL_0$ and $SEL_1$ are decoded to determine which $RAS_n$ and $CAS_n$ will be active.
1	1	<b>Clear Refresh Counter</b> —This mode will clear the three refresh counters (Row, Column, and Bank) on the HIGH-to-LOW transition of RAS <sub>i</sub> , putting them at the start of the refresh sequence. In this mode, all four $RAS_n$ are driven LOW upon receipt of RAS <sub>i</sub> so that DRAM wake-up cycles may be performed. This mode also asynchronously clears the $Q_n$ outputs.

Address Output Function Table

$CS$	$MC_1$	$MC_0$	MSEL	Mode	MUX Output
L	L	L	X	Refresh without Error Correction	Row Counter Address
			H	Refresh with Error Correction	Column Counter Address
			L		Row Counter Address
	H	L	H	Read/Write	Column Address Latch
			L		Row Address Latch
	H	H	X	Clear Refresh Counter	Zero
H	L	L	X	Refresh without Error Correction	Row Counter Address
			H	Refresh with Error Correction	Column Counter Address
			L		Row Counter Address
	H	L	X	Read/Write	Zero
			X		Zero
	H	H	X	Clear Refresh Counter	Zero

RAS Output Function Table

RAS <sub>I</sub>	$\overline{CS}$	MC <sub>1</sub>	MC <sub>0</sub>	SEL <sub>1</sub>	SEL <sub>0</sub>	Mode	RAS <sub>0</sub>	RAS <sub>1</sub>	RAS <sub>2</sub>	RAS <sub>3</sub>
L	X	X	X	X	X	Non-refresh	H	H	H	H
H	L	L	L	X	X	Refresh without Scrubbing	L	L	L	L
		L	H	X	X	Refresh with Scrubbing	L	L	L	L
		H	L	L	L	Read/Write	L	H	H	H
				L	H		H	L	H	H
				H	L		H	H	L	H
				H	H		H	H	H	L
	H	H	X	X	X	Clear Refresh Counter	L	L	L	L
	L	L	X	X	X	Refresh without Error Correction	L	L	L	L
	L	H	H			Refresh with Error Correction	L	L	L	L
	H	L				Read/Write	H	H	H	H
	H	H	H			Clear Refresh Counter	L	L	L	L

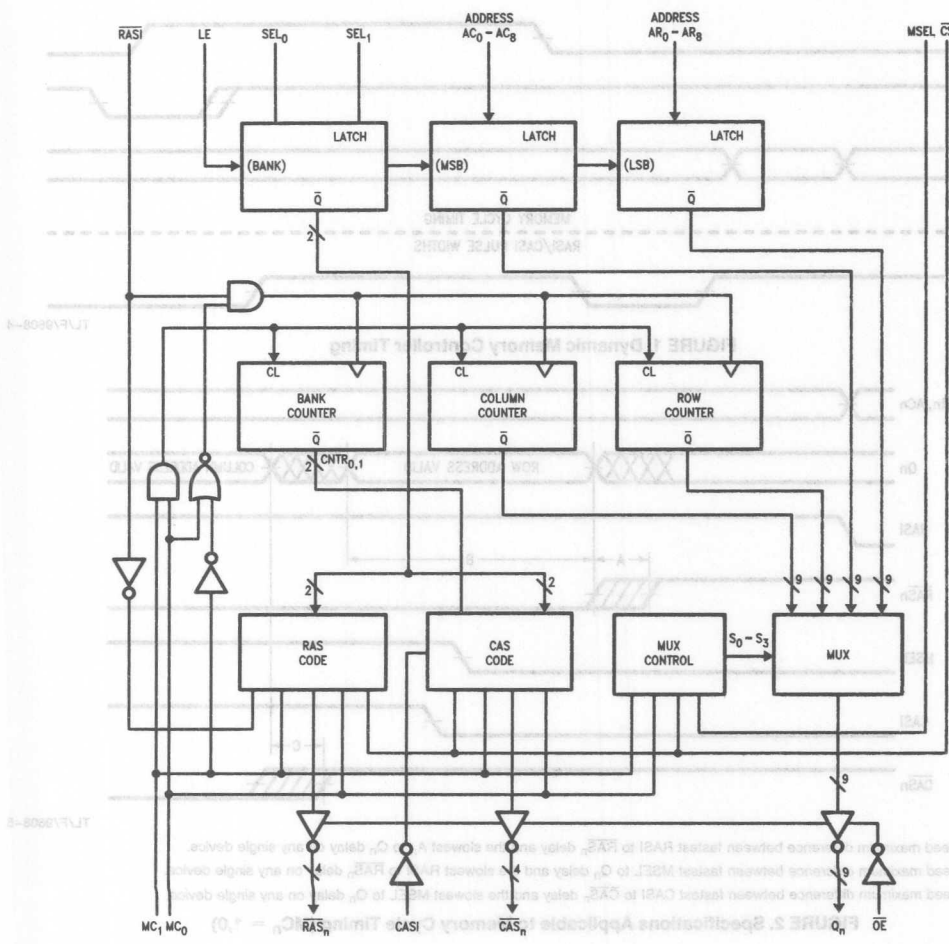
CAS Output Function Table

Inputs				Internal Counter		Inputs		Outputs				
CASI	CS	MC <sub>1</sub>	MC <sub>0</sub>	CNTR <sub>1</sub>	CNTR <sub>0</sub>	SEL <sub>1</sub>	SEL <sub>0</sub>	CAS <sub>0</sub>	CAS <sub>1</sub>	CAS <sub>2</sub>	CAS <sub>3</sub>	
H	L	L	L	X	X	X	X	H	H	H	H	
			L	L	X	X	L	H	H	H		
			L	H	L	L	H	L	H	H		
			H	L	H	L	H	L	H	H		
		H	L	X	X	L	L	L	H	H	H	
			L			L	H	H	L	H	H	
							H	L	H	H	L	
							H	H	H	H	L	
	H	H	H	X	X	X	X	H	H	H	H	
			L	X	X	X	X	H	H	H	H	
			L	L	L	X	X	L	H	H	H	
			L	H	L			H	L	H	H	
		H	L	H	L	L	H	H	H	L	H	
			H	H	H	H	H	H	H	H	L	
			H	L	X	X	X	X	H	H	H	H
			H	H								
L	X	X	X	X	X	X	H	H	H	H		

Unit Loading/Fan Out: See Section 2 for U.L. definitions

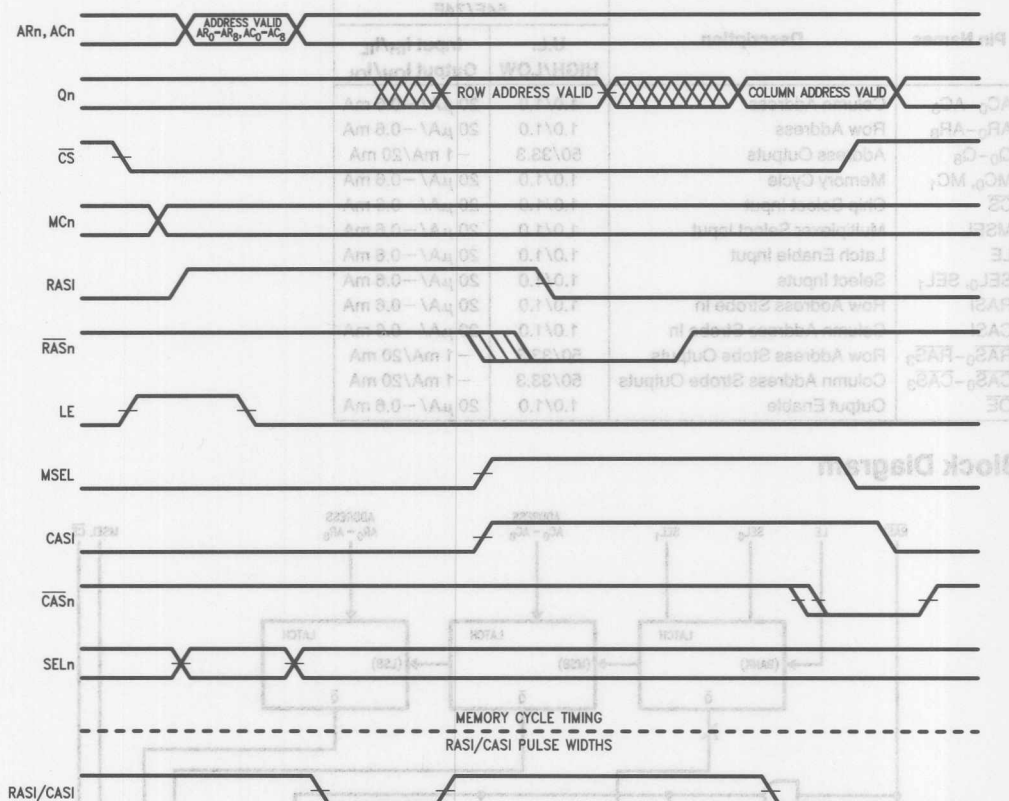
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
AC <sub>0</sub> –AC <sub>8</sub>	Column Address	1.0/1.0	20 $\mu$ A/–0.6 mA
AR <sub>0</sub> –AR <sub>8</sub>	Row Address	1.0/1.0	20 $\mu$ A/–0.6 mA
Q <sub>0</sub> –Q <sub>8</sub>	Address Outputs	50/33.3	–1 mA/20 mA
MC <sub>0</sub> , MC <sub>1</sub>	Memory Cycle	1.0/1.0	20 $\mu$ A/–0.6 mA
$\overline{CS}$	Chip Select Input	1.0/1.0	20 $\mu$ A/–0.6 mA
MSEL	Multiplexer Select Input	1.0/1.0	20 $\mu$ A/–0.6 mA
LE	Latch Enable Input	1.0/1.0	20 $\mu$ A/–0.6 mA
SEL <sub>0</sub> , SEL <sub>1</sub>	Select Inputs	1.0/1.0	20 $\mu$ A/–0.6 mA
RASI	Row Address Strobe In	1.0/1.0	20 $\mu$ A/–0.6 mA
CASI	Column Address Strobe In	1.0/1.0	20 $\mu$ A/–0.6 mA
RAS <sub>0</sub> –RAS <sub>3</sub>	Row Address Strobe Outputs	50/33.3	–1 mA/20 mA
CAS <sub>0</sub> –CAS <sub>3</sub>	Column Address Strobe Outputs	50/33.3	–1 mA/20 mA
OE	Output Enable	1.0/1.0	20 $\mu$ A/–0.6 mA

Block Diagram



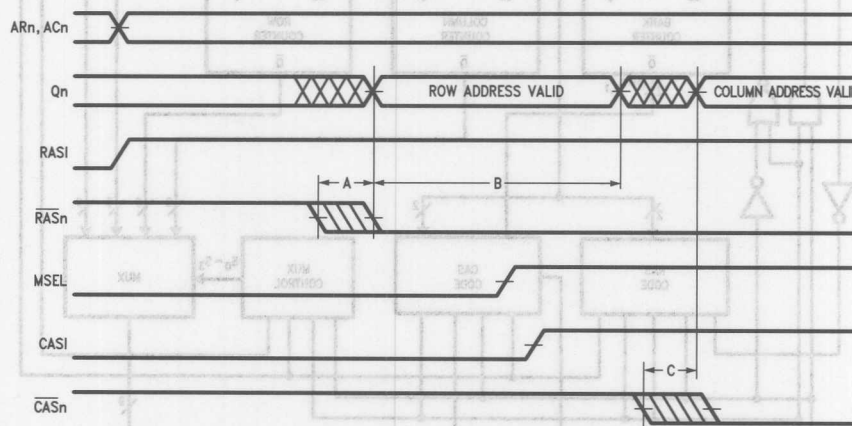


## Timing Waveforms



TL/F/9608-4

FIGURE 1. Dynamic Memory Controller Timing



TL/F/9608-5

**Note A:** Guaranteed maximum difference between fastest RASi to  $\overline{RAS}_n$  delay and the slowest  $A_n$  to  $Q_n$  delay on any single device.

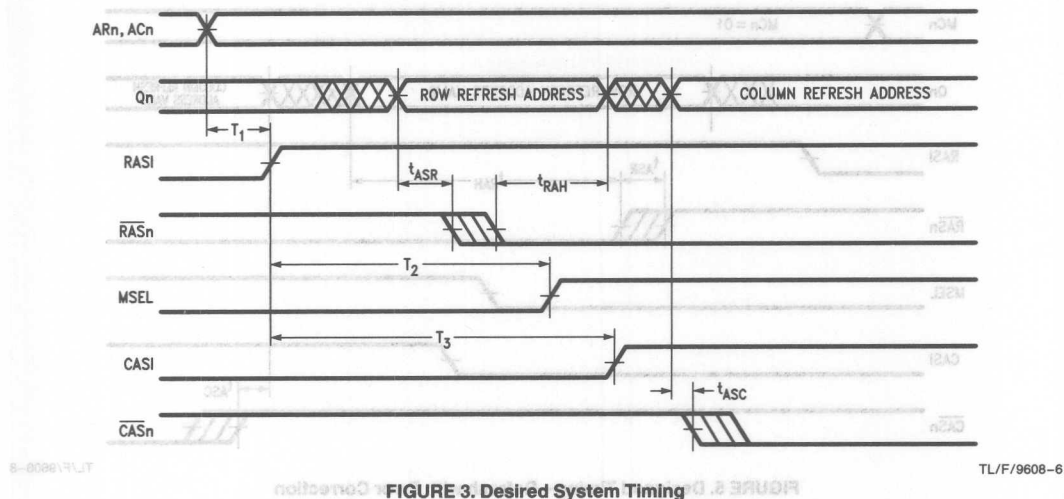
**Note B:** Guaranteed maximum difference between fastest MSEL to  $Q_n$  delay and the slowest RASi to  $\overline{RAS}_n$  delay on any single device.

**Note C:** Guaranteed maximum difference between fastest CASi to  $\overline{CAS}_n$  delay and the slowest MSEL to  $Q_n$  delay on any single device.

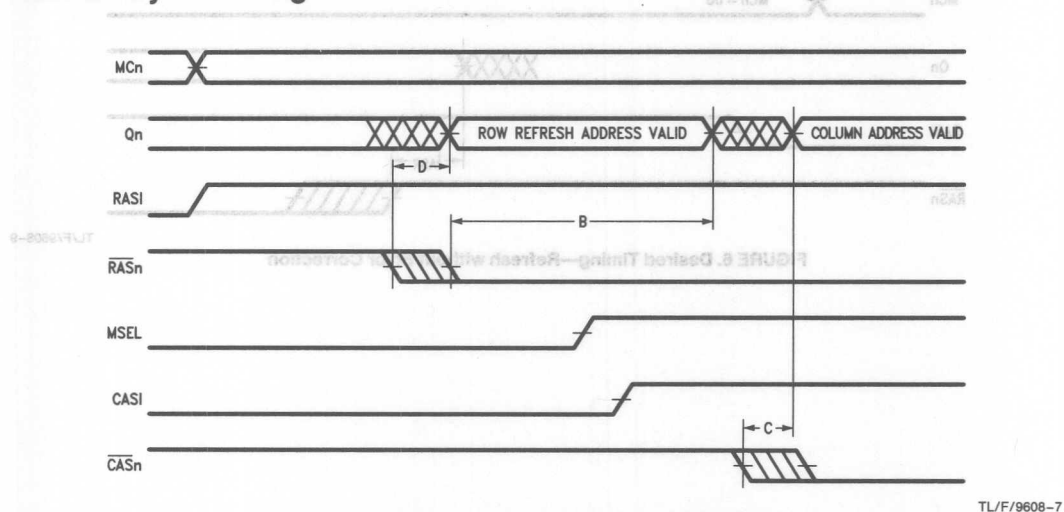
FIGURE 2. Specifications Applicable to Memory Cycle Timing ( $MC_n = 1,0$ )

## Timing Waveforms (Continued)

Refresh Cycle Timing (Continued)



## Refresh Cycle Timing



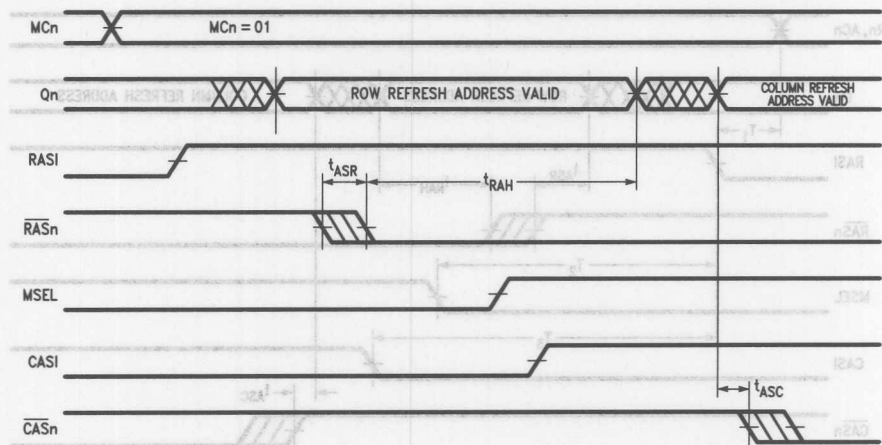
**Note B:** Guaranteed maximum difference between fastest MSEL to  $Q_n$  delay and the slowest RASi to  $\overline{RAS}_n$  delay on any single device.

**Note C:** Guaranteed maximum difference between fastest CASi to  $\overline{CAS}_n$  delay and the slowest MSEL to  $Q_n$  delay on any single device.

**Note D:** Guaranteed maximum difference between fastest RASi to  $\overline{RAS}_n$  delay and the slowest  $MC_n$  to  $Q_n$  delay on any single device.

## Refresh Cycle Timing (Continued)

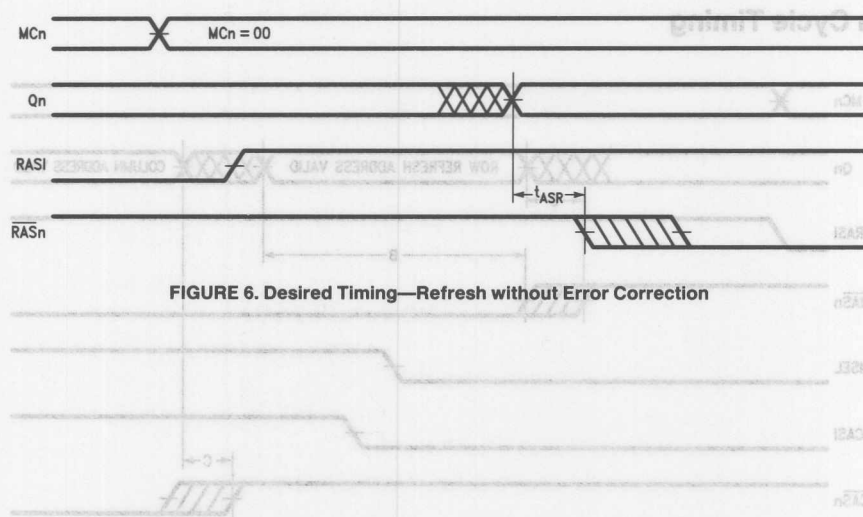
Timing Waveforms (Continued)



TL/F/9608-8

FIGURE 5. Designed Timing—Refresh with Error Correction

TL/F/9608-8



TL/F/9608-9

FIGURE 6. Desired Timing—Refresh without Error Correction

TL/F/9608-9

FIGURE 4. Specifications Applicable to Refresh Cycle Timing ( $MCn = 00, 01$ )

Note B: Guaranteed maximum difference between fastest  $MSEL$  to  $Qn$  delay and the slowest  $RASi$  to  $\overline{RASn}$  delay on any single device.

Note C: Guaranteed maximum difference between fastest  $CASI$  to  $\overline{CASn}$  delay and the slowest  $MSEL$  to  $Qn$  delay on any single device.

Note D: Guaranteed maximum difference between fastest  $RASi$  to  $\overline{RASn}$  delay and the slowest  $MCn$  to  $Qn$  delay on any single device.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	−0.5V to V <sub>CC</sub>
Standard Output TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature

Military

Commercial

Supply Voltage

Military

Commercial

−55°C to +125°C

0°C to +70°C

+4.5V to +5.5V

+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = −1 mA
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = −1 mA
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = −3 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 1.0 mA
		54F 10% V <sub>CC</sub>		0.8			I <sub>OL</sub> = 12.0 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 1.0 mA
		74F 10% V <sub>CC</sub>		0.8			I <sub>OL</sub> = 12.0 mA
I <sub>IH</sub>	Input HIGH Current			20	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			100	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	−60		−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CEX</sub>	Output HIGH Leakage Current			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current			300	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			300	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current			300	mA	Max	V <sub>O</sub> = HIGH Z

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	29F		Military 29F		Commercial 29F				Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 500\text{ pF}$			
		Min	Max	Min	Max	Min	Max	Min	Typ		
$t_{PLH}$	Propagation Delay	3.0	11.0			2.5	12.0		19.0	ns	2-3
$t_{PHL}$	AR to $Q_n$	3.0	11.0			2.5	12.0		22.0		
$t_{PLH}$	Propagation Delay	3.0	11.0			2.5	12.0		19.0	ns	2-3
$t_{PHL}$	AC to $Q_n$	3.0	11.0			2.5	12.0		22.0		
$t_{PLH}$	Propagation Delay	3.5	12.0			3.0	13.0		23.0	ns	2-3
$t_{PHL}$	RASI to RAS <sub>i</sub>	3.5	12.0			3.0	13.0		20.0		
$t_{PLH}$	Propagation Delay	1.0	8.0			1.0	8.5		19.0	ns	2-3
$t_{PHL}$	CASI to CAS <sub>i</sub>	1.0	8.0			1.0	8.5		17.0		
$t_{PLH}$	Propagation Delay	3.0	13.0			2.5	14.0		24.0	ns	2-3
$t_{PHL}$	MSEL to $Q_n$	3.0	13.0			2.5	14.0		21.0		
$t_{PLH}$	Propagation Delay	4.0	15.0			3.5	16.0		25.0	ns	2-3
$t_{PHL}$	MC <sub>n</sub> to $Q_n$	4.0	15.0			3.5	16.0		22.0		
$t_{PLH}$	Propagation Delay	3.5	17.5			3.0	18.5		24.0	ns	2-3
$t_{PHL}$	MC <sub>n</sub> to RAS <sub>n</sub>	3.5	17.5			3.0	18.5		22.0		
$t_{PLH}$	Propagation Delay	4.0	12.5			3.5	13.5		23.0	ns	2-3
$t_{PHL}$	MC <sub>n</sub> to CAS <sub>n</sub>	4.0	12.5			3.5	13.5		21.0		
$t_{PLH}$	Propagation Delay	4.0	15.0			3.5	16.0		25.0	ns	2-3
$t_{PHL}$	LE to RAS <sub>n</sub>	4.0	15.0			3.5	16.0		24.0		
$t_{PLH}$	Propagation Delay	5.0	13.5			4.5	14.5		24.0	ns	2-3
$t_{PHL}$	LE to CAS <sub>n</sub>	5.0	13.5			4.5	14.5		24.0		
$t_{PLH}$	Propagation Delay	3.5	12.0			3.0	13.0		23.0	ns	2-3
$t_{PHL}$	LE to $Q_n$	3.5	12.0			3.0	13.0		22.0		

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	29F		Military 29F		Commercial 29F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Max	Min	Max	Min	Max		
$t_{pZH}$ $t_{pZL}$	Output Disable Time OE to $Q_n$	1.0 1.0	9.5 9.5			1.0 1.0	10.0 10.0	ns	2-5
$t_{pZH}$ $t_{pZL}$	Output Disable Time OE to $Q_n$	1.0 1.0	9.5 9.5			1.0 1.0	10.0 10.0	ns	2-5
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time OE to $RAS_n$	1.0 1.0	9.5 9.5			1.0 1.0	10.0 10.0	ns	2-5
$t_{pZH}$ $t_{pZL}$	Output Disable Time OE to $RAS_n$	1.0 1.0	9.5 9.5			1.0 1.0	10.0 10.0	ns	2-5
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time OE to $CAS_n$	1.0 1.0	9.5 9.5			1.0 1.0	10.0 10.0	ns	2-5
$t_{pZH}$ $t_{pZL}$	Output Enable Time OE to $CAS_n$	1.0 1.0	9.5 9.5			1.0 1.0	10.0 10.0	ns	2-5
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW $CAS_n, RAS_n$	15.0 15.0				15.0 15.0		ns	2-4
$t_{skew}$	$Q_n$ to $CAS_n, RAS_n$		10.0				10.0	ns	

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	29F		Military 29F	Commercial 29F	Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$	$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $A_n$ to LE	5.0 5.0			5.0 5.0	ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $A_n$ to LE	5.0 5.0			5.0 5.0	ns	2-6
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW SEL to LE	5.0 5.0			5.0 5.0	ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW SEL to LE	5.0 5.0			5.0 5.0	ns	2-6







## Section 5 Contents

Ordering Information and Physical Dimensions  
Bookshelf  
Distributors  
5-3

# Section 5 Ordering Information and Physical Dimensions

**Section 5 Contents**

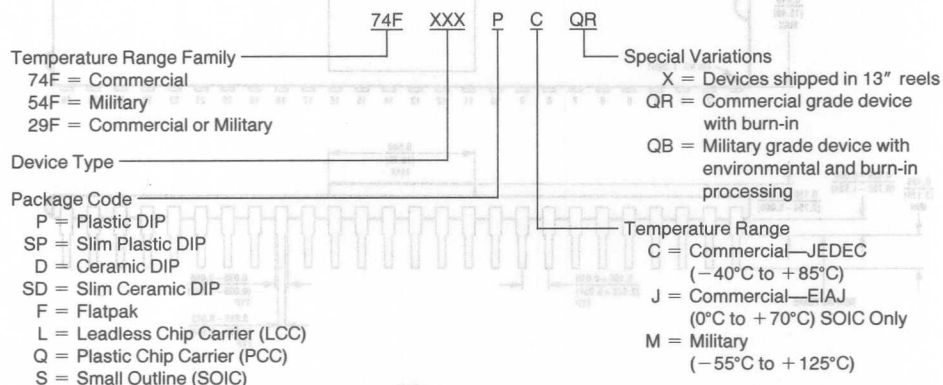
Ordering Information and Physical Dimensions .....	5-3
Bookshelf	
Distributors	

Section 5  
Ordering Information and  
Physical Dimensions



## FAST® Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

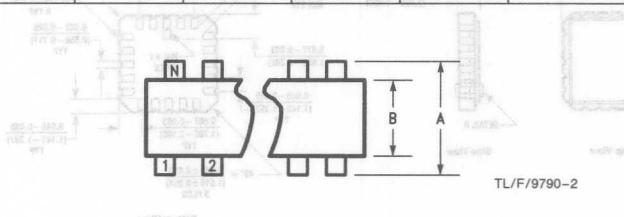


**For most current packaging information, contact Product Marketing.**

JEDEC-EIAJ Small Outline Package Comparison

	Dim	14-Pin		16-Pin		20-Pin		24-Pin	
		Min	Max	Min	Max	Min	Max	Min	Max
JEDEC	A	0.228 (5.80)	0.245 (6.20)	0.228 (5.80)	0.245 (6.20)	0.393 (10.0)	0.420 (10.65)	0.393 (10.0)	0.420 (10.65)
	B	0.149 (3.80)	0.158 (4.00)	0.149 (3.80)	0.158 (4.00)	0.291 (7.40)	0.300 (7.60)	0.291 (7.40)	0.300 (7.60)
EIAJ	A	0.300 (7.62)	0.350 (8.89)	0.300 (7.62)	0.350 (8.89)	0.300 (7.62)	0.350 (8.89)	0.300 (7.62)	0.350 (8.89)
	B	0.198 (5.02)	0.245 (6.22)	0.198 (5.02)	0.245 (6.22)	0.198 (5.02)	0.245 (6.22)	0.198 (5.02)	0.245 (6.22)

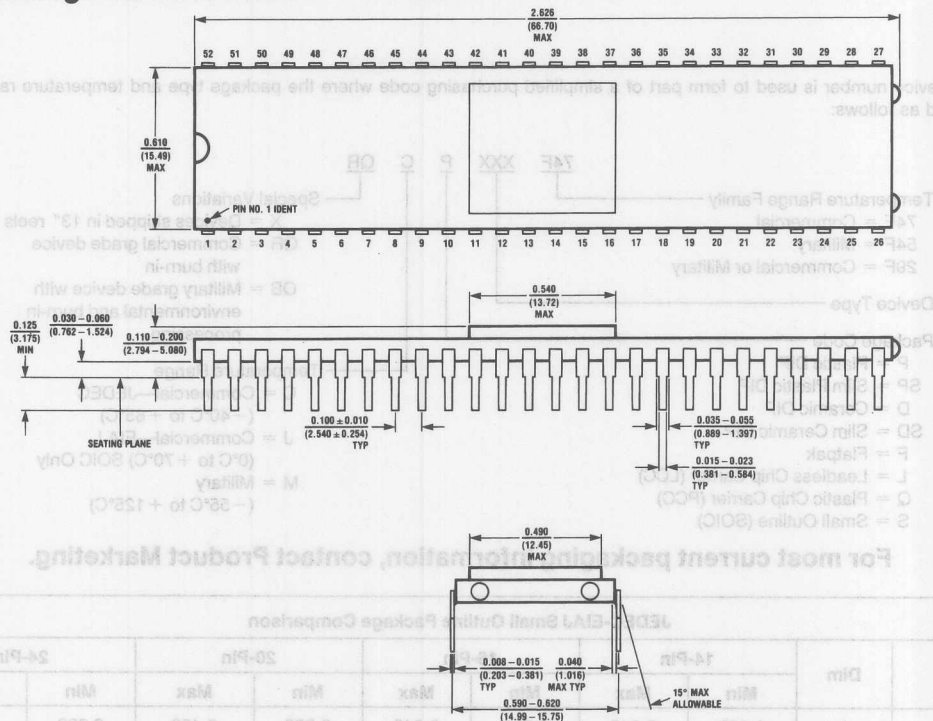
Units: inch (mm)



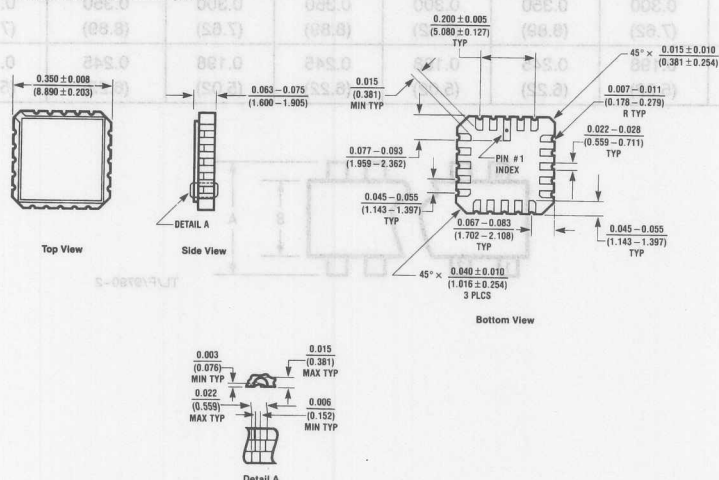


All dimensions are in inches (millimeters)

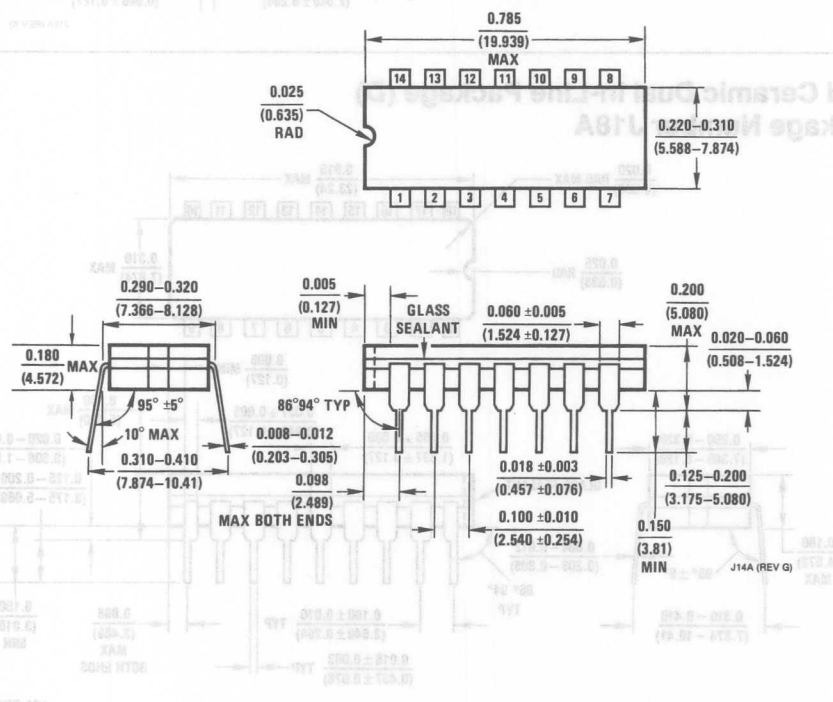
## 52 Lead Side-Brazed Dual In-Line Package (D) NS Package Number D52A



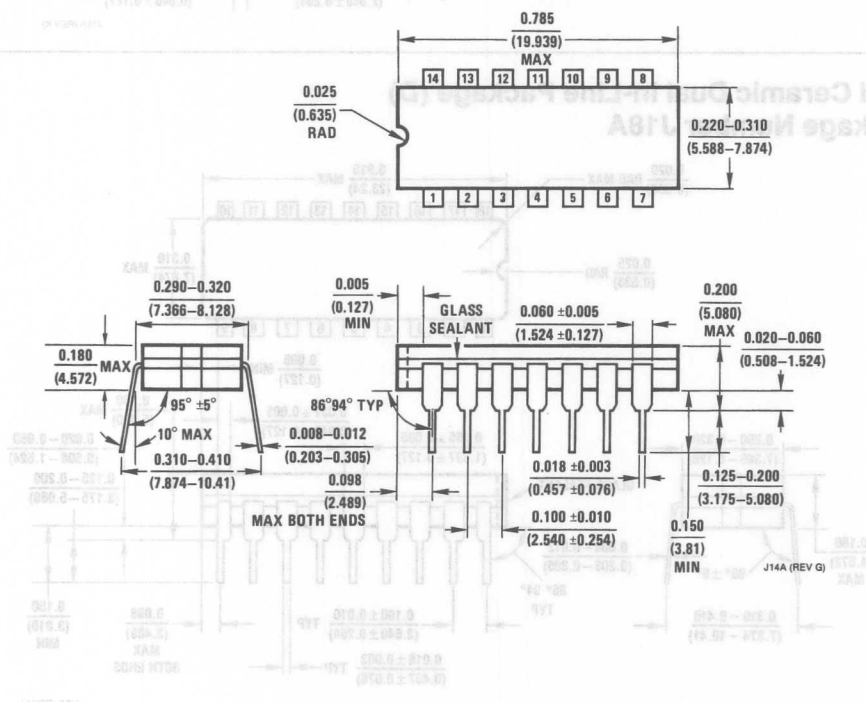
## 20 Terminal Ceramic Leadless Chip Carrier (L) NS Package Number E20A



5

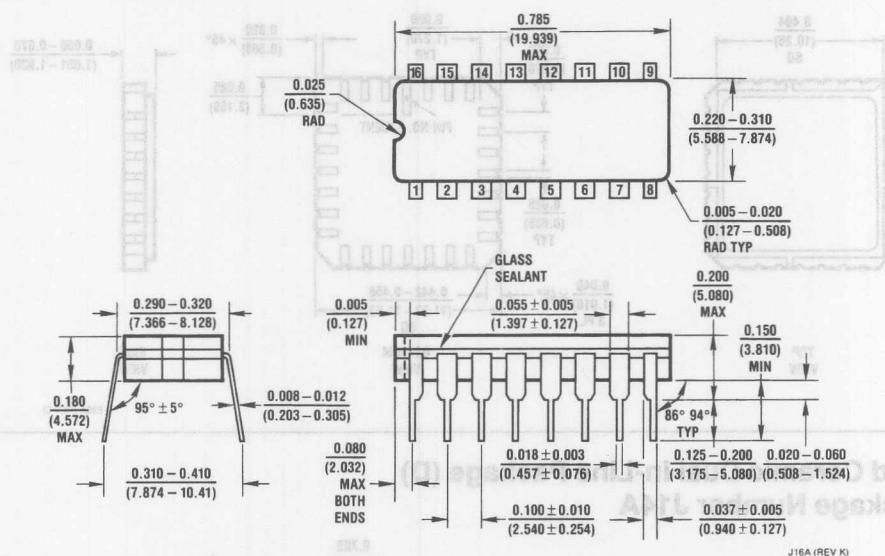


0.220-0.310



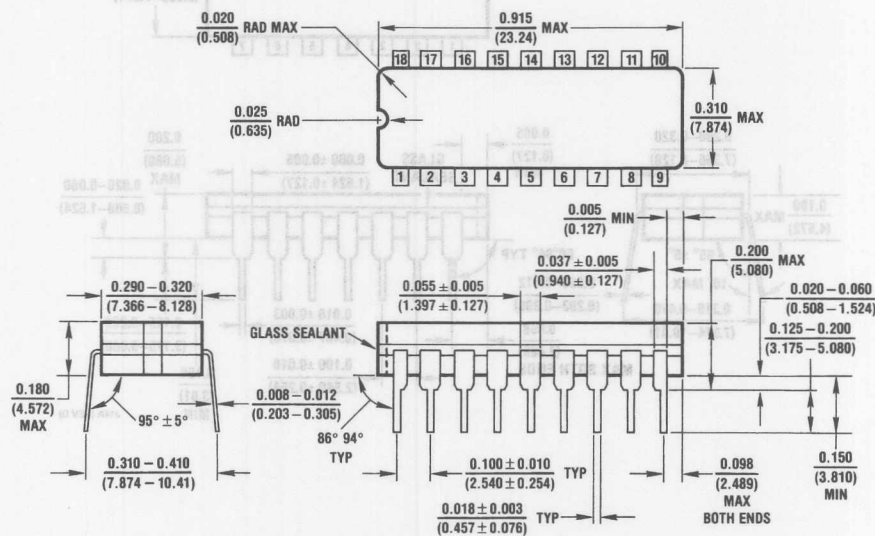


**16 Lead Ceramic Dual In-Line Package (D)  
NS Package Number J16A**



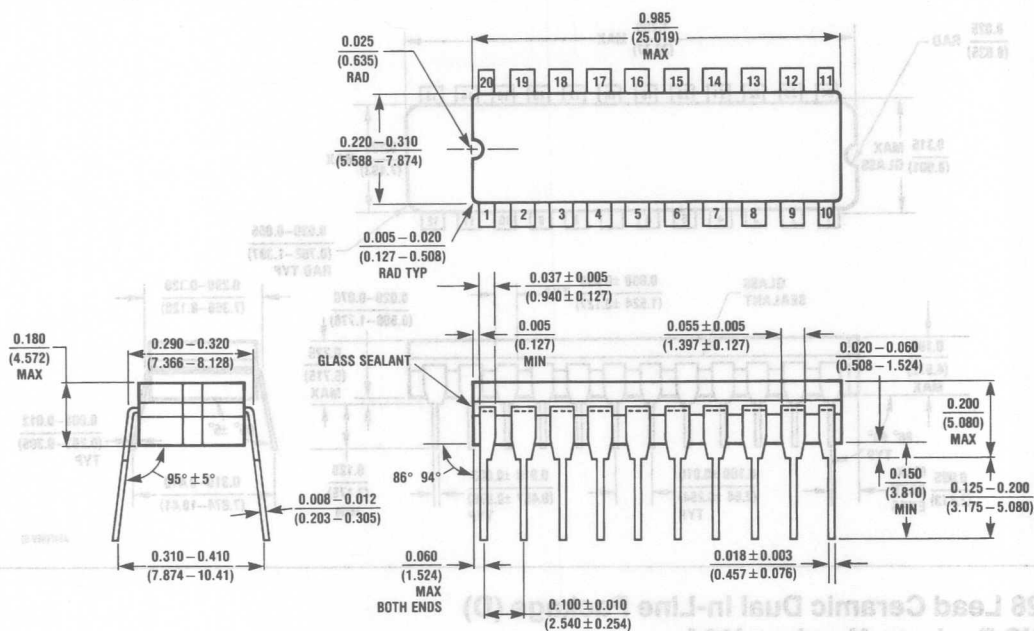
J16A (REV K)

**18 Lead Ceramic Dual In-Line Package (D)  
NS Package Number J18A**

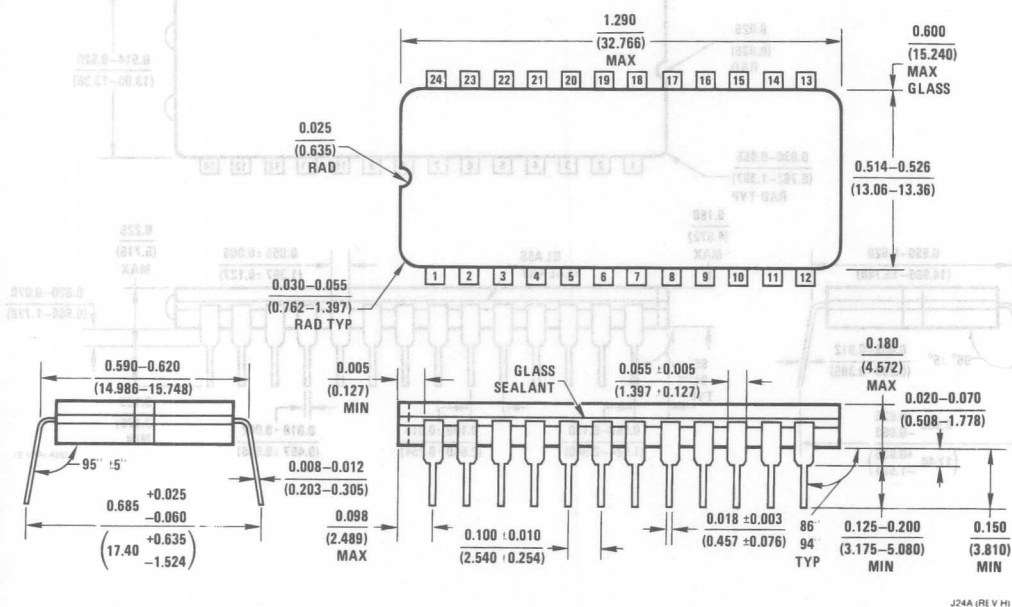


J18A (REV L)

## 20 Lead Ceramic Dual In-Line Package (D) NS Package Number J20A



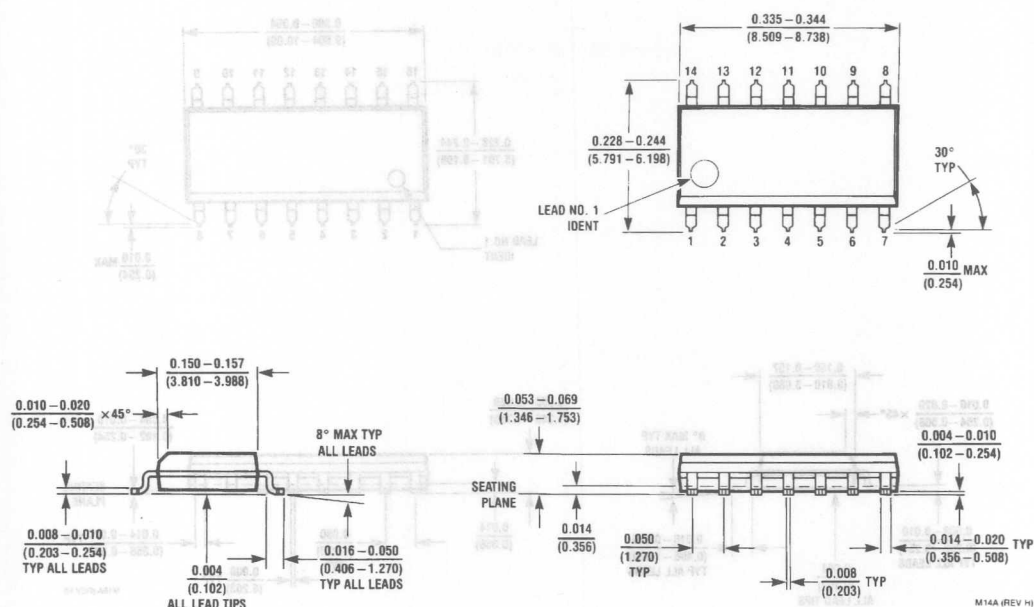
## 24 Lead Ceramic Dual In-Line Package (D) NS Package Number J24A



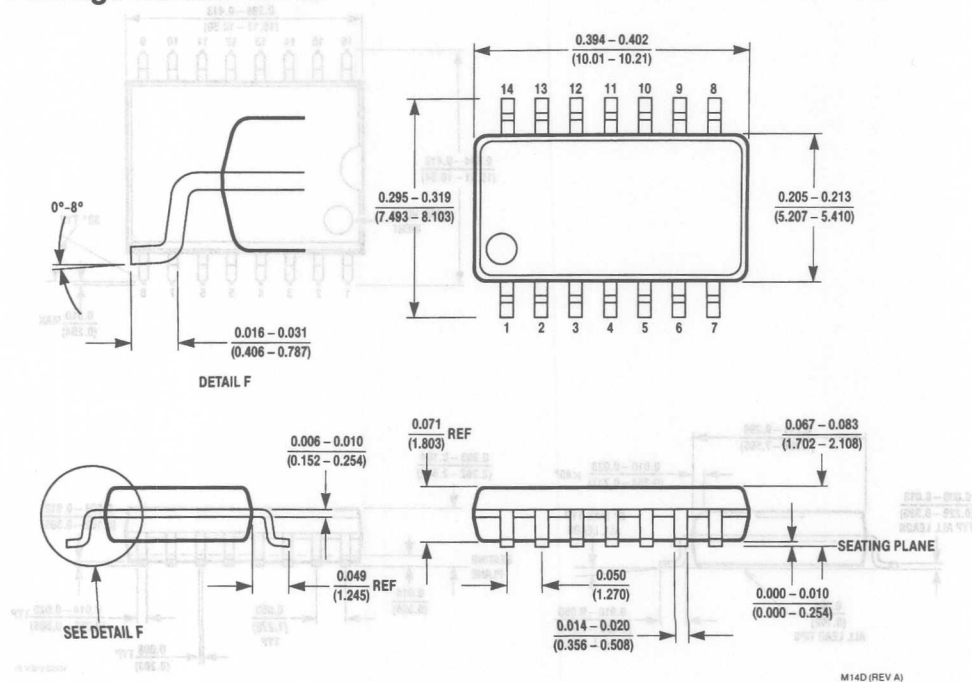


## J28A, REV F

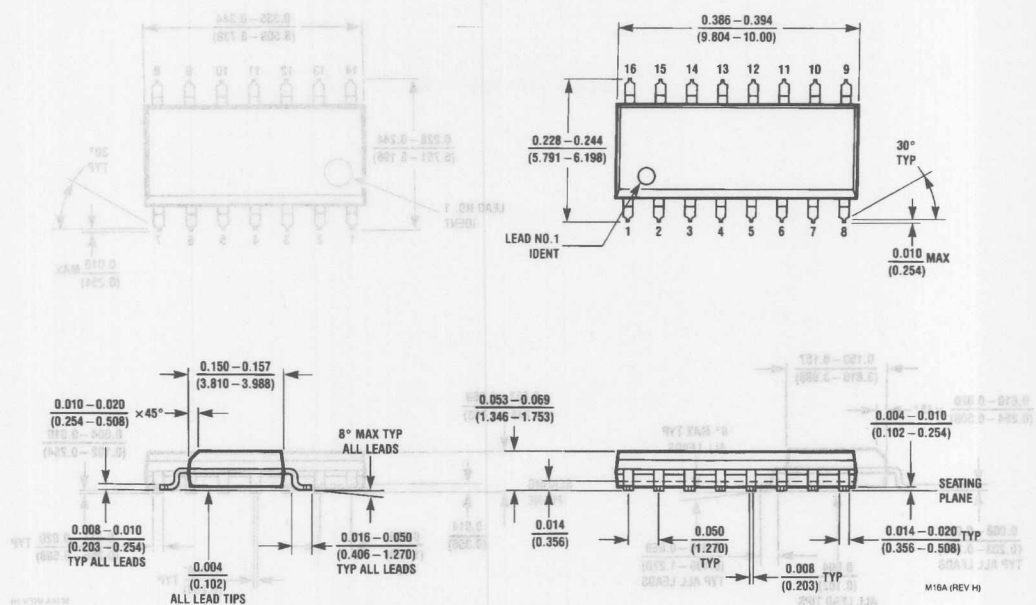
# 14 Lead Small Outline Integrated Circuit (S) NS Package Number M14A



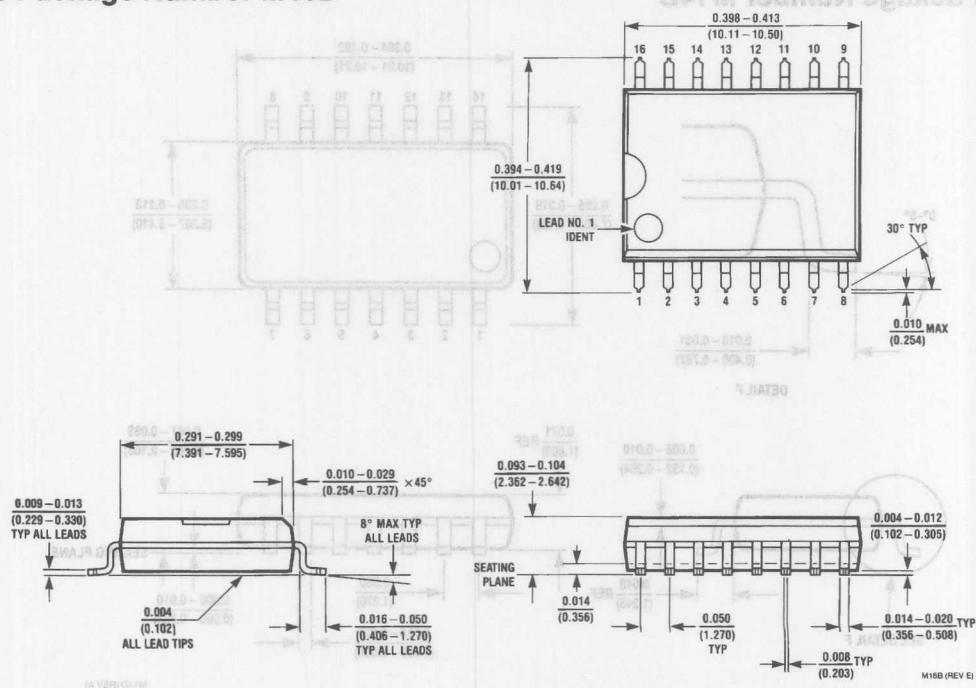
# 14 Lead Small Outline Package — EIAJ (SJ) NS Package Number M14D



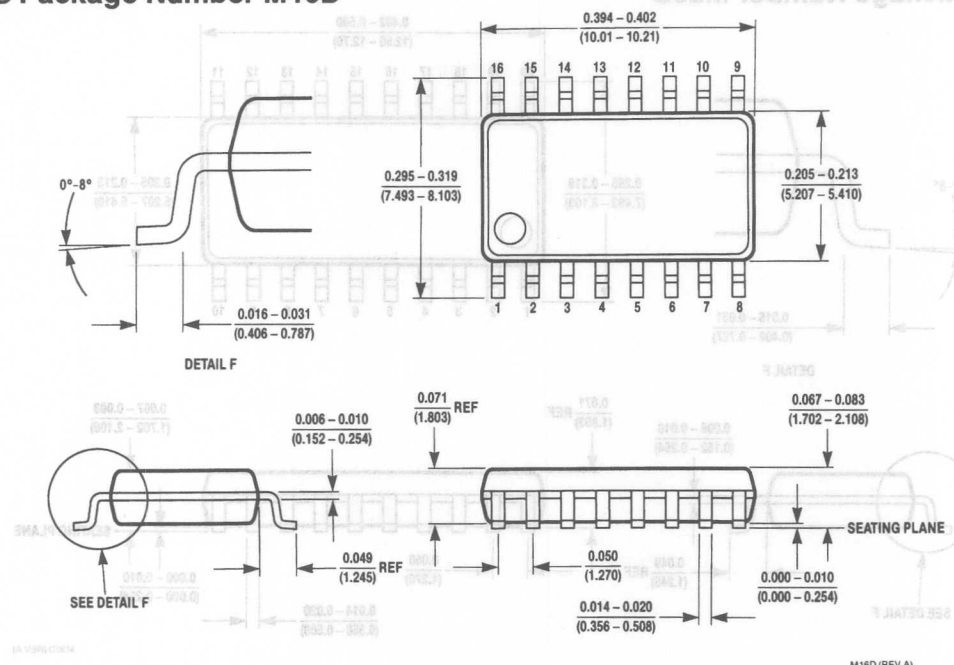
# 16 Lead Small Outline Integrated Circuit (S) NS Package Number M16A



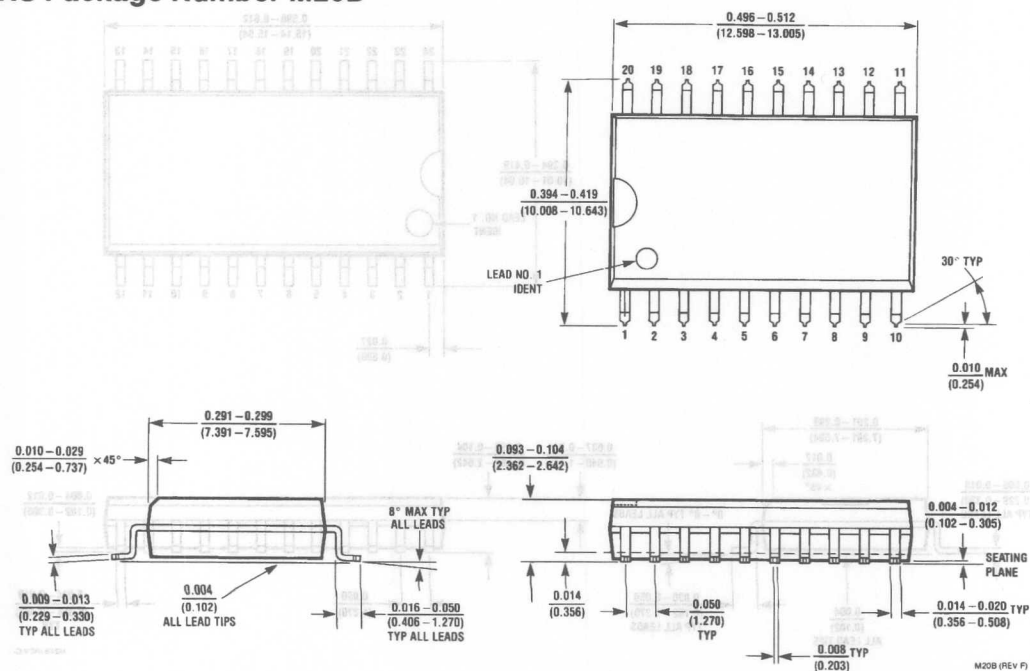
# 16 Lead (0.300" Wide) Small Outline Integrated Circuit (S) NS Package Number M16B



# 16 Lead Small Outline Package — EIAJ (SJ) NS Package Number M16D

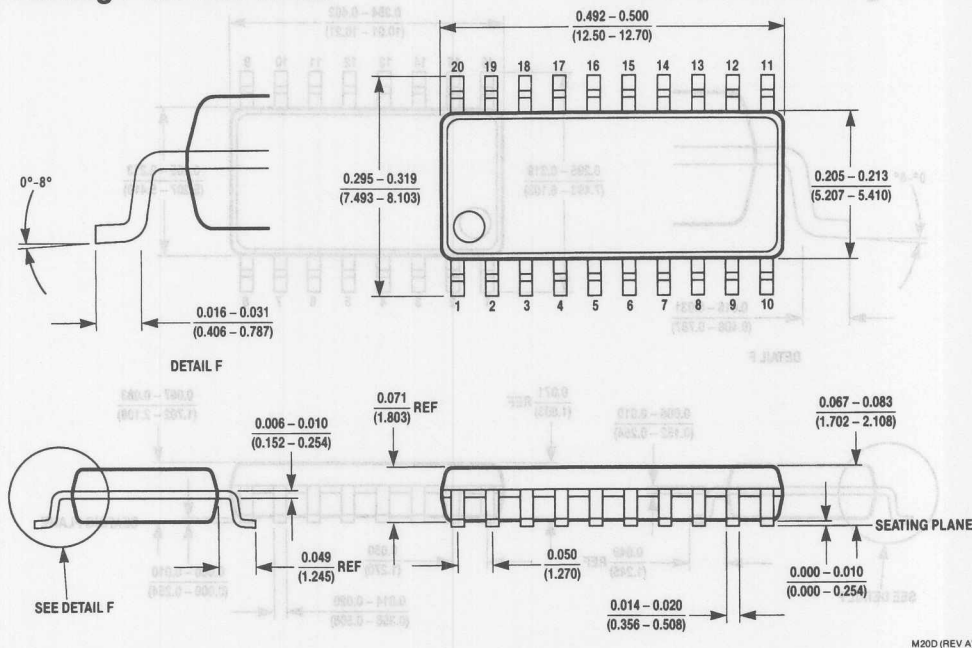


# 20 Lead Small Outline Integrated Circuit (S) NS Package Number M20B

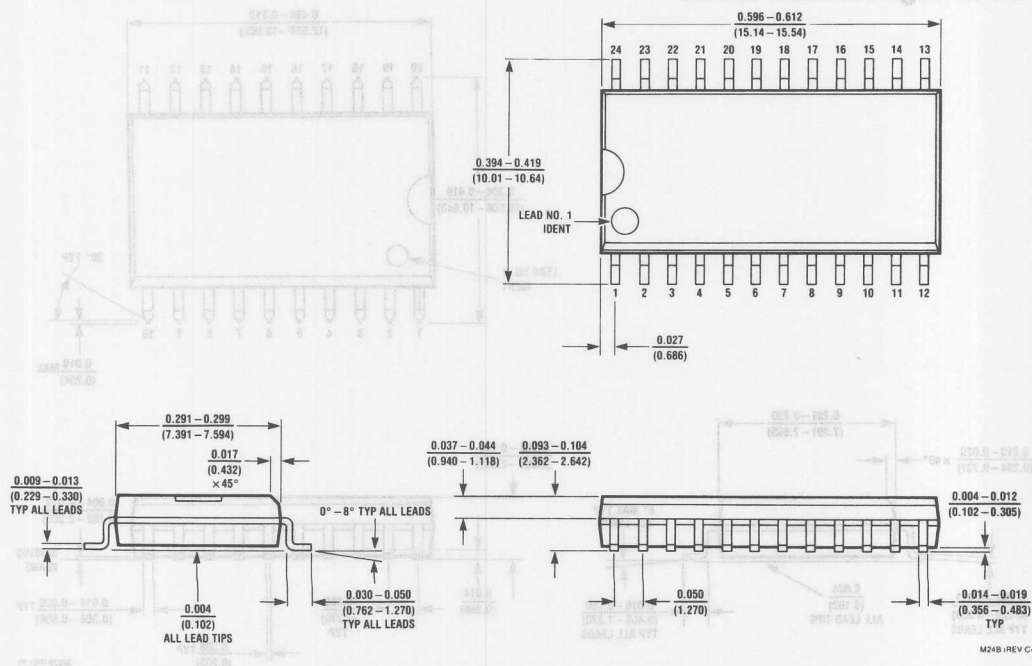


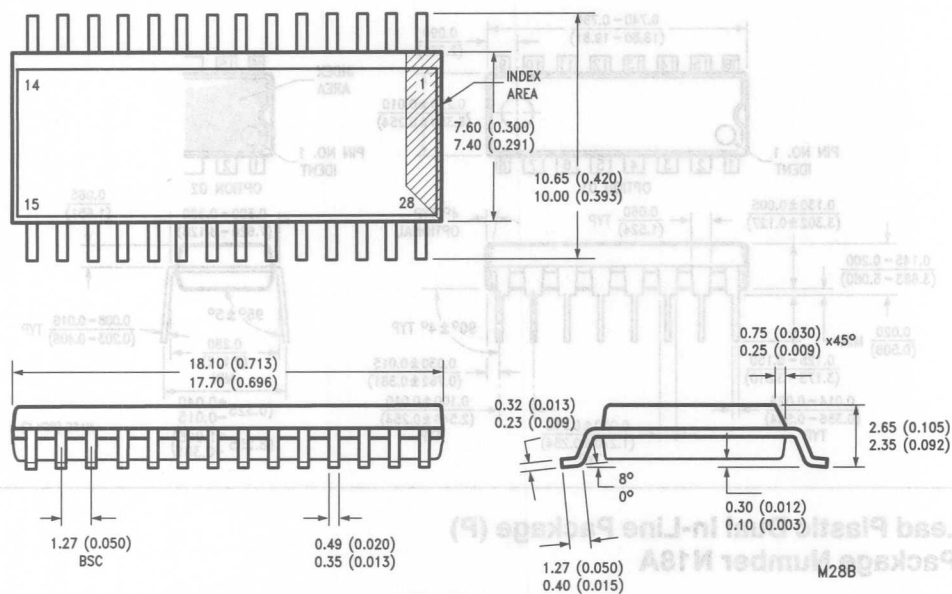


# 20 Lead Small Outline Package — EIAJ (SJ) NS Package Number M20D

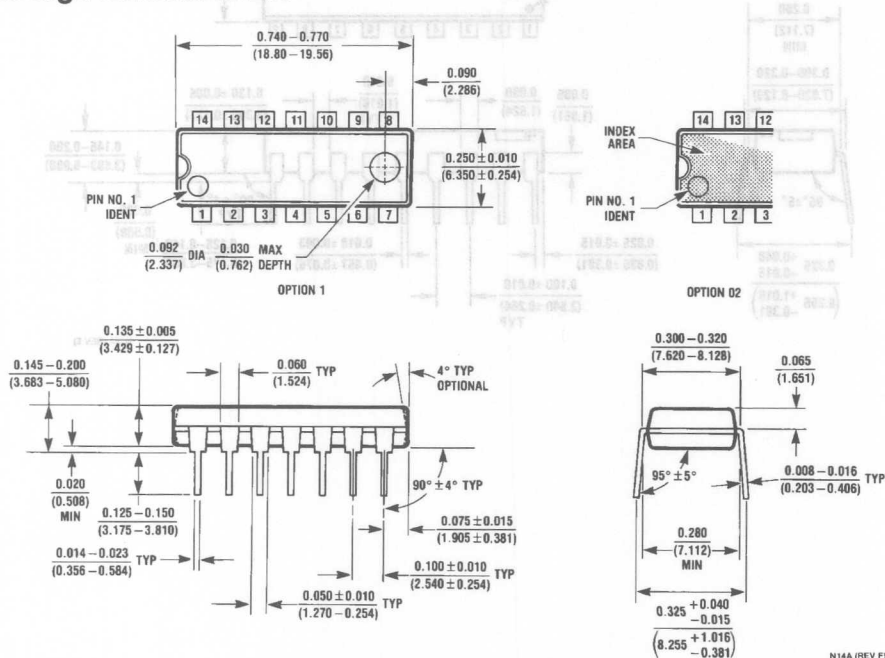


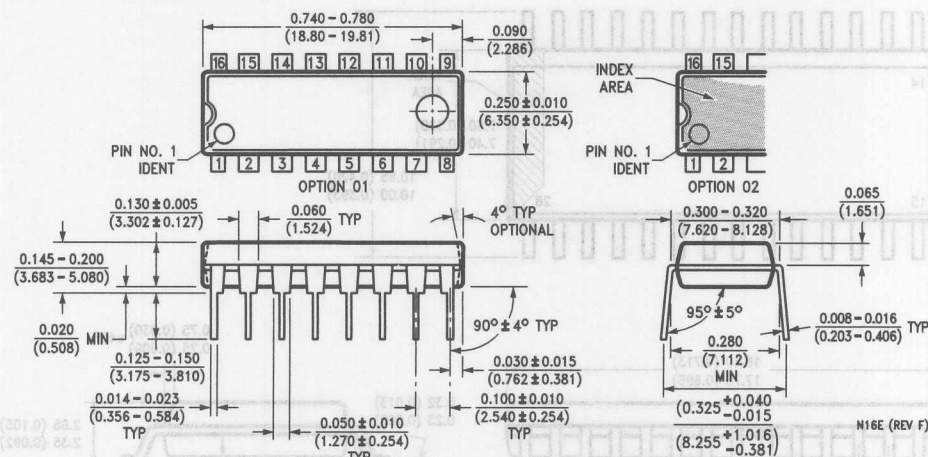
# 24 Lead Small Outline Integrated Circuit (S) NS Package Number M24B



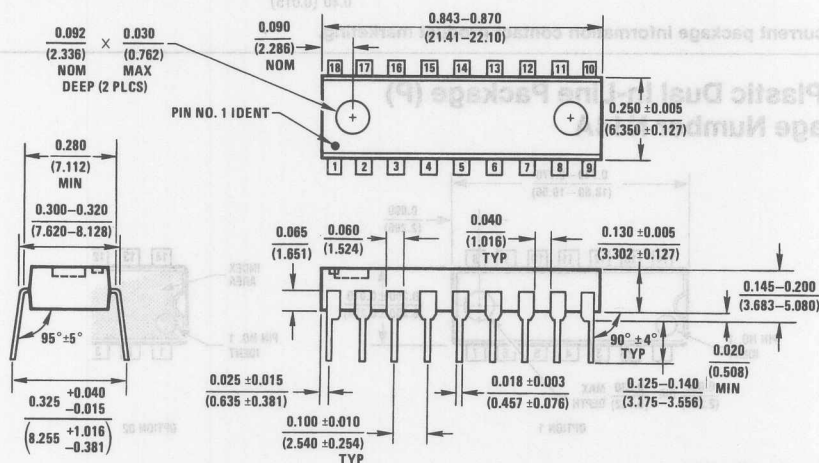
**28 Lead Small Outline Integrated Circuit (S)****\*NS Package Number M28B**

\*For most current package information contact product marketing.

**14 Lead Plastic Dual In-Line Package (P)****NS Package Number N14A**



**18 Lead Plastic Dual In-Line Package (P)  
NS Package Number N18A**



Technical drawing of a 10-pin D-sub connector, showing front, side, and detail views with dimensions in inches and millimeters.

**Front View Dimensions:**

- Overall Width:  $0.970 \pm 0.090$  (24.638–25.146)
- Pin Pitch:  $0.092 \times 0.030$  (2.337  $\times$  0.762) MAX DP
- Pin 10 Position:  $0.240 \pm 0.260$  (6.096–6.604)
- Pin 1 Position:  $0.032 \pm 0.005$  (0.813  $\pm$  0.127) RAD

**Side View Dimensions:**

- Overall Height:  $0.280$  (7.112) MIN
- Pin Height:  $0.290 \pm 0.325$  (7.366–8.255)
- Pin Angle:  $97.5^\circ \pm 7.5^\circ$
- Pin Spacing:  $0.065$  (1.651)
- Pin Diameter:  $0.060$  NOM (1.524) TYP
- Pin Spacing:  $0.040$  (1.016) TYP
- Pin Spacing:  $0.130$  0.005 (3.302 0.127)
- Pin Spacing:  $0.145 \pm 0.200$  (3.683–5.080)
- Pin Spacing:  $0.020$  (0.508) MIN
- Pin Spacing:  $0.125 \pm 0.150$  (3.175–3.810)
- Pin Spacing:  $0.100 \pm 0.010$  (2.540  $\pm$  0.254)
- Pin Spacing:  $0.014 \pm 0.023$  (0.355–0.585)
- Pin Angle:  $90^\circ \pm 0.004^\circ$

**Detail Views:**

- OPTION 1:** Shows the pin 10 position and the pin 1 position.
- OPTION 2:** Shows the pin 10 position and the pin 1 position.

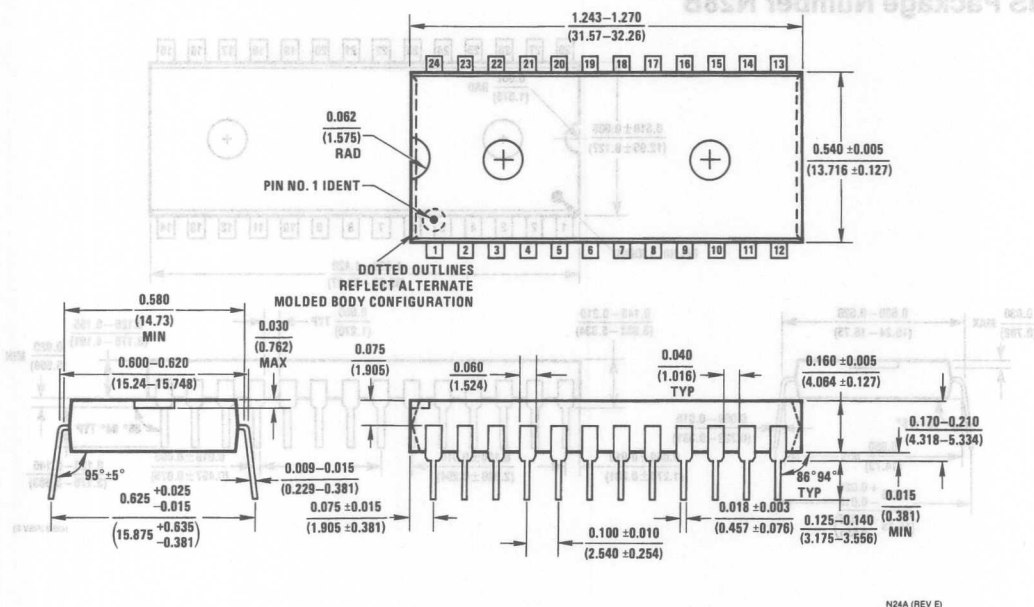
**Pin Numbers:** 1 through 10 are labeled on the top of the connector.

**Notes:**

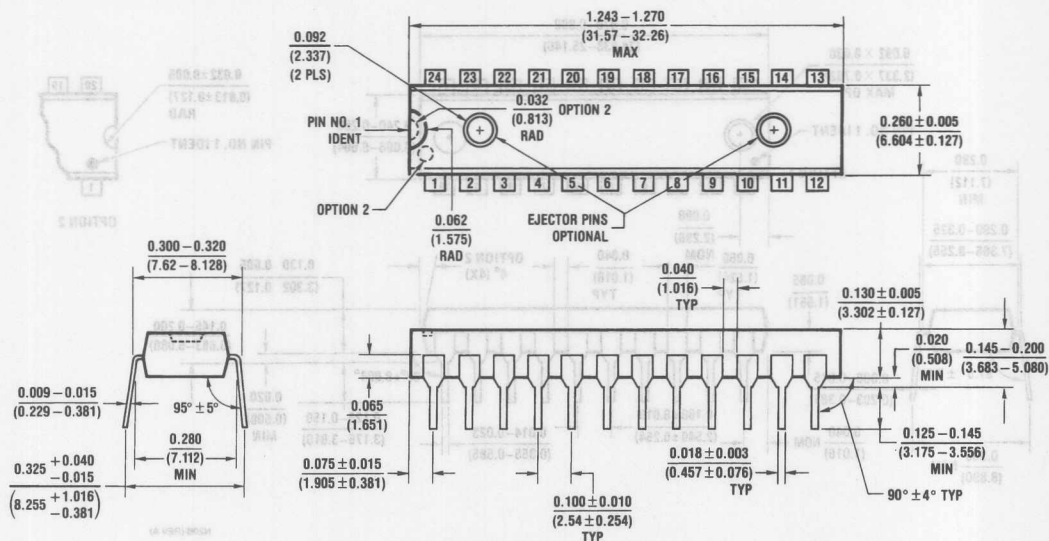
- PIN NO. 1 IDENT
- OPTION 1
- OPTION 2
- 90° ± 0.004°

**Dimensions in Millimeters:**

- Overall Width: 24.638–25.146
- Pin Pitch: 2.337  $\times$  0.762
- Pin 10 Position: 6.096–6.604
- Pin 1 Position: 0.813  $\pm$  0.127
- Overall Height: 7.112
- Pin Height: 7.366–8.255
- Pin Angle: 97.5°  $\pm$  7.5°
- Pin Spacing: 1.651
- Pin Diameter: 1.524
- Pin Spacing: 1.016
- Pin Spacing: 3.302 0.127
- Pin Spacing: 3.683–5.080
- Pin Spacing: 0.508
- Pin Spacing: 3.175–3.810
- Pin Spacing: 2.540  $\pm$  0.254
- Pin Spacing: 0.355–0.585
- Pin Angle: 90°  $\pm$  0.004°

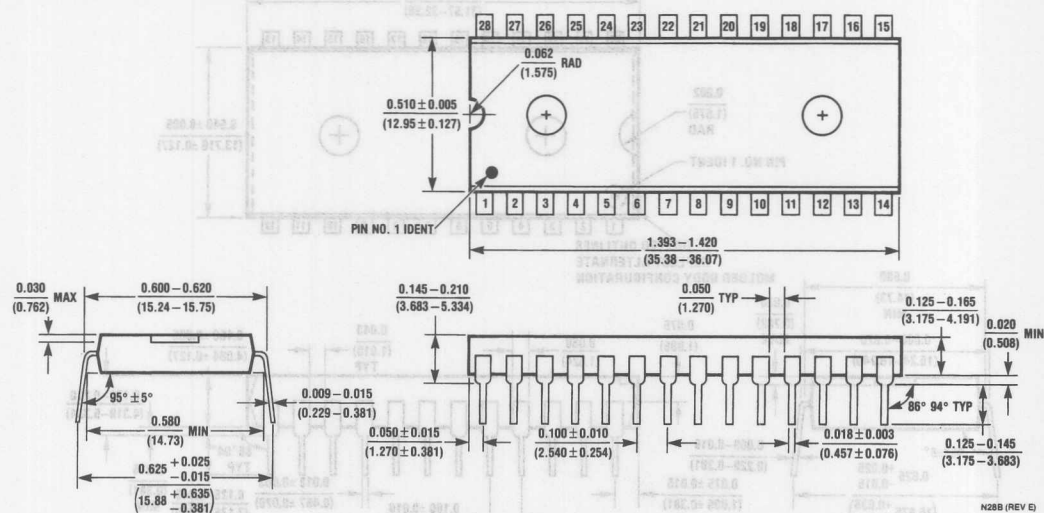


## 24 Lead Slim (0.300" Wide) Plastic Dual In-Line Package (SP) NS Package Number N24C



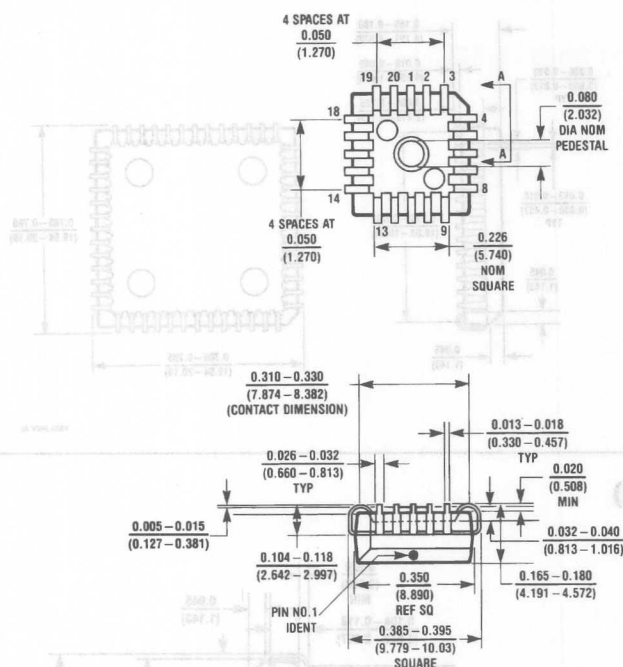
N24C (REV F)

## 28 Lead Plastic Dual In-Line Package (P) NS Package Number N28B

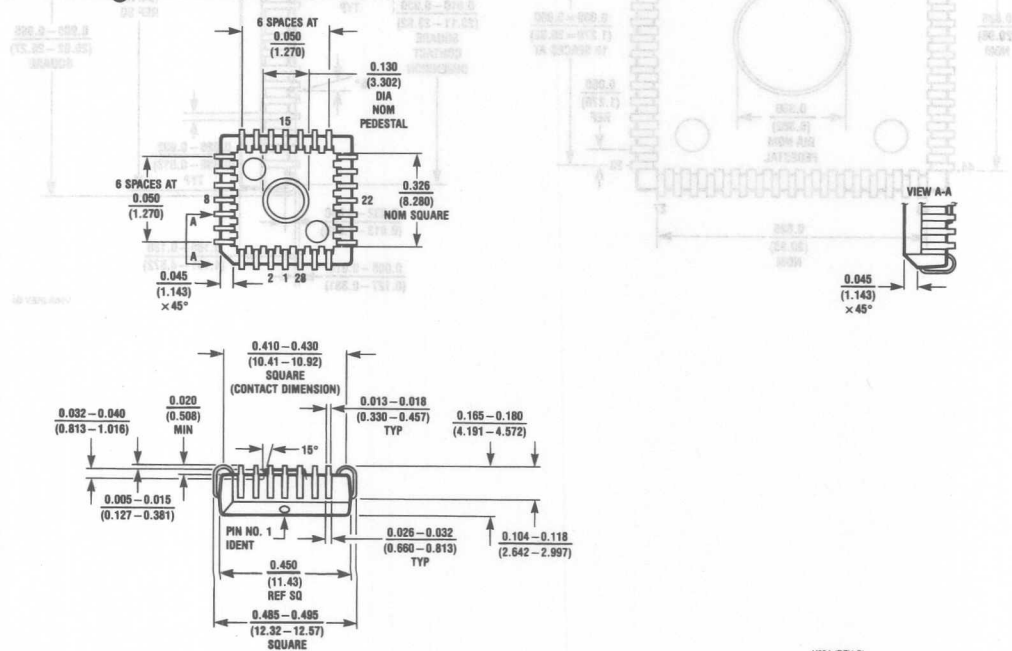


N28B (REV E)

## 20 Lead Plastic Chip Carrier (Q) NS Package Number V20A

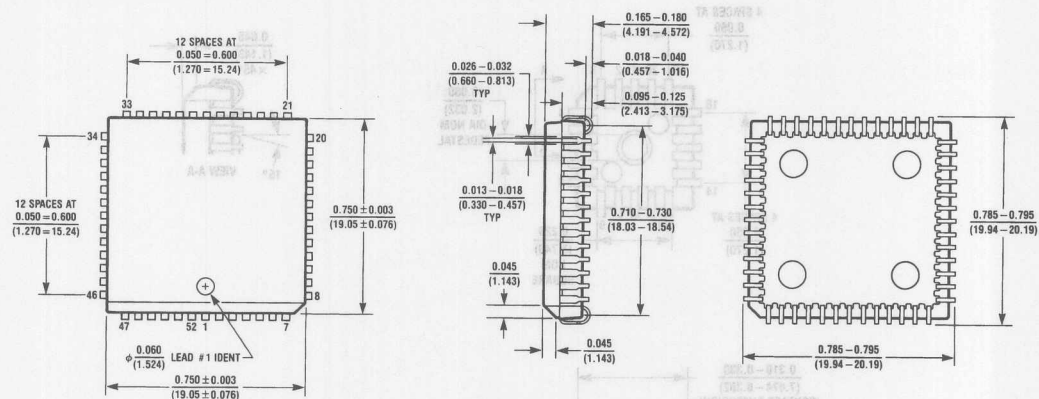


## 28 Lead Plastic Chip Carrier (Q) NS Package Number V28A

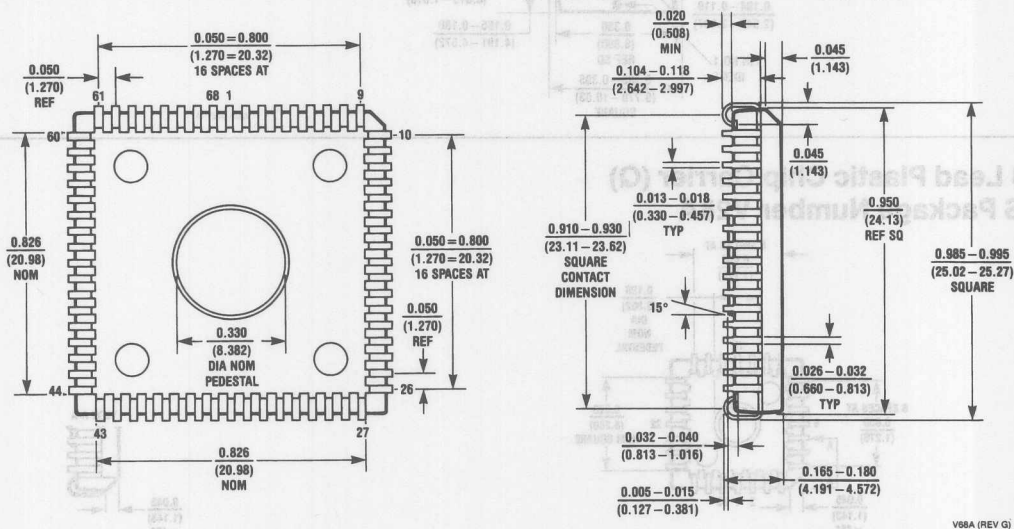




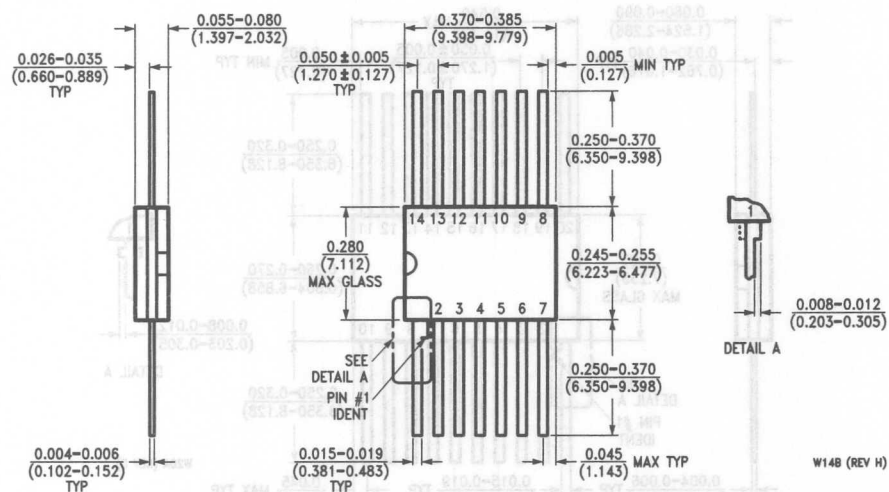
## 52 Lead Plastic Chip Carrier (Q) NS Package Number V52A



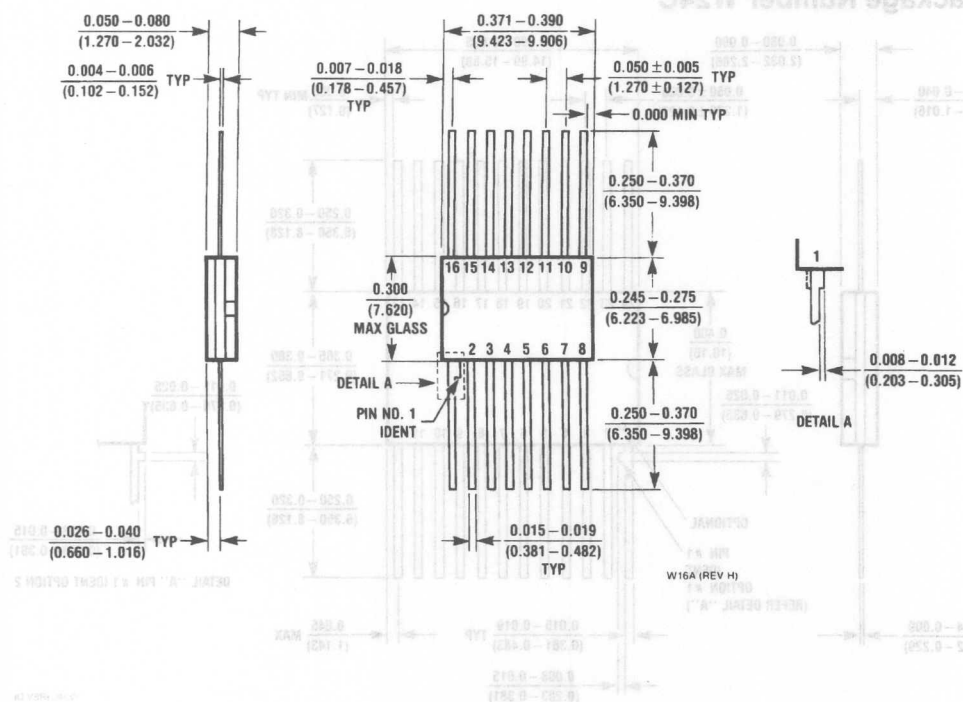
## 68 Lead Plastic Chip Carrier (Q) NS Package Number V68A



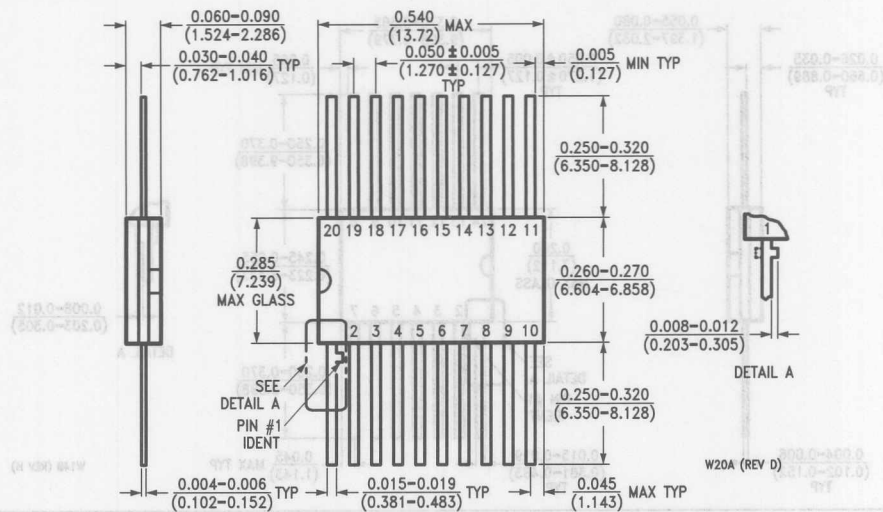
# 14 Lead Ceramic Flatpak (F) NS Package Number W14B



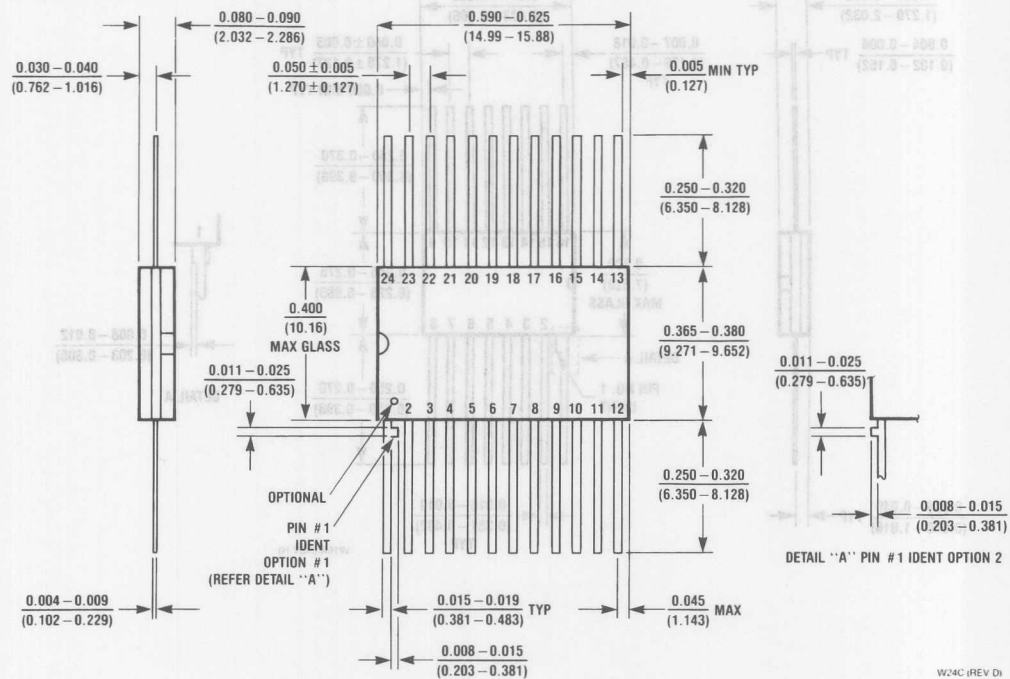
# 16 Lead Ceramic Flatpak (F) NS Package Number W16A



## 20 Lead Ceramic Flatpak (F) NS Package Number W20A



## 24 Lead Ceramic Flatpak (F) NS Package Number W24C







NOTES

## **Bookshelf of Technical Support Information**

National Semiconductor Corporation recognizes the need to keep you informed about the availability of current technical literature.

This bookshelf is a compilation of books that are currently available. The listing that follows shows the publication year and section contents for each book.

Please contact your local National sales office for possible complimentary copies. A listing of sales offices follows this bookshelf.

We are interested in your comments on our technical literature and your suggestions for improvement.

Please send them to:

Technical Communications Dept. M/S 16-300  
2900 Semiconductor Drive  
P.O. Box 58090  
Santa Clara, CA 95052-8090

## **ALS/AS LOGIC DATABOOK—1990**

Introduction to Advanced Bipolar Logic • Advanced Low Power Schottky • Advanced Schottky

## **ASIC DESIGN MANUAL/GATE ARRAYS & STANDARD CELLS—1987**

SSI/MSI Functions • Peripheral Functions • LSI/VLSI Functions • Design Guidelines • Packaging

## **CMOS LOGIC DATABOOK—1988**

CMOS AC Switching Test Circuits and Timing Waveforms • CMOS Application Notes • MM54HC/MM74HC  
MM54HCT/MM74HCT • CD4XXX • MM54CXXX/MM74CXXX • Surface Mount

## **DATA ACQUISITION LINEAR DEVICES—1989**

Active Filters • Analog Switches/Multiplexers • Analog-to-Digital Converters • Digital-to-Analog Converters  
Sample and Hold • Temperature Sensors • Voltage Regulators • Surface Mount

## **DATA COMMUNICATION/LAN/UART DATABOOK—1990**

LAN IEEE 802.3 • High Speed Serial/IBM Data Communications • ISDN Components • UARTs  
Modems • Transmission Line Drivers/Receivers

## **DISCRETE SEMICONDUCTOR PRODUCTS DATABOOK—1989**

Selection Guide and Cross Reference Guides • Diodes • Bipolar NPN Transistors  
Bipolar PNP Transistors • JFET Transistors • Surface Mount Products • Pro-Electron Series  
Consumer Series • Power Components • Transistor Datasheets • Process Characteristics

## **DRAM MANAGEMENT HANDBOOK—1989**

Dynamic Memory Control • Error Detection and Correction • Microprocessor Applications for the  
DP8408A/09A/17/18/19/28/29 • Microprocessor Applications for the DP8420A/21A/22A  
Microprocessor Applications for the NS32CG821

## **EMBEDDED SYSTEM PROCESSOR DATABOOK—1989**

Embedded System Processor Overview • Central Processing Units • Slave Processors • Peripherals  
Development Systems and Software Tools

## **F100K ECL LOGIC DATABOOK & DESIGN GUIDE—1990**

Family Overview • 300 Series (Low-Power) Datasheets • 100 Series Datasheets • 11C Datasheets  
ECL BiCMOS SRAM, ECL PAL, and ECL ASIC Datasheets • Design Guide • Circuit Basics • Logic Design  
Transmission Line Concepts • System Considerations • Power Distribution and Thermal Considerations  
Testing Techniques • Quality Assurance and Reliability • Application Notes

Quiet Series: 54ACT1Q/74ACT1QXXX • 54FCT/74FCTXXX • FCTA: 54FCTXXXA/74FCTXXXA

## **FAST® ADVANCED SCHOTTKY TTL LOGIC DATABOOK—1990**

Circuit Characteristics • Ratings, Specifications and Waveforms • Design Considerations • 54F/74FXXX

## **FAST® APPLICATIONS HANDBOOK—1990**

Reprint of 1987 Fairchild FAST Applications Handbook

Contains application information on the FAST family: Introduction • Multiplexers • Decoders • Encoders  
Operators • FIFOs • Counters • TTL Small Scale Integration • Line Driving and System Design  
FAST Characteristics and Testing • Packaging Characteristics

## **GENERAL PURPOSE LINEAR DEVICES DATABOOK—1989**

Continuous Voltage Regulators • Switching Voltage Regulators • Operational Amplifiers • Buffers • Voltage Comparators  
Instrumentation Amplifiers • Surface Mount

## **GRAPHICS HANDBOOK—1989**

Advanced Graphics Chipset • DP8500 Development Tools • Application Notes

## **INTERFACE DATABOOK—1990**

Transmission Line Drivers/Receivers • Bus Transceivers • Peripheral Power Drivers • Display Drivers  
Memory Support • Microprocessor Support • Level Translators and Buffers • Frequency Synthesis • Hi-Rel Interface

## **LINEAR APPLICATIONS HANDBOOK—1986**

The purpose of this handbook is to provide a fully indexed and cross-referenced collection of linear integrated circuit applications using both monolithic and hybrid circuits from National Semiconductor.

Individual application notes are normally written to explain the operation and use of one particular device or to detail various methods of accomplishing a given function. The organization of this handbook takes advantage of this innate coherence by keeping each application note intact, arranging them in numerical order, and providing a detailed Subject Index.

## **LS/S/TTL DATABOOK—1989**

Contains former Fairchild Products

Introduction to Bipolar Logic • Low Power Schottky • Schottky • TTL • TTL—Low Power

## **MASS STORAGE HANDBOOK—1989**

Rigid Disk Pulse Detectors • Rigid Disk Data Separators/Synchronizers and ENDECs  
Rigid Disk Data Controller • SCSI Bus Interface Circuits • Floppy Disk Controllers • Disk Drive Interface Circuits  
Rigid Disk Preamplifiers and Servo Control Circuits • Rigid Disk Microcontroller Circuits • Disk Interface Design Guide

## **MEMORY DATABOOK—1990**

PROMs, EPROMs, EEPROMs • TTL I/O SRAMs • ECL I/O SRAMs

## **MICROCONTROLLER DATABOOK—1989**

COP400 Family • COP800 Family • COPS Applications • HPC Family • HPC Applications  
MICROWIRE and MICROWIRE/PLUS Peripherals • Microcontroller Development Tools

## **MICROPROCESSOR DATABOOK—1989**

Series 32000 Overview • Central Processing Units • Slave Processors • Peripherals  
Development Systems and Software Tools • Application Notes • NSC800 Family

## **PROGRAMMABLE LOGIC DATABOOK & DESIGN MANUAL—1990**

Product Line Overview • Datasheets • Designing with PLDs • PLD Design Methodology • PLD Design Development Tools  
Fabrication of Programmable Logic • Application Examples

## **REAL TIME CLOCK HANDBOOK—1989**

Real Time Clocks and Timer Clock Peripherals • Application Notes



## RELIABILITY HANDBOOK—1986

Reliability and the Die • Internal Construction • Finished Package • MIL-STD-883 • MIL-M-38510  
The Specification Development Process • Reliability and the Hybrid Device • VLSI/VHSIC Devices  
Radiation Environment • Electrostatic Discharge • Discrete Device • Standardization  
Quality Assurance and Reliability Engineering • Reliability and Documentation • Commercial Grade Device  
European Reliability Programs • Reliability and the Cost of Semiconductor Ownership  
Reliability Testing at National Semiconductor • The Total Military/Aerospace Standardization Program  
883B/RETSTM Products • MILS/RETSTM Products • 883/RETSTM Hybrids • MIL-M-38510 Class B Products  
Radiation Hardened Technology • Wafer Fabrication • Semiconductor Assembly and Packaging  
Semiconductor Packages • Glossary of Terms • Key Government Agencies • AN/ Numbers and Acronyms  
Bibliography • MIL-M-38510 and DESC Drawing Cross Listing

## SPECIAL PURPOSE LINEAR DEVICES DATABOOK—1989

Audio Circuits • Radio Circuits • Video Circuits • Motion Control Circuits • Special Function Circuits  
Surface Mount

## TELECOMMUNICATIONS—1990

Line Card Components • Integrated Services Digital Network Components • Analog Telephone Components  
Application Notes